**Digital Integrated Circuits**
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**Lecture-6**
**Schottky Transistor**
**Introduction to Bipolar Logic Circuits**

We shall begin with a brief recapitulation of what we had been doing in the last class that is the switching aspects of an inverter circuit. The circuit which we have been discussing quite familiar by now is given here, so you have a base resistance, a collector resistance and you have a supply voltage and this is the input point and this is the output point and in this circuit suppose you apply a voltage waveform of this type that is this goes up to, this is forward voltage $v_{F.}$ and then you have a reverse voltage $v_{R.}$. Then what is the sequence of switch happens, that is what we are interested in.

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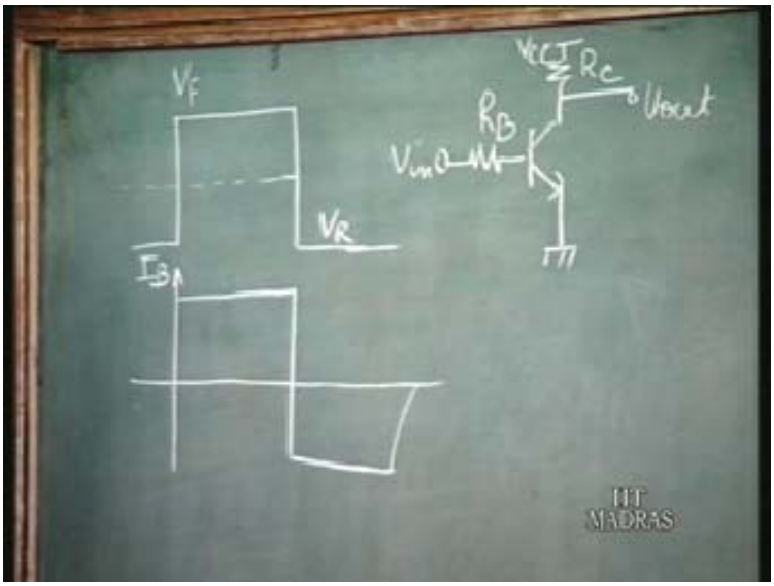


Now what is going to be the base current waveform that is the next thing of interest, $I_{B.}$ We have seen that $I_{B.}$ at this point you can assume it to be almost a constant and again here you know it remains a constant reverse base current flows and then finally it goes to zero, this is the waveform which we have. Let us call this $I_{F.}$ the forward current and you have a reverse current $I_{R.}$. Now you know that $I_{F.}$ we can write is nearly equal to $v_{F.}$ by $r_{B.}$ and $I_{R.}$ is nearly equal to $v_{R.}$ by $r_{B.}$ that is because we assume here that the input voltage is again that is $v_{F.}$ and $v_{R.}$ their magnitudes are much greater than the base emitter voltages because the base emitter voltage in this period is going to be very small compared to this input voltages. Only after at this point in time when the base charge has been completely discharged, the base emitter voltage tend to become sufficiently negative and so the reverse base current falls.

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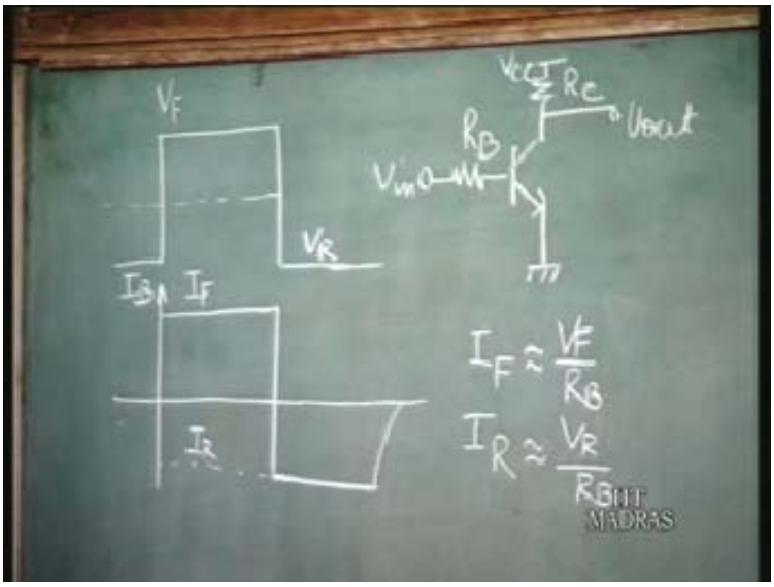


So with this assumption if we now take up the base current to plot the base charge, we have also seen that what happens is in this period, the base gets charged it builds up and then when the input voltage goes negative the base charges are removed. So basically goes to zero here. Now how do you calculate this base charges, what is the relation governing this? That we have seen the familiar relation $I_B$ is equal to $Q_B$ by $\tau_n$ plus dt. You get this nature of base charge variation, if you solve this differential equation for $Q_B$ and of course you have to take the proper initial conditions and then you get this nature we have already done that. of course what it means is when forward current is flowing then in the steady state once it reaches here this goes to zero $I_B$ is equal to $I_F$ so $Q_B$ is equal to $I_F$ $\tau_n$ and then this is the peak value and then it goes down. Now if you plot the collector current what happens is when the base charge is building up the collector current also builds up but then it reaches saturation.

The base charge when the collector current reaches saturation is given by $I_C$ sat into $\tau_t$ where $\tau_t$ is the transit time. So this is the value say when the transistor reaches saturation. So if we plot it here, drop this line here so the collector current keeps increasing here, reaches saturation and then although the base charge keeps building up the collector current has saturated. That is governed by the circuit, it cannot build up any further so it becomes a constant. At this point the base current has reversed but still the collector current remains at the saturation value till the base charge falls down to $I_C$ sat $\tau_t$ so the collector current will remain in the saturation value.

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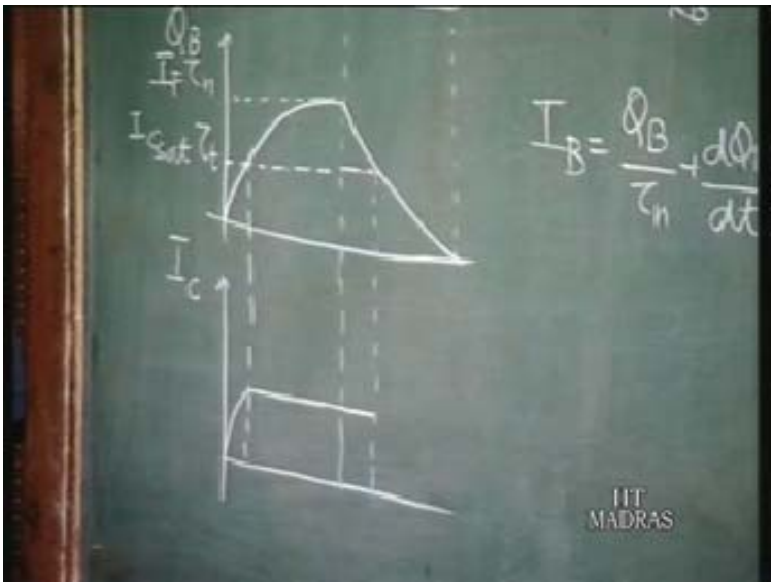


Up to this point and then of course it will discharge. So you have, you should say three components of delay here one is the on time, this is the on time you may call $t_{on}$ that is the time required for the current to reach the saturation value. Once after you have applied a forward voltage at the input then while switching off, there are two delay components one is called the storage delay time this value $t_{sd}$. That is the time required for the transistor to come out of saturation, after you have applied the reverse voltage and then there is another component which is the discharge time that is it comes out of saturation but finally what you have to do is you have to switch off the transistor.

The transistor has to go to cut off so what is the time required for the transistor to go from saturation to cut off that is called the discharge time. So this is the discharge time, let us call it $t_d$ so you have the various relations, $t_{on}$ we have already seen that relation, tou$_n$ ln what is the relation one by one minus $I_{Csat}$ by beta into $I_F$. So this is the time required for the transistor to turn on.

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Then you have the storage delay time so that is basically what you do is you solve this equation, we have already done that and then you see what time it requires to go to these values. Storage delay time we have also seen that $tou_n$ ln you have $I_F$ plus $I_R$ divided by $I_{Csat}$ by beta plus $I_R$. There is another relation we did not put it down in the last class but you can very well do it yourself, it's very simple. It is given by $tou_n$ ln $1 + I_{Csat}$ by beta $I_R$. $I_R$ actually is the modulus of current, $I_R$ is a negative current but that is what we are interested is in the modulus. So you have these three components of delay so these are the different relations, so given a particular circuit you can very easily calculate $I_{Csat}$.

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Also if $I_F$ and $I_R$ given the input voltages from the relations here for $I_F$ and $I_R$, if you know $I_F$ and $I_R$ you know the beta of the transistor you can calculate the different delay components of the particular circuit. It's very simple. Let us take a particular example just to give you an idea of what is the values of delays. So let us take an example, I shall take a particular problem here, $v_{CC}$ is equal to say 5 volts, $r_C$ equal to 1.5 kilo ohms, beta is equal to 50 and say $tou_n$ is equal to 10 nano seconds. Now if you just put these values, you can calculate all these things and if $I_F$ is equal to say 1 milli ampere, $t_{on}$ works $tou_2$, I just put down the results just to give the idea of the different delays works out to 0.66 nano seconds. If $I_R$ is also equal to one milli ampere, $t_{sd}$ will be equal to 6.31 nano seconds and $t_d$ will be equal to 0.62 nano seconds. Now in case $I_R$ is equal to 10 milli ampere, $t_{sd}$ is equal to 0.89 nano seconds and $t_d$ is 0.064 nano seconds. What comes out of this?

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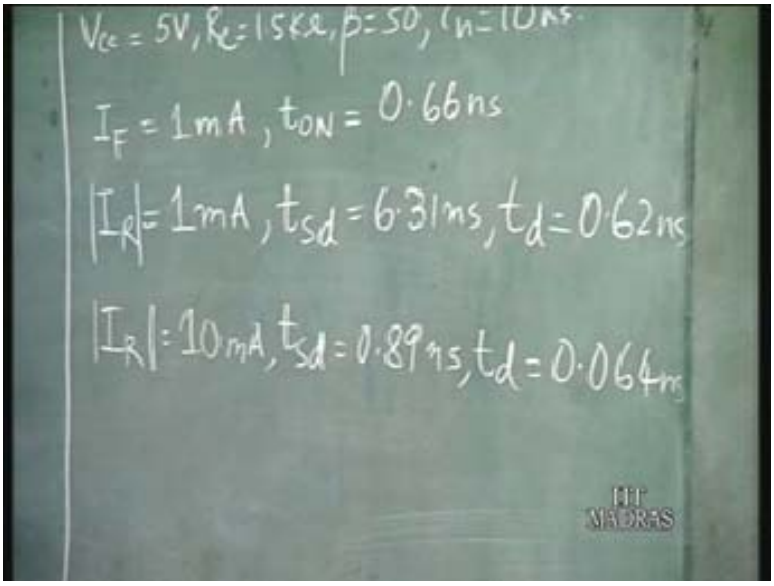


If this calculations, number one if you look at it, the reverse current is very important. How much reverse current is because it is the reverse current which is actually pulling out the charges, excess base charge is pulled out when a reverse current flows. So the larger the reverse current the faster is the removal of the excess base charge. So you can see here the storage delay time is the major component of delay and of course with increase in the reverse current the storage delay time reduces. So it is very important to be able to reduce the storage delay time because see the charges are very large when you go above saturation, there is lot of excess charge and that has to be removed. So that takes a lot of time so this gives you an idea of the delays. That is very important to have large reverse current to reduce the delays, to reduce the delay and of the delays the storage delay time is the major component and of course the storage delay time occurs when the transistor goes to saturation.

So this is about the different delay components. Before going ahead one more point, in addition to these delays we have actually neglected another component of delay which is due to the junction capacitances. These are all the stored charge delays, delays due to stored charge but if when you are changing the voltage across the junction there is a capacitance. So that capacitance also has to be charged and discharged so there is also going to be a delay due to that. So basically for the delay due to the junction capacitances, you have basically I think delay due to junction capacitances. You can look at it as a circuit like this, you have a resistance and you have a capacitance. That is the input capacitance, you have an r and c at the input side and you are applying a voltage like this. So the voltage across the capacitance must change so it is finally going to the steady state. Now the delay depends on the R C time constant. So the delay depends up on the r c time constant.

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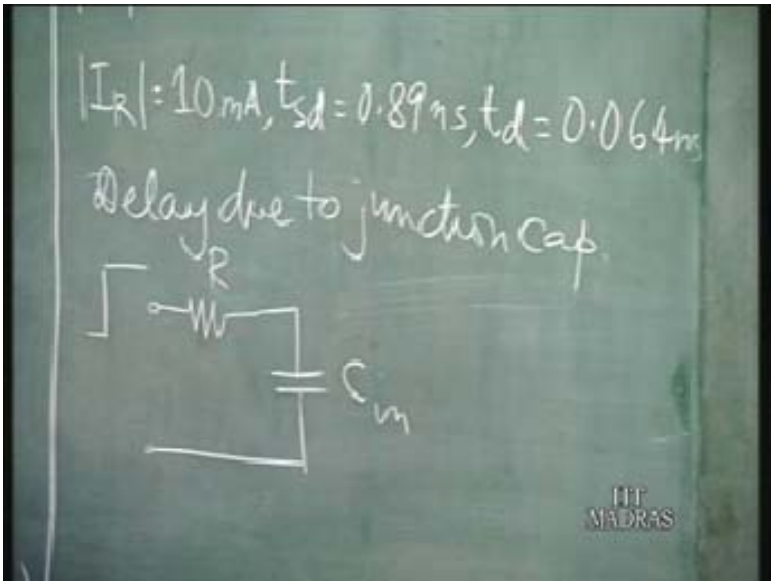


The larger the r c time constant, the larger is the delay and you can very well calculate that. It's not very easy to calculate provided you make an assumption. See this input capacitance is actually a junction capacitance which we are talking off and the junction capacitance is not a constant capacitance. It depends up on the voltage across the capacitance which makes it a very difficult problem to solve. Isn't it? That capacitance itself is continuously changing but for all to simplify the problem, we usually replace this input capacitance by an average capacitance. We call c effective, in the circuit it includes not only this base emitter capacitance, the disjunction but also you have the base collector junction capacitance which has to be reflected in the input side, you know how to do that miller effect, I think you are aware of that. So basically you have an input capacitance which has to be charged so now you can easily calculate that. For example if you take a small particular case that is input if the voltage across c effective changes from zero to v on say. That is when you are charging the input, it changes from zero to $v_{on}$ say the voltage across this and you have applied a $v_{F}$ here.

So you can solve this very easily and you will get that $t_{on}$ will be equal to r c effective ln $1 + v_{on}$ by $v_{F}$. Of course the assumption here is that $v_{n}$ is $v_{F}$, $v_{on}$ is much smaller than $v_{F}$, if that is the assumption then you get this. Basically the idea is it is going to be proportional to r c time constant. So you have these two components of delays, one due to the stored charge which is actually the diffusion capacitance which we are talking of. We have already seen the two type of capacitance, diffusion capacitance or stored charge capacitance and the other is the junction capacitance or the depletion capacitance. Now there is a basic difference in the two types of capacitances, the effects of the two types of capacitances which we shall see here. See if you look at this circuit here, come back to this circuit. Now if we increase both $r_{B}$ and $r_{C}$ by the same amount, suppose we increase $r_{B}$ and $r_{C}$ by the same amount, same factor.

What happens to these delays due to the diffusion capacitance, due to the stored charges? If you look at this expression now say $t_{on}$ what happens to see you have a $I_{Csat}$ by $I_{F}$, now if what happens to $I_{Csat}$ if you increase $r_{C}$? It reduces and $I_{F}$? Because you

are increasing $r_{B.}$ it also reduces, it reduces by the same amount if you are increasing both the resistances by the same factor. So what happens to $t_{on.}$? It remains the same. What if you take up $t_{sd.}$ this relation stored charge delay? Again see both I mean the numerator and the denominator would change by the same amount, if you change $r_{B.}$ and $r_{C.}$ by the same factor. If you increase $r_{B.}$, both $I_{F.}$ and $I_{R.}$ would reduce, $I_{Csat.}$ would also reduce if we increase $r_{C.}$ and $I_{R.}$ would also reduce and if the change in the resistance values in the same factor, this factor remains constant. No change in $t_{sd.}$ even $t_{d.}$, $I_{Csat.}$ by $I_{R.}$ remains constant.

So in this circuit if you change the values of all resistances you increase or decrease by the same factor, the delays due to stored charge component does not change. That is because you see again if you come back if you consider them as capacitance $r_{C.}$ time constant, the $r_{C.}$ time constant due to the diffusion capacitance. Now the diffusion capacitance is proportional to current and current is inversely proportional to resistance. So what is $r_{C.}$ time constant going to be? That is independent of r change because if r goes up capacitance goes down because the current goes down. So $r_{C.}$ time constant doesn't change, independent of change in the resistance that is diffusion capacitance but if you look at the junction capacitance, expressions $t_{on.}$ it is $r_{C.}$ effective and c is independent of currents. So if you increase r, the delay is going to increase. So these are the two basic difference in the nature of two delays.

So suppose the resistance values in the circuit are very high say, so what is going to happen? This delay due to the junction capacitance is going to dominate and then if you go on reducing the value of the resistances in the circuit, this delay is going to go down whereas the delay due to the stored charges is constant. So if you keep on reducing the resistances in the circuit, the delays due to the junction capacitances will slowly reduce and finally the delays will be determined by the stored charges.

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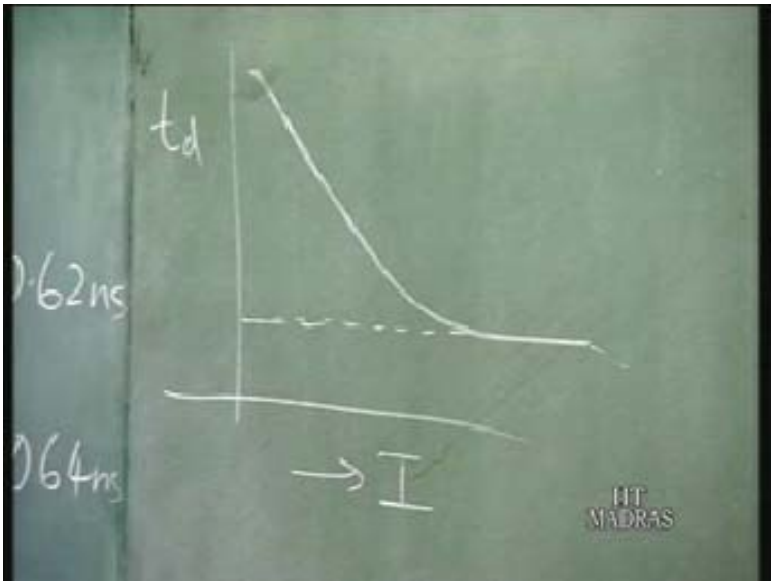


So if the resistance values are very high it is the junction capacitance delays due to the junction capacitance which is dominating or you can look it at other ways. If the current levels are very low, it is the junction capacitance delays which is dominating but if you increase the current levels by reducing the resistances then you are reducing the delays because the diffusion capacitance is constant, delays due to diffusion capacitance is constant. So you are reducing the delays and finally it becomes determined by the delays that are determined by the stored charge delays which is a constant, it doesn't change after and that delay which you finally arrive at which is the lowest delay in the circuit I mean basically if I just plot it versus current the delays, it will go down with increase in current because the junction capacitance. This is the delay due to the say the stored charges is a constant.

So finally it will go down and then it becomes a constant like that. If you go on increasing the current so it is going to become determined by the delays of the stored charges and what is this stored charge capacitance mostly determined by the storage delay time. So if you want to increase the maximum speed at which a circuit can be operated, you have to reduce the storage delay time. That is very important, so you can go on increasing the current on the circuit but initially the delay will fall finally it doesn't change any further because the delays due to stored charge is independent of that. So in order to increase the speed of the circuit, you have to find mechanisms by which the stored charge delay must be reduced or eliminated possible. The way to do it is to see whether transistor does not go to saturation. If the transistor did not go to saturation then the stored charge delay is eliminated. Now how to do that? Now if you had a circuit for example where you see when you apply a forward voltage what happens is the transistor output, the collector emitter voltage is going to drop as you go on increasing the base current we have seen that and when it reaches saturation $V_{CE}$ becomes equal to around 0.2 volts but suppose you had a circuit by which just when it was approaching saturation then the base charge storage it would stop by some mechanism that would be an ideal case.

Now that is really achieved in a type of bipolar transistor called a schottky transistor, I will just tell you what it is, it is called a schottky transistor. Now we have already seen what is a schottky diode, what is a schottky diode? A schottky diode is a metal semiconductor junction which has rectifying properties and a property of a schottky diode in comparison with a p n junction diode is that the cut in voltage is much lower. That is it in the forward conduction mode the current starts conducting at a much lower voltage for example I will draw this again that if you have a p n junction diode characteristics like this I V, schottky is going to be something like this. So it starts conducting at a much lower voltage, suppose if this is 0.6 volts say this may be 0.3" volts.

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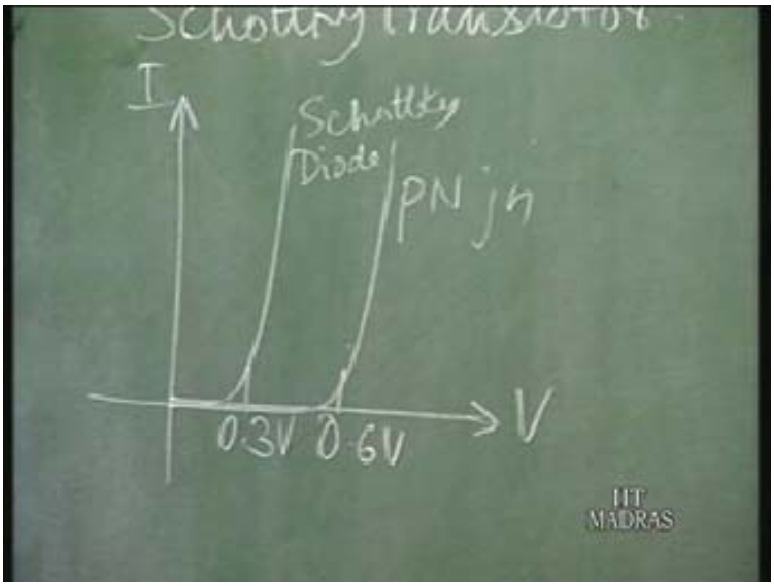


So that is the difference between a schottky diode and a p n junction diode in terms of characteristics. Now that is utilized in a schottky transistor. A schottky transistor is something like this, we have a normal transistor and between the base and the collector you have a schottky diode. Now what happens? Suppose if you look at this transistor what happens in the circuit? In order to drive this transistor to saturation what you do is that you try to increase the base current and as the base current is increased the collector voltage drops and what happens is that as the collector voltage drops the base collector junction gets forward biased and the transistor goes to saturation.

Now in this case say when this collector voltage is falling, suppose this collector voltage is 0.3 volts less than the base voltage what is going to happen? This schottky diode will start conducting for example let us say this base voltage is 0.7 volts and this collector voltage is falling because you are increasing the base current and when it reaches say 0.4 volts, what happens is this diode starts conducting and then the base current which was flowing into the base, the excess base current will start flowing into the schottky diode and there is a conduction path from here to here.

Whereas it flows through the schottky diode into the collector and this in the diode once it starts conducting it's a very steep characteristics, the voltage is almost clamped to that value, so this is almost clamped at 0.3 volts, maximum 0.4 volts.

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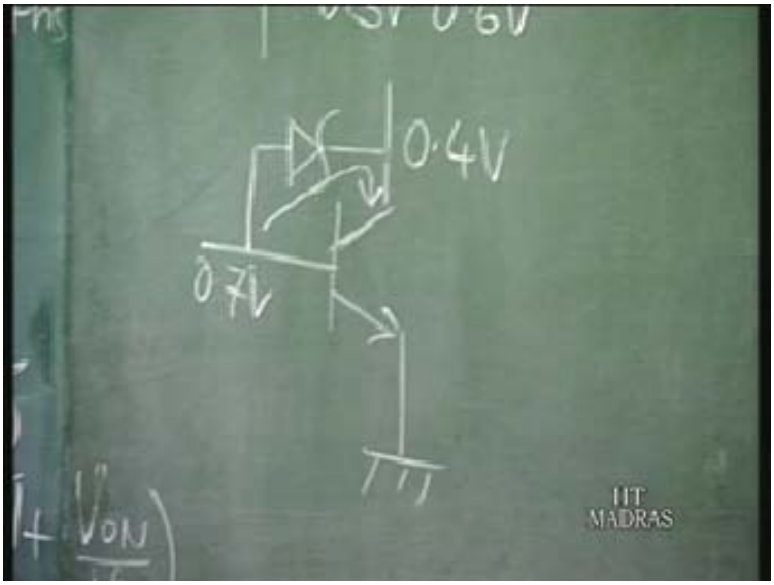


So this voltage, the collector voltage becomes clamped to around 0.4 volts or may be it may go down to 0.3 volts but it cannot go down below that and this is actually serving as the bypass path for the excess base current and the base charge cannot build up any further. So this actually prevents the transistor from going to saturation, the transistor does not go to saturation, it goes to the edge of saturation and then it gets clamped, the output voltage gets clamped. So when you have a transistor like this called the schottky transistor, the symbol for this transistor is this (Refer Slide Time: 31:14). This is the symbol for a schottky transistor so when I draw like this, it actually means that this is a transistor with a schottky diode between the base and the collector, this is called the schottky transistor and this transistor is not going to go to saturation because of this schottky diode will start conducting, when the transistor goes to the edge of saturation and obviously this transistor will not have the storage delay component which is going to make it a faster device.

In the circuit if you replace a normal transistor with a schottky transistor, you get this improved performance in terms of speed. Now it's a very good concept, you have a schottky diode between the base and collector but how do you realize it. Technology, is it going to be very difficult if you want to introduce a schottky diode between base and collector. Let us see how one does it? Actually the beauty of this is that it is very conducive, it doesn't make technology very much difficult. I just draw the cross section of the bipolar transistor first, the integrated circuit bipolar transistor. So this is the n +

p, n + n, plus this p, p, p, so this is the emitter contact, the base contact here and this is the collector contact.

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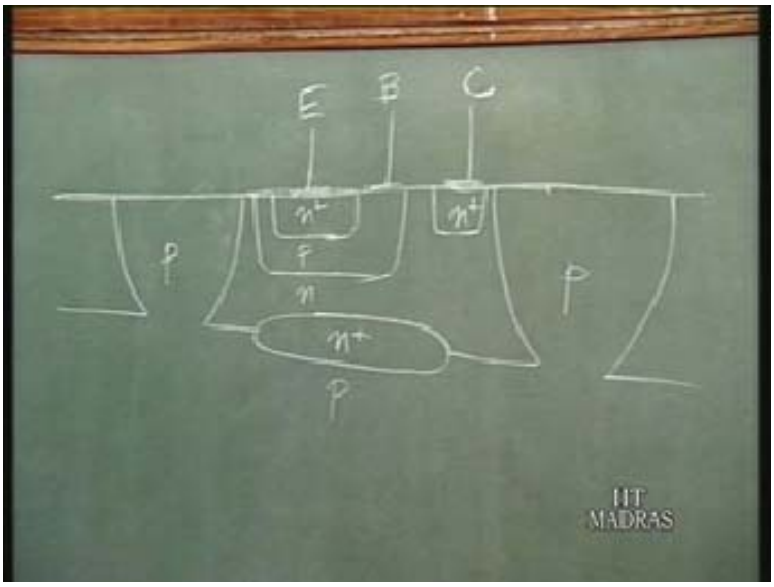


So this is the integrated bipolar transistor. So you have an island I will just draw the top view also because I think to give you the overall picture. So this is the p i length, this is the top view then you have the emitter which is like this then you have the base, then you have the n plus collector and so now the contacts this is the emitter contact, this is the base contact and you have the collector contact. Of course you have the buried collector also which is somewhere underneath. So this is actually the overall picture, so this is the p plus actually this is the island in which you have the transistor. This is the top view, we are looking from the top, this is the cross section. So this is from top view which is actually circular and then you see the cross section. so this is an island in which the device is formed a p n junction which isolates which is actually reverse biased all the time, so that it isolates the different transistors on the same chip.

So this is the emitter contact which is here, the base contact which is here so this is the base p region and this is the n plus collector region and this is the collector contact. Now why do you require n plus? For collector because the metal which is usually aluminum say gives a holmic contact only with n plus, with n type it gives a schottky contact. Schottky means rectifying properties, so you would require a holmic property, holmic contact here so here you have to make an n plus layer. Now how do you get a schottky transistor? It is very simple, the only modification that you do is in this circuit is that this base contact which you have here, look at this. You just extend it over the n type collector region, that's all. What do you have here? Metal n type semiconductor.

This region behaves as a schottky diode, here it behaves as a schottky diode the metal semiconductor n type semiconductor here behaves as a schottky diode. So from the base

contact to the collector so this is the collector region, you have a schottky diode. So this is the base, it goes to the base and again you have a contact to the n type collector. So just if you go back to this one here, so from the base you have a schottky to the collector and you have the normal transistor.
So this is very simple, you just have to extend it basically the base contact has to be extended over the n type collector region, so that gives you a schottky transistor. So technologically it is very simple you don't have to do too much, it is very simple to convert a normal bipolar transistor to a schottky transistor. So you see that in a digital circuit to improve the maximum operating speed of the circuit, you have to reduce the storage delay time and to do that, you can have a schottky transistor. So you can prevent the transistor to go to saturation, if you can just make it switch between the cut off and the active region rather than from cut off to the saturation region and that is done, one way to do it is to have a schottky transistor which actually does not go to saturation. So basically in bipolar digital circuits they can be classified into two categories bipolar logic families, one is called saturated logic and the other is non-saturated logic.

In saturated logic the transistors are switched between the cut off and the saturation region. In non-saturated logic the transistors do not go to saturation. They are generally higher speed circuits and the transistors go from cut off to the edge of saturation. So the output voltage would not reduce to 0.2 volts as such, it would reduce to around 0.4 to 0.3 volts. Actually the logic low would go up a little bit but that is a small price to pay for the gain in speed which you achieve. So the examples of the saturated logic are the TTL and the i squared l whereas the examples of non-saturated logic, you have the schottky TTL where you use schottky transistors and you also have the ECL emitter couple logic where the transistor also does not go to saturation but in that case you do not use a schottky transistor but you adjust the voltage levels in the circuit in such a way that the transistors actually do not go to saturation. We shall discuss that in detail when we come to ECL but there also the transistors do not go to saturations.

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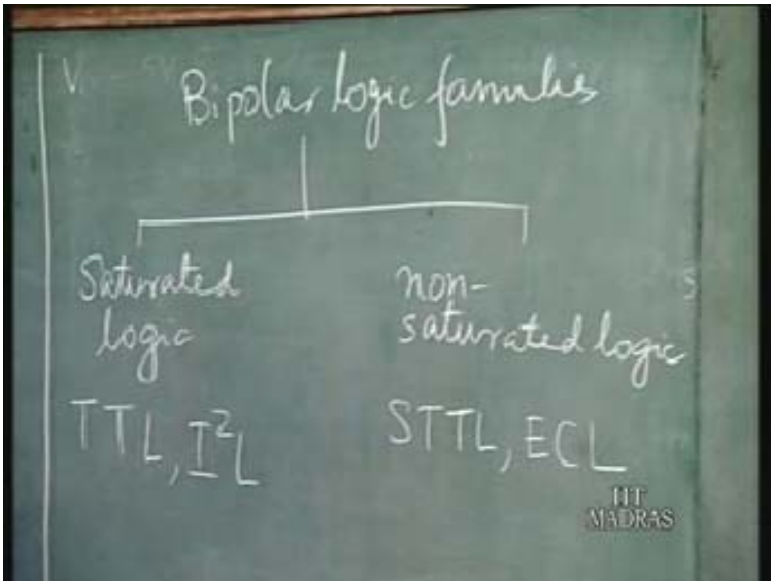


These would be obviously much faster compared to the saturated logic family. So this gives you an idea of the different types of logic families.
Basically classification based on whether the transistors are going into saturation or not. So with that we come to the end of this discussion on switching properties of this bipolar transistor inverter circuit which is very important. These concepts which we have developed, when discussing this is very important in understanding basically the delays in any logic circuit. So if you understood this very clearly, then one can very easily appreciate the different delays, I mean the different delays in the different logic families and how one is different from other.

Actually before going into the logic families as such, one topic we shall take up that is the different characteristics of logic families that is when you take up a logic family what are the different properties by which you can actually characterize a logic family. What are the different specifications you talk of? Suppose you want to make a distinction between two logic families, you say that this logic family is better than this but better is a very vague term, so you have to say in terms of certain characteristics, better or worse. So what are the different characteristics or figures of merit of these logic families? You just have some idea of that before we actually go into the logic families so that we can discuss them in terms of these characteristics or specifications.

The different characteristics or specifications or figures of merit, characteristics or specifications I think specification is a better word, specification of logic families. They are propagation delay that is it gives you an idea of the speed of the device, speed of the logic circuit, how fast or slow it is. So propagation delay, there are also some other related specification they are called rise time and fall time. So this propagation delay rise time, fall time they all relate to the delay component of logic circuit.

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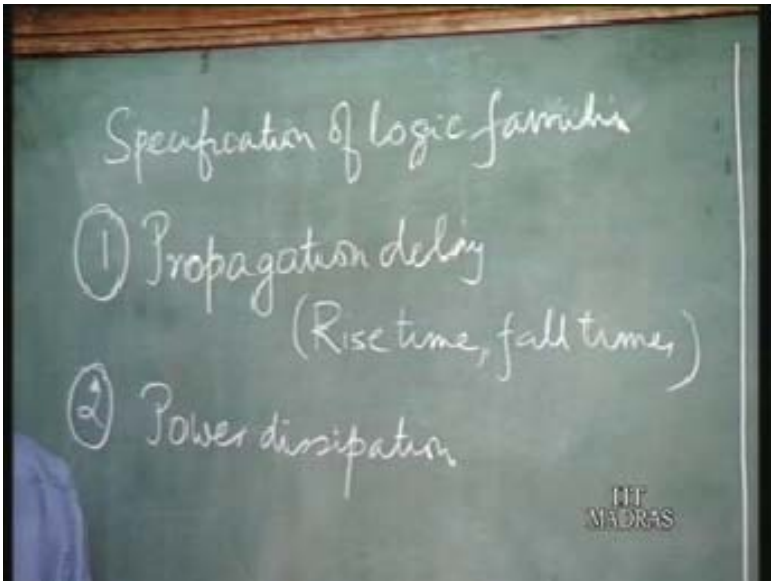


We shall come to these definitions that is very important before we actually go into this discussion. then power dissipation is also very important, nowadays in fact it has become very important, characteristic of a logic circuit because of the fact that the train nowadays is to pack in more and more circuits, more and more components in a given area, you make the devices smaller so you are having more number of components in a given area.

So the power dissipation is actually going up in a given circuit. So that puts a limit on the packing density, so one has to really think of power dissipation. So we shall see about power dissipation, in fact we shall also see how these two are related, they are related as we had seen when we put up the curve with the current, if you increase the current the delay goes down. Of course it becomes a constant but if you increase the current, you are also increasing the power dissipation. So if you increase the power dissipation there is a possibility of reducing the delay, so they are interrelated. In fact all these characteristics may be sort of interrelated. So your propagation delay you have power dissipation, the other is noise margin. That is it gives you an idea of how much noise a circuit can tolerate.

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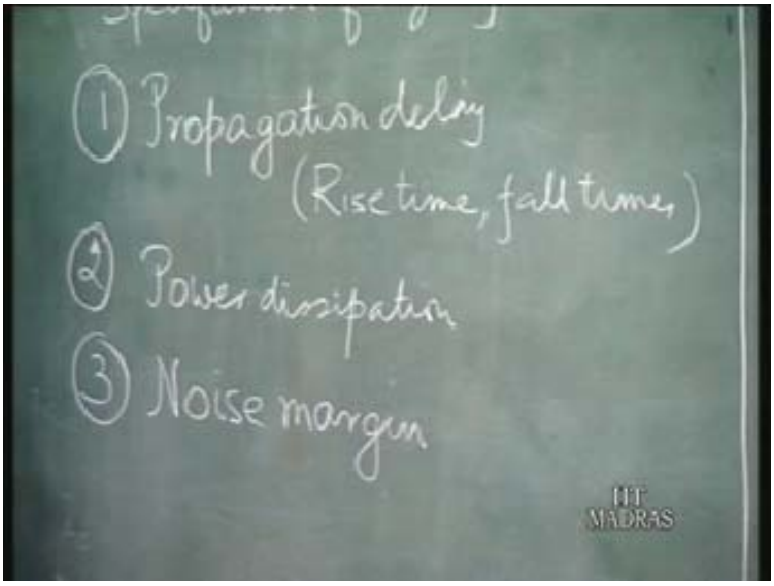


So that is also important and also the other important thing is fan out. That is fan out, fan in also to some extent that is if you have a gate say for example if you have a NAND gate the two input whatever the NAND gate, so this output can be fed as input to subsequent stages of gates. So how many outputs can you connect to this gate, that tells you about the fan out? So there is a limitation because if you go on increasing the fan out, the other characteristics start getting degraded. The speed may fall all these things, so again there is a limit on the fan out. So all these things are very important characteristics of logic families and when we discuss one with respect to the another, we have to discus in terms of these specifications and so in the next class we shall take this up, give you the proper definitions and then we shall move on to actual circuits. We shall take up the actual logic circuits, we will start with TTL and then go to i square l ECL and all that so we shall stop here today.