Digital Integrated Circuits
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Lecture -40

Transmission line effects

We have now come to the end of this course. In this course we have studied various aspects of digital integrated circuits and mostly we concentrated on the component that is effect of the different components on the performance of the circuit. In today's class we shall take up another aspect which we have not discussed so far that is the effect of interconnects. That is if we have a digital circuit say for example a NAND gate which is driving another NAND gate, there is line which carries the signal from the output of one gate to the other, so this is an interconnect.

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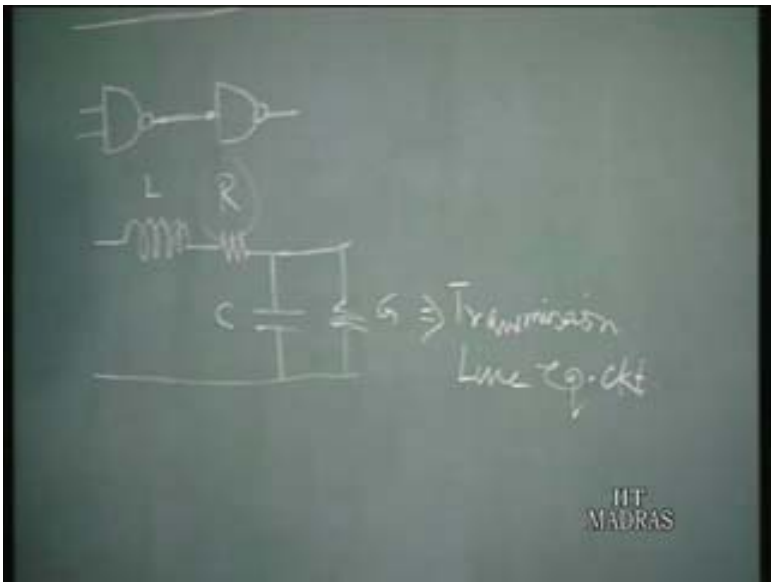

Now what is this effect of this interconnect? We normally expect that the signal at the input of the gate which is being driven is identical to the signal at the output of the driving gate. That is this is a short circuit and there is no difference between these two and input of this gate and the output of the other gate but it is not always true. The interconnects have lot of effect on the performance of the digital circuits especially in today's world with the shrinking of device dimensions, the gate delays have reduced tremendously while this effects of interconnects remained as before. In fact the delay of modern day integrated circuits is controlled to a large extent by the effect of this interconnects. In today's class we shall take up the effect of the interconnects on the performance of the digital integrated circuits.

Now this interconnects have a number of different effects for example it may cause a delay of the signal that is the signal which is going from output of this gate to the input of the other may get delayed and also that may cause distortion. That is the nature of the signal at the input of the driven gate may be different from the nature of the signal at the output of the driving gate. So that may cause a lot of problems. We have to understand these effects and try to take remedial measures. In today's class we shall see the different effects of the interconnect on the performance of the digital circuit.

This interconnect line which transmits a signal from one point to the other is called a transmission line can be modeled as consisting of an inductance, resistance and a capacitance and a conductance. So L, R, C and G. Now these components are distributed throughout the line, so these are not lumped components but these will be distributed throughout the interconnecting line. Usually for a unit length of the line, this L will represent the inductance per unit length or the resistance per unit length, C the capacitance per unit length and G the conductance per unit length.

This is the equivalent circuit of a transmission line which is used to convey a signal from one point to the other. This is a transmission line equivalent circuit. In many cases for simplicity of analysis at first what we shall do is we shall assume that R which is the resistance is very small and this G which is the conductance between the two lines that is very high. So that we have the equivalent circuit consisting of only the inductance and capacitance. This is L, this is C and this is called a lossless transmission line.

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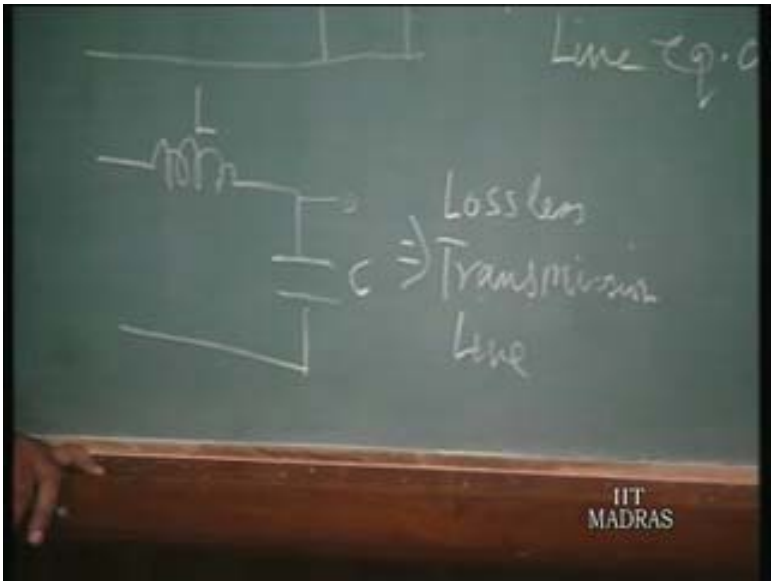

We shall first take up the effect of this lossless transmission line on the performance of integrated circuit and then we shall consider the effects of say for example the resistance on the line subsequently.

Now what is the effect of this transmission line? Let us take a particular case suppose we have a voltage source and then we have a switch and then this is the transmission line which transmits the signal.

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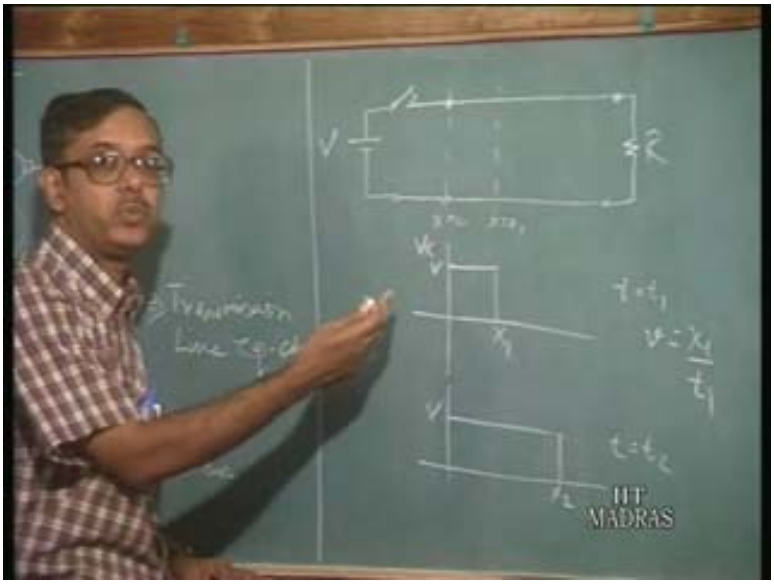

Then of course we may have a load resistance, this voltage V. Now suppose at t = 0, the switch is closed. Now when the switch is closed what happens is this voltage waveform is not immediately available at the load end. The voltage front will move with a particular velocity that is if you call this point x =0, this point x = $x_{1.}$. So at t = $t_{1.}$ if you plot the voltage across this line this is what you see that is the voltage front has moved by a distance $x_{1.}$ at say time t = $t_{1.}$.

At time t = $t_{2.}$ it may move to the point $x_{2.}$ and this is v. So this voltage v is not instantaneously available at the load end, it moves with a particular velocity v and so if it has moved $x_{1.}$ at time $t_{1.}$ then the velocity will be given by $x_{1.}$ by $t_{1.}$. This is the velocity of the wave, the voltage front. Together with this voltage front you also have a current front which also moves that is if you the current along this line also will move and there will be a particular ratio between the voltage and the current.

If the voltage is v at this point, if you take the current which will be i is related to the voltage v by a certain ratio we shall come to that. This voltage moves with a velocity v. Now what is this velocity of this voltage front and also the current front? It can be

shown that the velocity v is given by 1 by root of LC where L is the inductance per unit plane and C is the capacitance per unit plane.

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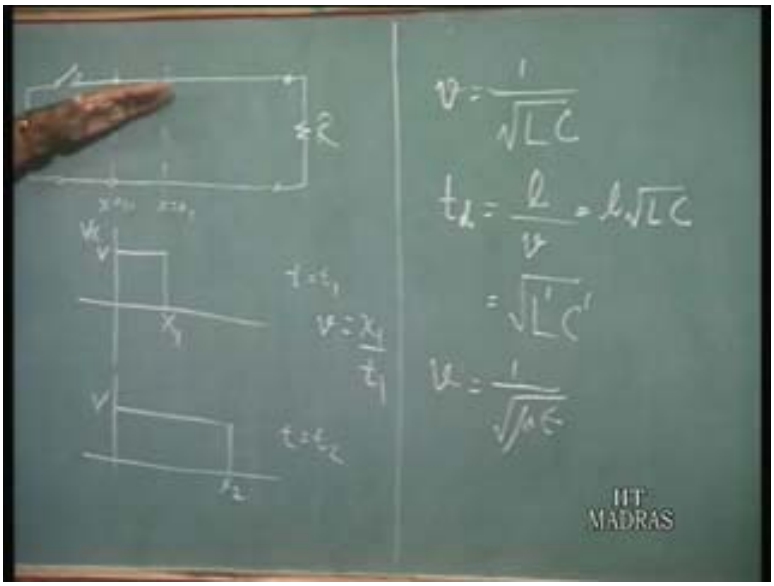

That is the velocity with which this waveform will move along this line. Now L is the inductance, C is the capacitance and so what is the delay of this line? delay of the line is l by v. This will be l into root of LC. Now since L is inductance per unit length and C is capacitance per unit length, we can write the delay as root of product of L prime and C prime where these are the total inductance and total capacitance of the line. L prime is L into the length of the line and C prime is the capacitance per unit length into the length of the line. This is going to be the delay of the line. For a particular line there is an associated delay, the time required for the wave to move from the source end to the load end.

Now this velocity which we have expressed as 1 by root LC can also be expressed as 1 by root of mu into epsilon where mu is the permeability and epsilon is the permittivity of the space between the pair of lines here. It is the permeability and permittivity of the space. You see that one interesting aspect is that the velocity in fact depends on the properties of the medium between the two lines and it's not really dependent on the property of the line themselves. Now this can also be expressed as C_0 by μ_r ϵ_r where C_0 is the velocity of light in vacuum and μ_r is the relative permeability and ϵ_r is the relative permittivity of the intermediate space between the two lines. The C_0 as you know is 3 into 10 to the power 10 centimeter per second.

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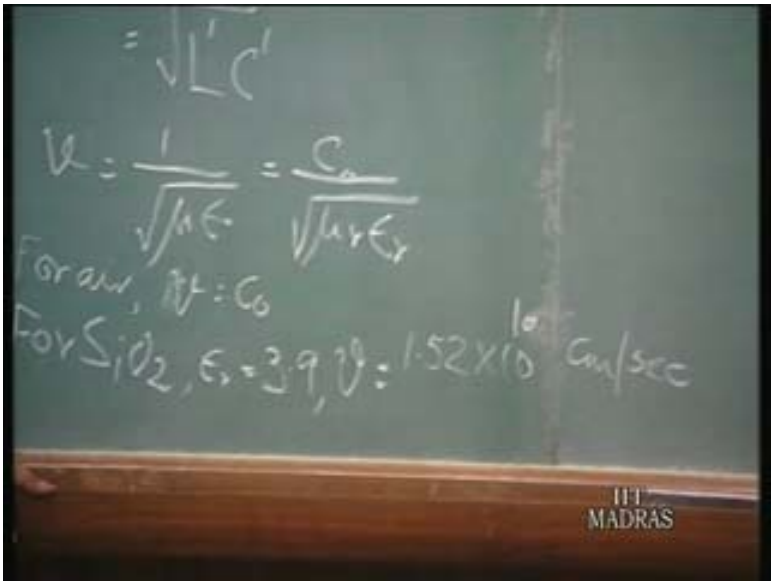

Now if we assume the intermediate medium to be air, so if mu_r and $epsilon_r$ are both equal to 1 so $V = C_0$.. Now say if the intermediate medium is silicon dioxide which is we know the dielectric material which is used in silicon devices over which the interconnecting lines will run. So we have $epsilon_r$ is equal to 3.9, this gives us a velocity of 1.52 into 10 to the power 10 centimeter per second which can also be written as this velocity. Better way to write it is, this is equal to 15.2 centimeter per nano seconds. In one nano second the wave will move by 15.2 centimeters so that is the velocity with which the wave front will move.

It is not instantaneous, the voltage at the source end of the line is not instantaneously available at the load end, so there is a time lag involved. Now coming back to the ratio of the voltage and the current on the line, this voltage and current on the line will have a ratio which is given by R_0 which is called a characteristic impedance of the line. As the voltage front moves along the line, there is a corresponding current front which also move along the line and the ratio of the voltage and the current is given by R_0. Let us calculate the value of R_0. As the voltage front say here moves by a small amount dx say from any point it moves by a small amount of dx.

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The extra capacitance that has to be charged on the line is say C into dx. The extra capacitance because C is the capacitance per unit length and so if the wave front has moved by distance dx so the extra capacitance is C into dx. We say dc is equal to C into dx that is the extra capacitance, C is the capacitance per unit line. I shall put it C prime, the total extra total capacitance.

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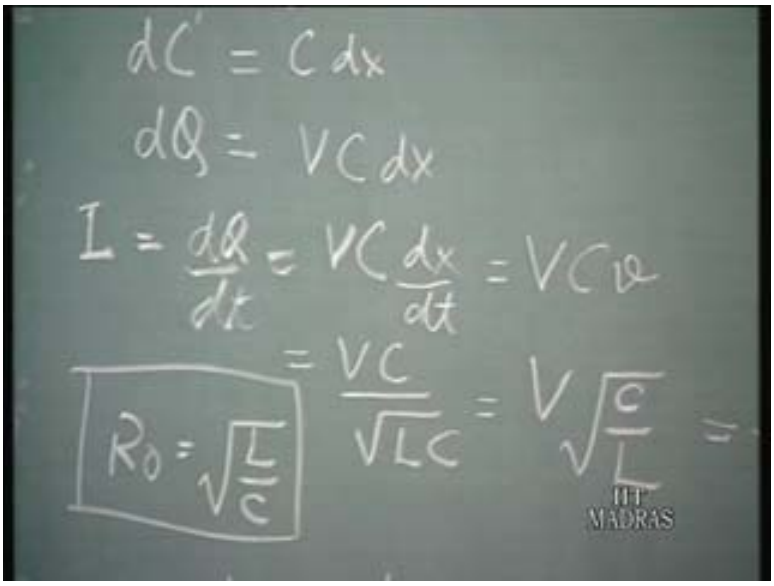

What is the extra charge that is required? That is this is the capacitance, the voltage which is charged by voltage V so V C dx that is the total charge and therefore the current is given by we know dQ dt so we get VC into dx dt which is nothing but the velocity.

We get VCv. Now this V is given by 1 by root LC. So 1 by root LC, this gives us V root C by L. Now if you write I as equal to V by R_0 we can see that R_0 is equal to root of L by C. This is the characteristic impedance of the line, it is related to the inductance per unit length of the line and the capacitance per unit length of the line. In fact if you bring the two lines, it is basically in this transmission line if the two lines are brought closer to one another, the capacitance goes up, the inductance goes down so R_0 will go down. Basically it also depends on the characteristic impedance of the line which will depend on the geometry of the line.

Basically the transmission line as we have seen is characterized by these two parameters. That is the delay of the line t_d which is as we have seen is given by the product of root of the product of the total inductance and total capacitance of the line L prime C prime. This is the delay of the line and the characteristic impedance which is R_0 equal to root L by C so these parameters. With the help of this analysis we shall now see the effect of these transmission lines on the effect of the signals which are to be transmitted from one point to the other. We have seen the two parameters, the delay line and the characteristic impedance. Now let us look at the effect on the transmission line. Suppose we have another signal source and voltage V and we have a transmission line.

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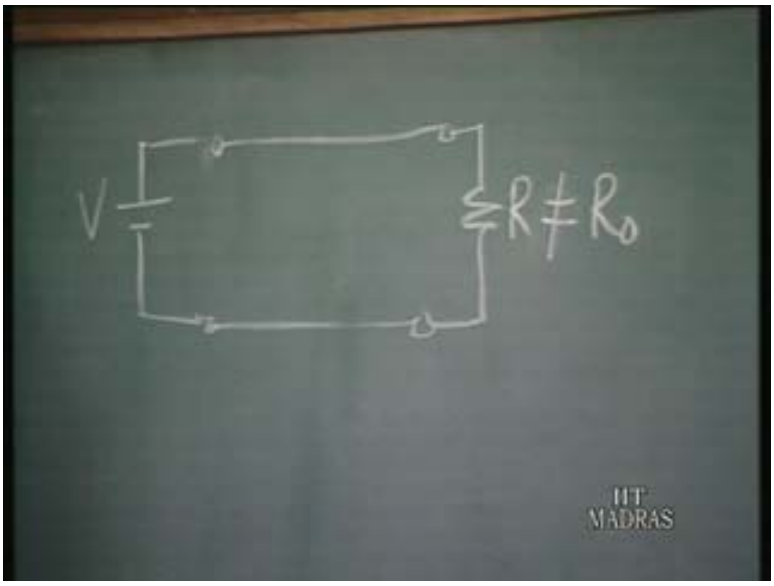

As we have seen that the voltage front and the current front will move along the line and the ratio is given by the characteristic impedance R_0. If this transmission line is infinitely long then these voltage front and current fronts will move along this line maintaining this ratio, there is no problem. Now again if we assume that there is a load resistance and the load resistance is equal to the characteristic impedance. Again what will happen is the voltage front and the current front will move maintaining a ratio of R_0 and once they reach the load end of the line, again since the load resistance is also R_0, there is no problem. Because again the ratio of the voltage and the current at the load end is equal to R_0 but suppose this load resistance is not equal to R_0 that is R is not equal to R_0.

Then what happens? Along the line as the voltage and current fronts are moving, the ratio of the voltage and current is R_0 but at the load end, the voltage the ratio of the voltage and current has to be R which is not equal to R_0. How do we take this into account that is having a ratio of R_0 along the line but having a ratio R at the load end. This can be explained or this can be sort of taken care of, if we consider reflections from the load end. That is there is a transmitted wave and there is a reflected wave, that is a part of the wave which moves to the load end, gets reflected back from the load to the source end. Now the reflected wave, the amplitude so if the transmitted signal amplitude is V, the transmitted voltage is V the reflected wave is going to be rho into V where rho is called the reflection coefficient.

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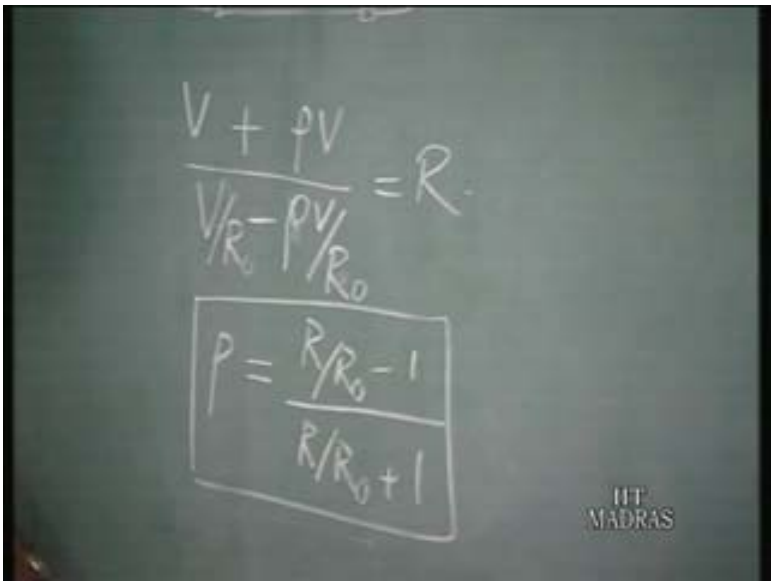

The reflected voltage is rho V. The total voltage at the load end is going to be V + rho V and if the current I is the incident current at load end then the reflected current is equal to rho I but it is in the opposite direction to the incident current. It is going to be minus rho I. Now this I is equal to V by R_0 because that is the ratio of the voltage to the current in the line. So V by R_0 is the incident current so the reflected current is going to be minus rho V by R_0. We can write this V by R_0 minus rho V by R_0. This is the ratio of the voltage and current at the load end and this should be equal to R. So V plus rho V divided by V by R_0 minus rho V by R_0 is equal to R.

Now from this we can just find out the value of rho. Rho can be expressed as R by R_0 minus 1 divided by R by R_0 + 1. This is the expression of rho which is the reflection coefficient. It is related to the ratio of the load resistance to the characteristic resistance of the line. Now from this we can see that the rho will always lie between + 1 and - 1, the value of rho is always between + 1 and - 1. When R tends to infinity that is it is sort of open circuit, rho will be equal to 1 and when R tends to zero that is a short circuit, rho will tend to -1.

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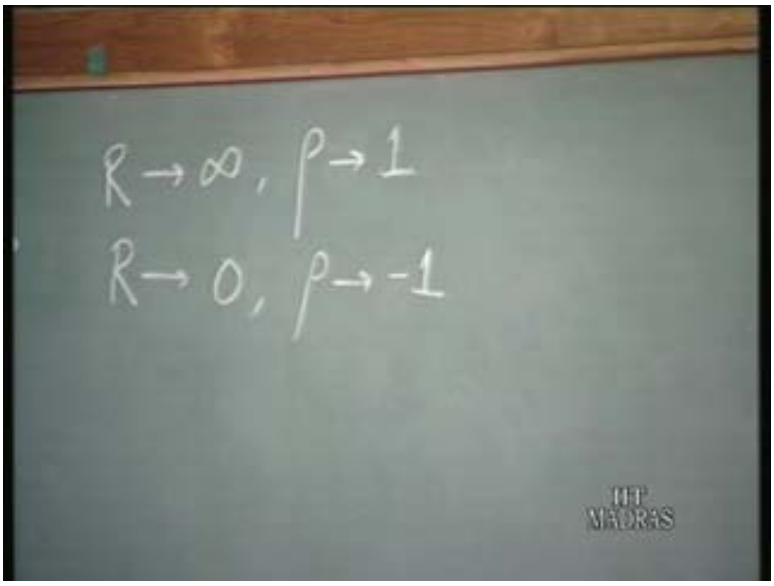

The extreme values of R that is when its open circuit, rho is going to be +1 and when R tends to zero that is it is a short circuit then the rho will tend to - 1. These are the ranges of rho, rho can lie between - 1 and + 1. For all intermediate values of R, rho will lie somewhere between + 1 and - 1. Knowing the values of R and R_0, we can calculate the rho that is the reflection coefficient and from that we can analyze the effect of the transmission line on the signal. That is what we shall take up next. Now let us consider a voltage source V having a source resistance R_S. This is driving a transmission line having a characteristic resistance R_0 and a delay t_d, we have a load resistance of R_L.

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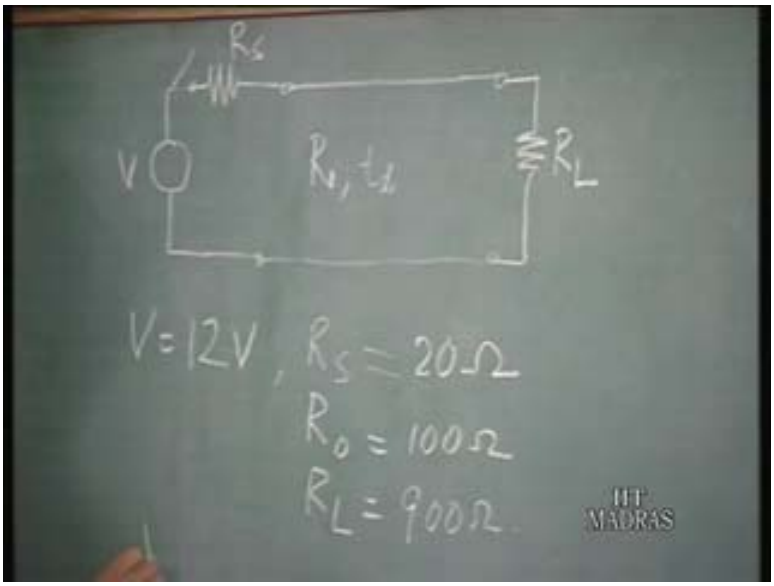

Now let us take some values for all these quantities here on the board and try to see what is going to be the nature of the waveform. How to calculate or how to analyze the nature of the waveform? Suppose V is equal to, as a dc voltage 12 volts and we also have a switch here. So its turned on at a time t =0, let R_S is equal to say 20 ohms, R_0 say is equal to 100 ohms, R_L is equal to say 900 ohms. These are the different resistances and the voltage source V is driving that line. Now if we were to assume that this transmission line is basically a short circuit then what do we expect? As soon as the switch is closed the output voltage, the voltage across the load resistance will be equal to V_{output} or across the load resistance V_L is equal to R_L by R_S plus R_L into V that is equal to 900 by 20 plus 900 into 12.

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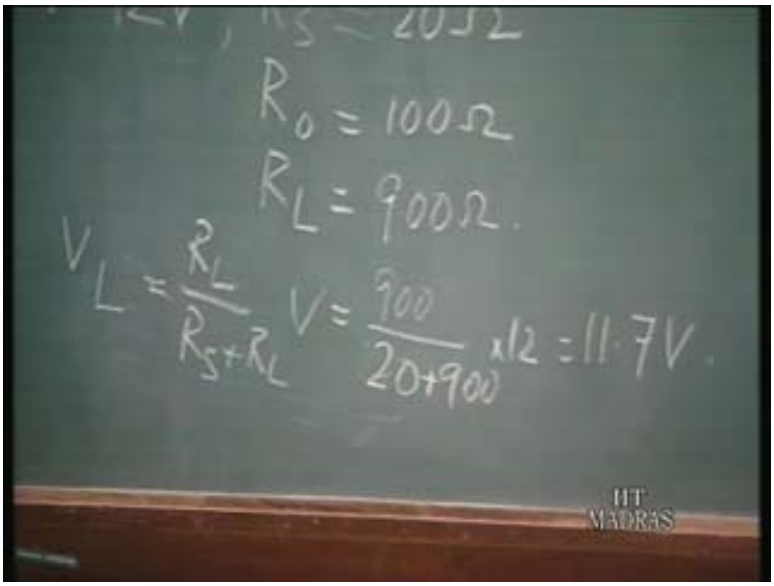

That may be almost around say about 11.7 volts. The voltage at the load end will be 11.7 volts. This is if we neglect the transmission line properties but let us see what we are going to get if we now analyze it from a transmission line point of view. In order to do that what we have to do is we have to calculate the reflection coefficients at the load end and the source end that is the first thing to do. So rho_L is equal to, we have already seen the expression for the reflection coefficient so that is going to be R_L by R_0 which is 900 by 100 - 1 divided by 900 by 900 + 1. So this is going to be 0.8.

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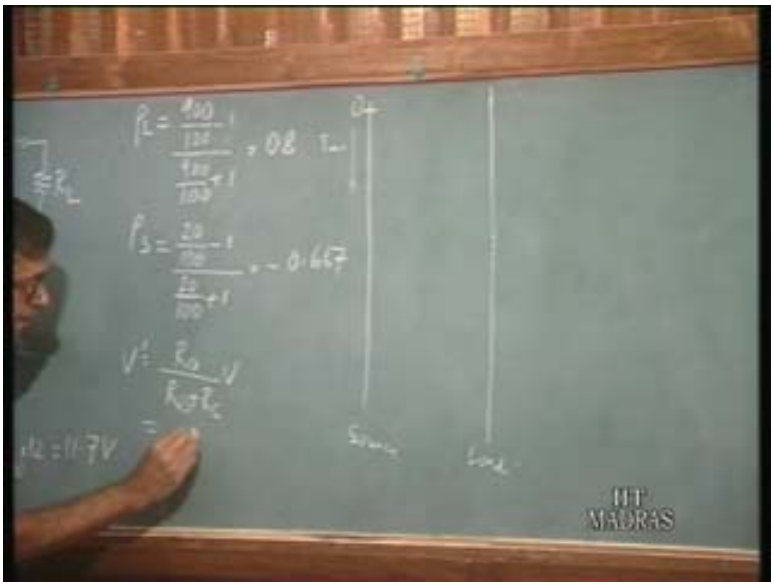

Rho$_S$ that is at the source end will be 20 by 100 minus 1 divided by 20 by 100 plus 1 so this is in fact going to be negative. In fact when the load resistance is less than the characteristic resistance, rho is always negative and when the load resistance is greater than the characteristic resistance rho is always positive. So this works out to minus 0.667 so these are the reflection coefficient. Now what we do is to find out the waveform there is a particular diagram which is drawn. It is drawn like this. This axis on this side is the time, this is zero say, this is the source and this is the load.

So it takes a time t_d for the waveform to move from the source end to the load end. Now what happens is initially a voltage front will move from the source end to the load end. Now what is the value of the voltage front? Here you see that at this end this is R_0 and this is R_S, so at this point if you say a voltage V prime is there which is going to move, what is the value of this voltage V prime? V prime will be equal to R_0 by R_0 plus R_S into V so that is equal to in this case R_0 is 100 and R_S is 20 into V that is 12 that will give 10 volts.

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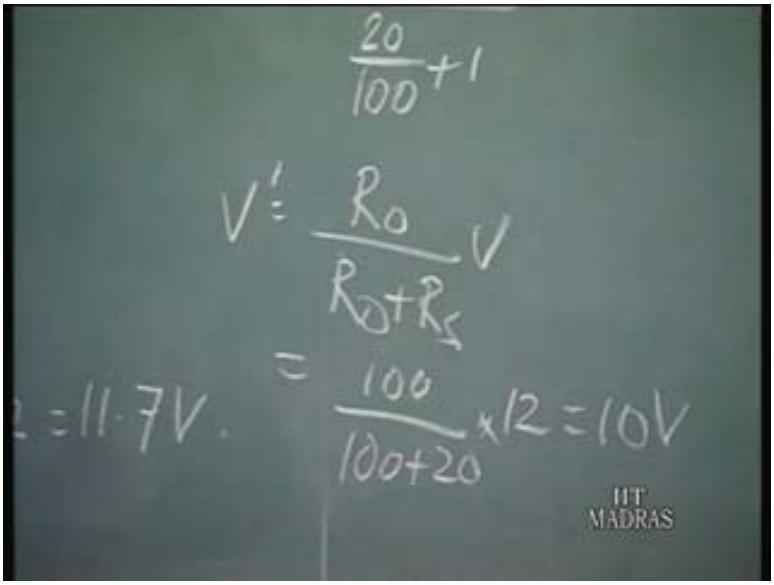

A voltage front of 10 volts is available here at the source end of the transmission line which is going to move towards the load end of the line. If we come back here in this diagram this is at time t =0 and at time t = t_d you have a 10 volt. This 10 volt front moves and reaches the loads end. Now this gets reflected and the reflection coefficient is at the load end rho_L.

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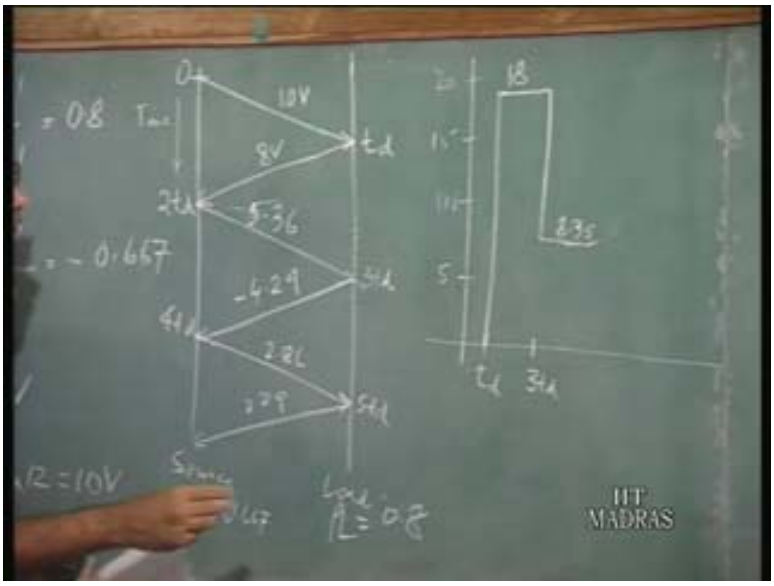

I will write it here is 0.8 and at the source end rho$_S$ is equal to - 0.667. The reflected wave here is 0.8 times the incident wave.

This one is 8 volts, so 0.8 times 10, 8 volts get reflected and reaches the source end at twice t_d. If we now observe the waveform at the load end at t_d which is equal to the delay of the line. The voltage you have is 10 + 8 is equal to 18 volts.

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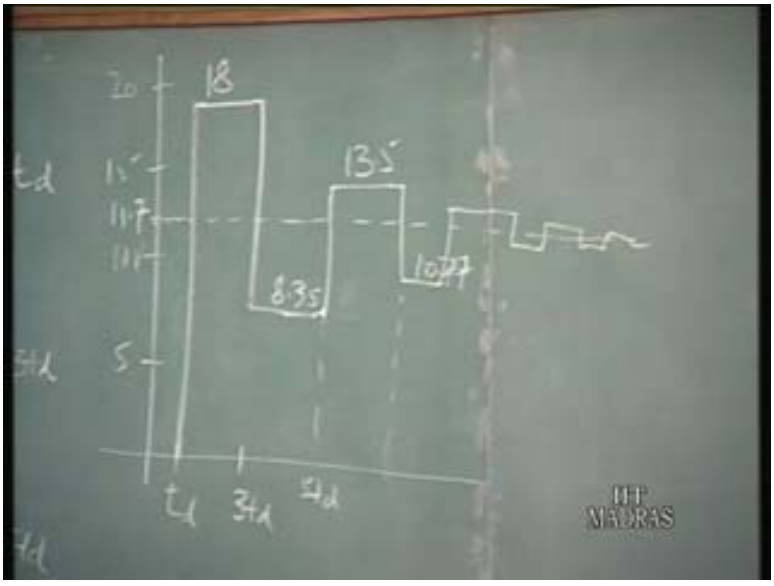

If this is 10 volts, 20 volts, 5, 15 volts so the waveform goes all the way up to 18 volts at $t = t_d$. Here again we come back to this diagram. This 0.8 volts has gone back to the source end. Now again this is going to get reflected from the source end with a

reflection coefficient equal to minus 0.667. The value of this is equal to, so 8 into minus 0.667 will give us minus 5.36 and then this is going to reach here at 3 t_d and then again you have another reflection at 3 t_d. The value here is going to be 0.8 times minus 5.36 which is equal to 4.29 - 4.29. What happens is at t =3 t_d, if we go back to this diagram now the voltage is equal to the sum of all these components 10 volts + 8 volts - 5.36 - 4.29.

The voltage here is due to the voltage which started off 3 t_d back and underwent this reflection, the wave which started off t_d back and underwent this reflection. We have to add up all these components. If we add up all these components we find that this is going to go down to 8.35. This is actually 18, this is 8.35. This is 4 t_d again this goes back here at 5 t_d and so this value here is 2.86 then again 0.8 times that is going to be 2.29. So at 5 t_d, the voltage will go up to 13.5, this is the sum of all these components. Similarly if we carry on this analysis we find that this is 5 t_d. At 7 t_d it goes down to 10.77.

Finally what we see is if we carry on this analysis for more lengths of time, you will find that it finally settles down to the value of 11.7 volts which is the expected value. If you go up like this and then come down and finally it will settle down to this value of 11.7 volts which is the voltage we expect if the transmission line is to be neglected. So in actual practice we will have a waveform which we see is very much distorted and it takes some time to settle down to the final value. This is the effect of the transmission line on the signal.
Now we have taken a particular case of a particular problem where we have defined the source resistance and the load resistances. Let us take an extreme case say for R_L equals infinity and R_S equals zero then what happens? In that case what we get is rho_L will be equal to 1 and rho_S will be equal to minus 1 plus this rho_L is plus 1 and rho_S is equal to minus 1.

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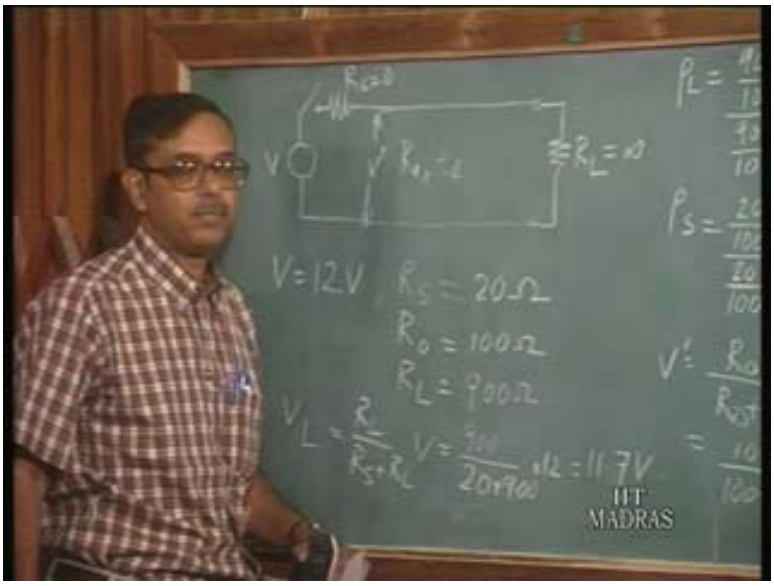

Then if we have an incident waveform V, what we will observe is at the load end the output waveform is going to be something like this.

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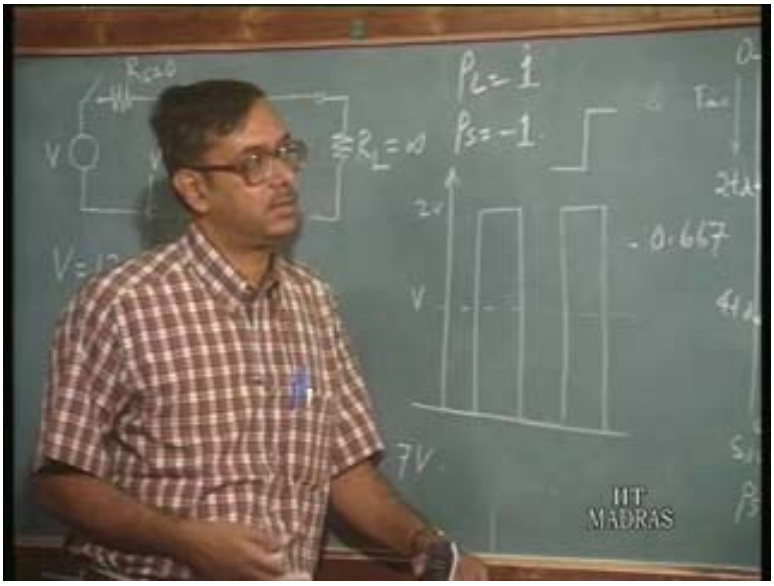

That is this is V, this is 2 V. Basically you have oscillation of this amplitude 2 v and this is never going to die down, this is going to continue indefinitely. We find that because this extreme case of one side being open circuit and the other side being short circuit, you have a situation where there are oscillations and this is never going to die down. The important thing is at the source signal is actually something like this and due to that you are having something like this. now in the actual circuit if this is going to drive a clock of a flip flop, what do we expect is that for example the clock of a shift

registers say, you expect in the register there is going to be one single shift but what you get is a number of waveforms and the shift register will see a number of clock pulses at the input.

So that there is going to be multiple shift, so what we have designed in the circuit is going to go ever and you are going to get something which is totally unexpected and you would not know what is happening but of course this is the extreme case. That is rho_L is one and rho_S is equal to minus 1. In other cases as we know that the magnitude of rho is less than one which means that with reflections, the reflected wave is going to ultimately die down because the rho is less than one. The amplitude of the reflected waves ultimately die down but of course over a period of time you get a lot of delays as well as a lot of distortion as you see here. We have seen that if you have a line which is short circuited at the source end and open circuited at the load end and if you have a wave form like this voltage v at the source end.

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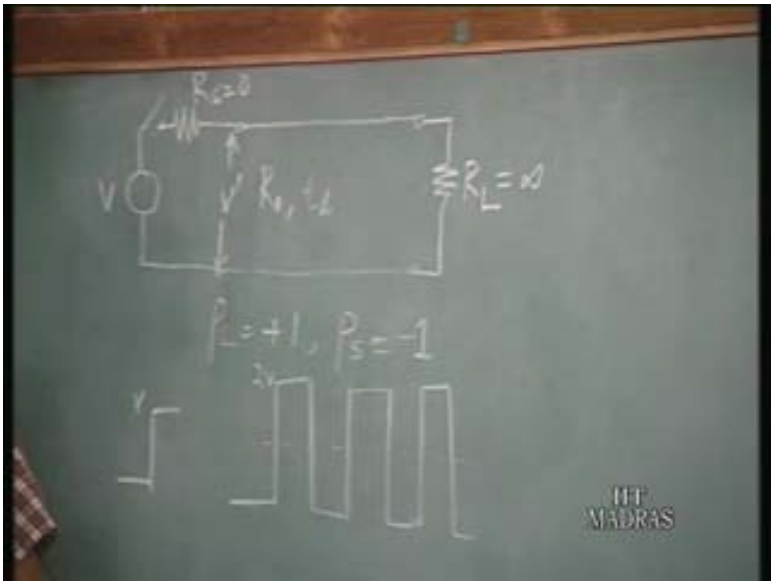

That is when we close this switch here, we get a waveform as step input at the source end of the line. The output is going to be something like this oscillations and which are not going to die down of amplitude twice V. This is of course going to be a very bad situation and of course this is the extreme case that is one end short circuit and the other end open circuit.

Now let us take an another case similar case where again the load is open circuit and the source is short circuit but the input waveform that is the input waveform V is not a step input but it is actually a ramp input like this.

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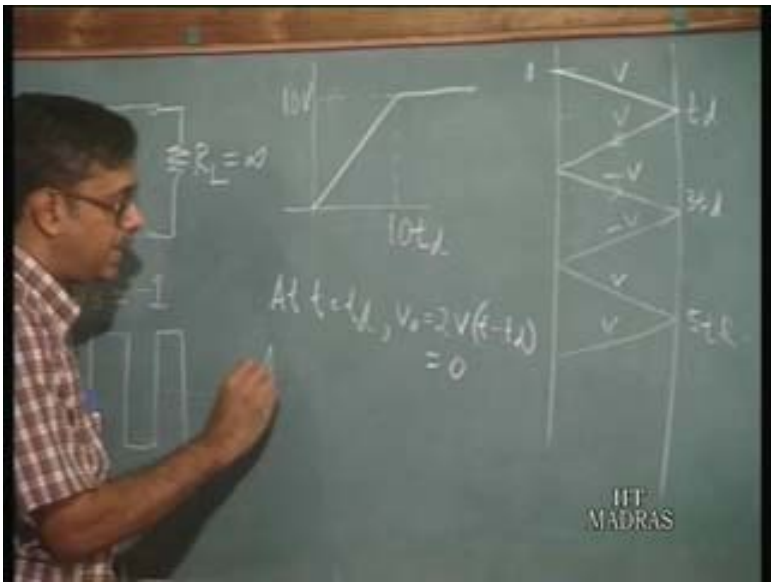

That is it takes time 10 t_d to rise to 10 volts that is the waveform rises to 10 volts at time 10 t_d that means for every t_d it rises by 1 volt. Now if we have such a waveform and if we still have the same conditions that at the load end, it is open circuit and at the source end it is short circuit. What is the output waveform let us look at it. In that case again if we take the same diagram what we have is at time t_d at t = t_d what we have is the output voltage is equal to... (Refer Slide Time: 40:04). Of course let us draw this diagram. Then this is zero, if you have a voltage V here this is plus 1, rho_L is plus 1 so this will have V. This one that is rho_S is minus 1 so this one will be minus V, this one will be again minus V. This one will be plus V, this one will be plus V, so this is t_d, 3 t_d, 5 t_d. At t is equal to t_d, you have twice the voltage which started off at time t_d before.

You have twice V (t – td) that is the voltage at time t - t_d. At voltage at time t minus td is a voltage at time t is equal to zero, for this ram this is equal to zero. The voltage is equal to zero. Now at t is equal to 3 t_d, voltage output will be equal to, at this point it is going to be twice the voltage which started off at time t_d before from the source end and minus twice the voltage it started off at time 3 t_d before that is from the source end.

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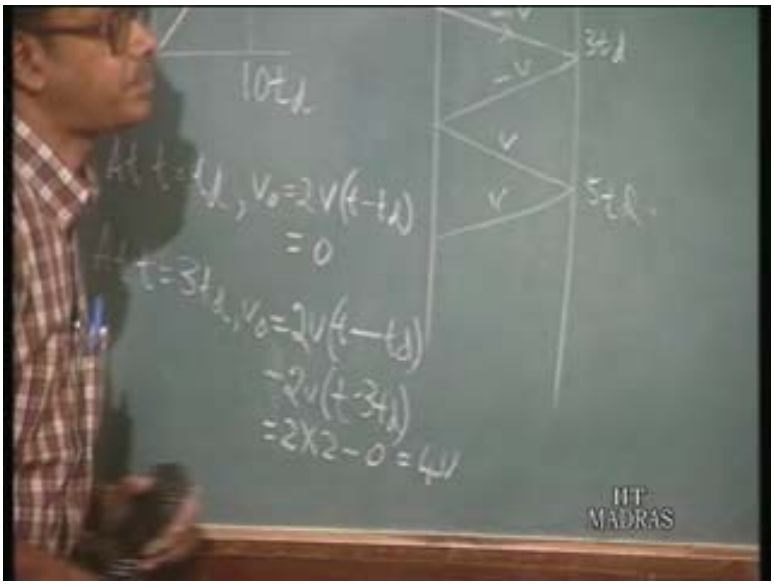

We can write V_{output} is equal to twice voltage t - t_d minus twice the voltage t - 3 t_d. The t minus t_d, now it is 3 t_d. So what was the voltage at t equal to twice t_d. From the ram we can see that at t is equal to twice t_d, the voltage is 2 volts so we can write is equal to 2 into 2 minus t minus 3 t_d is t is equal to 3 t_d is zero. So this is zero, so you have 4 volts. The output voltage I will write here, at t is equal to t_d, it is zero. This is t_d, it is zero at t is equal to 3 t_d it goes up to 4 volts.

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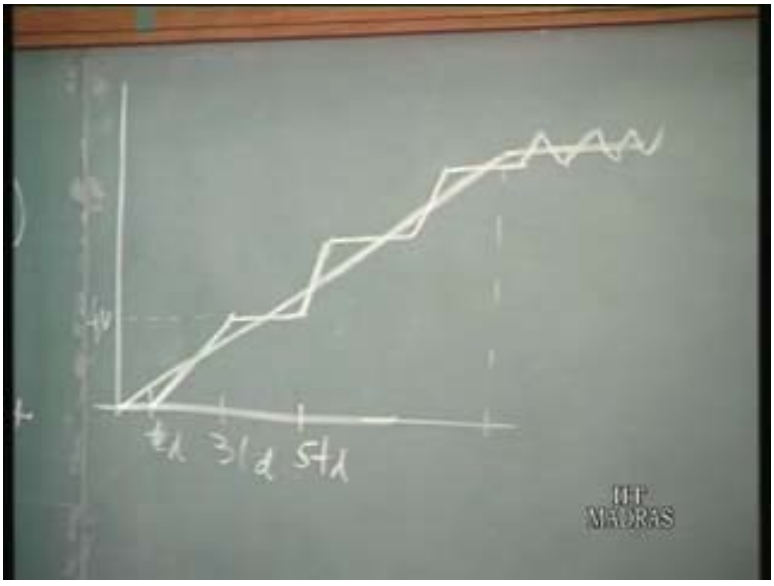

Let us suppose this is the ram which we are talking of. Now that is the input ram, so the output this is 4 volts at t is equal to 3 t_d.

Now at t is equal to 5 t_d what happens is you have again V_{output} will be equal to… Again if you look at this point is going to be twice the voltage which started off t_d before, minus twice the voltage which started off 3 t_d before and twice the voltage which started of 5 t_d before.

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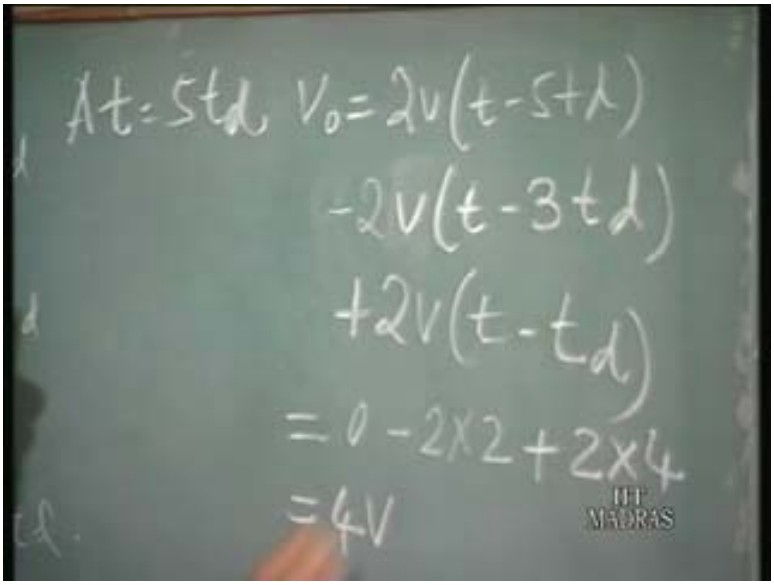

So twice v (t minus 5 t_d) minus twice v (t minus 3 t_d) plus twice v (t minus t_d). This is going to be equal to 4 volts. At 5 t_d it still remains at 4 volts. If you continue this analysis we will find that what you get is the output which is going to go like this. So this becomes like this, it is going to go like this. We have the input ramp here straight line and this is the output which goes like this. What we see is that the output almost very closely follows the input in this case. Although this is the situation where the output is open circuit and the input side is short circuit. This is the same situation if you have the unit step, we have seen how serious problems we have.

The conclusion is that if the input waveform is slowly varying then the transmission line effects are going to be minimal. the distortions due to the transmission line is going to be very small. So only when the rise time of the input waveform is very small compared to the delay of the transmission line, the transmission line effects become more dominant. This is again I just repeat that only when the rise time of the input waveform becomes small compared to the delay of the line then only the transmission line effects become dominant. In fact it is rule of thumb to say that the transmission line effects become dominant when the delay time of the line that is t_d is going to be more than the rise time by 5.

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In other words we can also say when the rise time is less than 5 times the delay time of the line then one has to actually look into the transmission line effects. This is the rule of thumb which is used to demarket, when the transmission line effects are dominant or when we can neglect transmission line effects. Now if you look at the different rise times for example if you have a rise time of say in picoseconds say if you have 1000 picoseconds that is one nanosecond of rise time.

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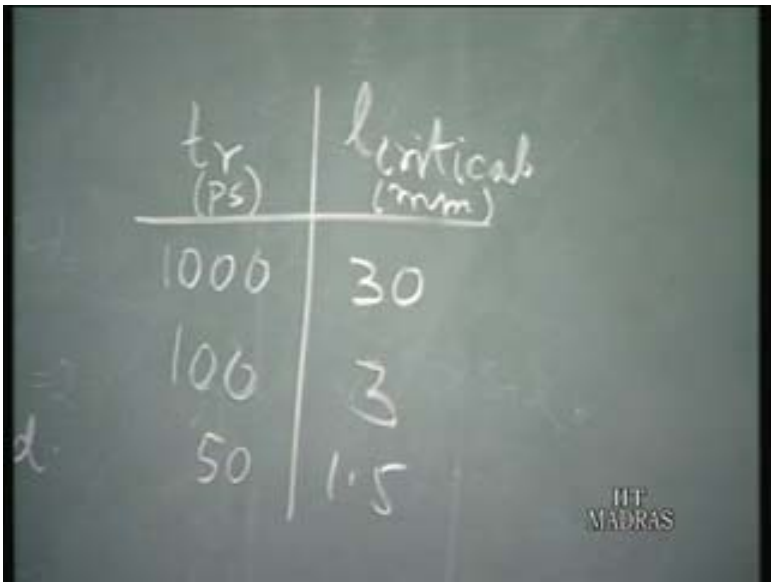

Then what is the critical length of a line when you have to start thinking of the transmission line effects that is what we have to consider.
Now suppose if we assume a velocity, as we have done of the wave in the line as 15.2 centimeter per nanosecond. This is the velocity of the waveform in the line that is we have already seen this value for silicon dioxide dielectric. Now for this the critical length of the line $l_{critical}$ is given by, it is going to be in 30 millimeters that is if the rise time is 1000 picoseconds then if the critical length of the line is less than 30 millimeter. If the line length, the interconnection length is less than 30 millimeter then we have to consider the transmission line effects. Now if it goes down to 100 picoseconds then this will also go down to 3 millimeters.

That is if the rise time is 100 picoseconds then the critical length of the line is 3 millimeter that means for this if the line length goes down below 3 millimeter we have to be careful. Similarly you know it scales linearly, if you go down to 50, this one will be 1.5. Now these values 100 picoseconds and all these are so uncommon values nowadays, we have the rise time and the fall time of this order. This 3 millimeter especially say for example 3 millimeter if you have something on a pcb of course we have to be very careful. We must consider the transmission line effects even if you go to very high speed circuits we may even have to consider transmission line effects on the chip.

These are some of the delays. Now what we have to look for now is that there are different models which can be used to analyze the circuit when we go to such small dimensions of lines or small rise time and fall time. Now which is the correct model to take to simulate the line, simulate the effects of the transmission line? So that is what we shall take up next.

Part – 2

Now we shall look at the different model which are used to represent the transmission lines and the particular models which must be for the particular situation which is the best model to use in order to simulate the transmission line.

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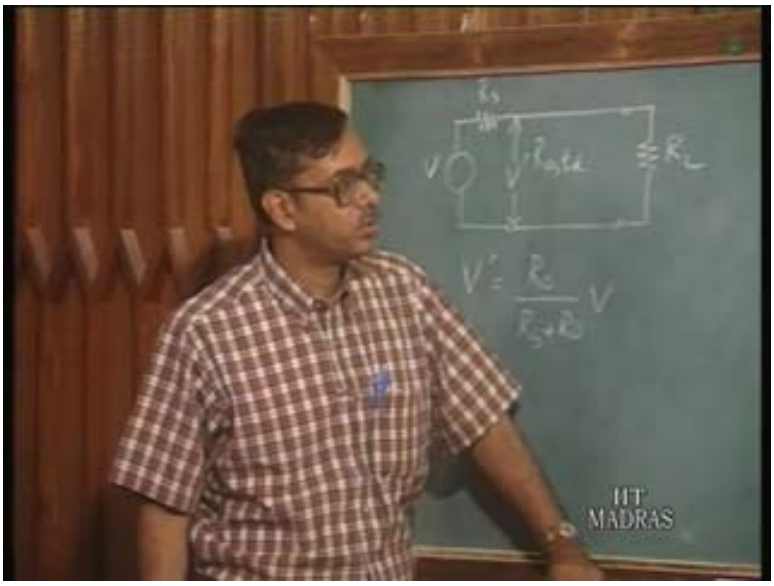

Now suppose we replace the transmission line by just equivalent capacitance say C and of course you have the source resistance from the voltage source.

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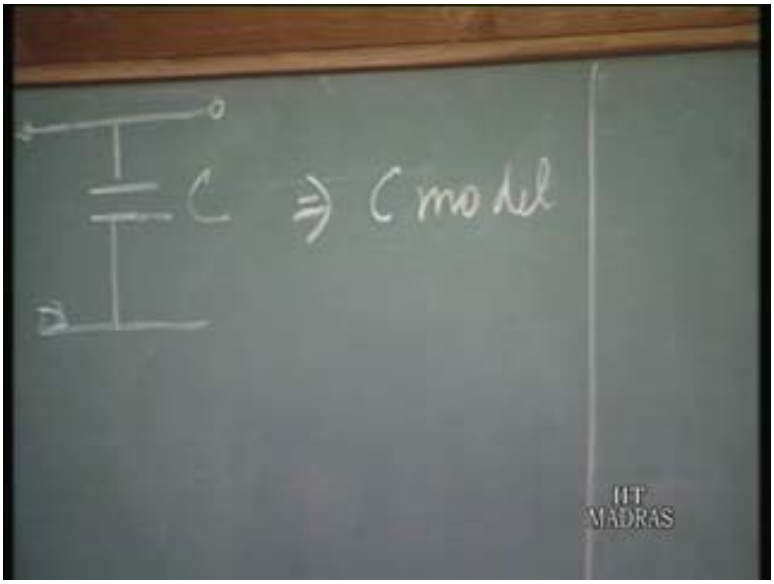

If you have just this model which is called the C model and if you consider open circuited line at the load end then we know that the output voltage $V_{0.}$ is equal to V (1- e to the power minus t by $R_{S.}$ that is the source resistance into C prime.

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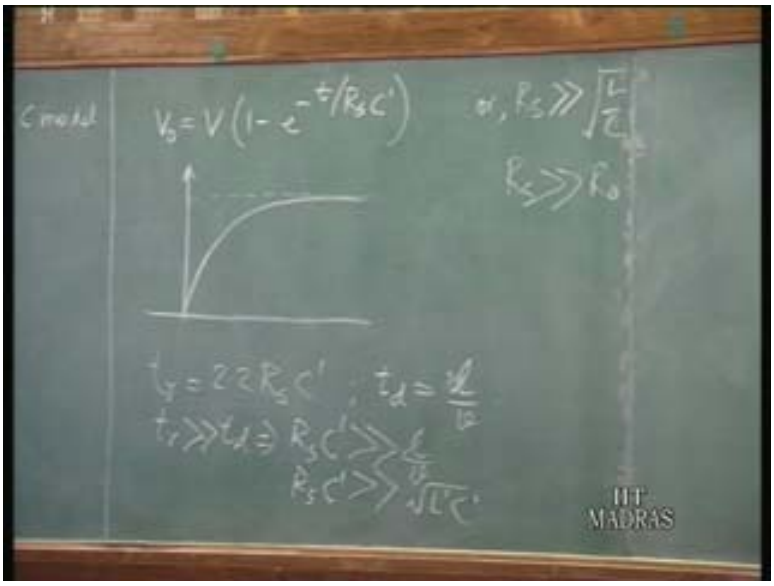

The C prime which is actually the total capacitance of the line. We actually replace the line by only its total capacitance that is the C model. The output voltage will be given something like this. That is when you have a step input, the output voltage will rise like this and finally reach this value and in this situation, the rise time is given by 2.2 R_s C prime. This is the situation if we have only a lumped capacitance to replace the transmission line. In this case the rise time is given by R_s into C prime whereas the delay of line is given by L by V. Now if we have a situation where the rise time, we have already said that the transmission line effects becomes minimal when the rise time is very much greater than the delay line.

So t_r very much greater than t_d would imply that R_s C prime is very much greater than L by V. The L by V is nothing but V is we have already seen is equal to L by V or is equal to t_d and which we have already seen is equal to related to the inductance and capacitance of the line and or in other words R_s C prime is very much greater than root L prime C prime. Now the L prime is the length of the line into L and C prime is the length of the line into C so we can write this as or R_s is very much greater than root of L by C and root of L by C we know is equal to R_0.

So R_s is very much greater than R_0. We can say that when R_s is very much greater than R_0, that is the source resistance is very much greater than the characteristic impedance of line, the rise time of the waveform is going to be very much greater than the delay line and then what happens is we need not consider the transmission line effects. The transmission line effects become minimal. In fact the line can be replaced by the capacitance of the line, just the capacitance of the line. This is because if we go back to our earlier model in the analysis how we have analyzed.

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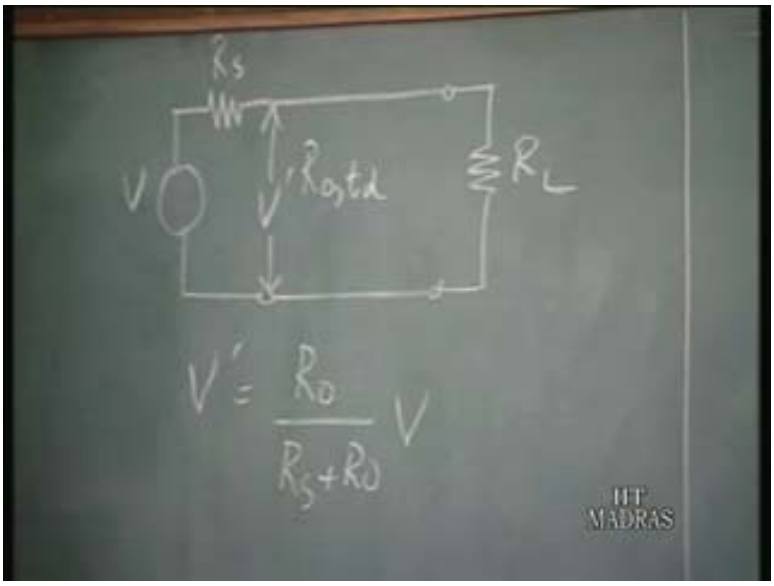

What we have seen is that if you have a transmission line, we get the same results using transmission line that is if you have a transmission line the input voltage to the transmission line is given by V prime which is equal to R_0 divided by R_s by R_0 into V. Now if R_0 is very much less than R_s that is the source resistance very much greater than characteristics resistance, V prime is going to be very much less than V. The input voltage at the source end of the transmission line is very much less than V so if the output voltage has to rise to V, it can only be through small increments, when the multiple reflections take place. If you do a transmission line analysis here so you have V prime coming here and then it will go up so you are going to have a situation like this.

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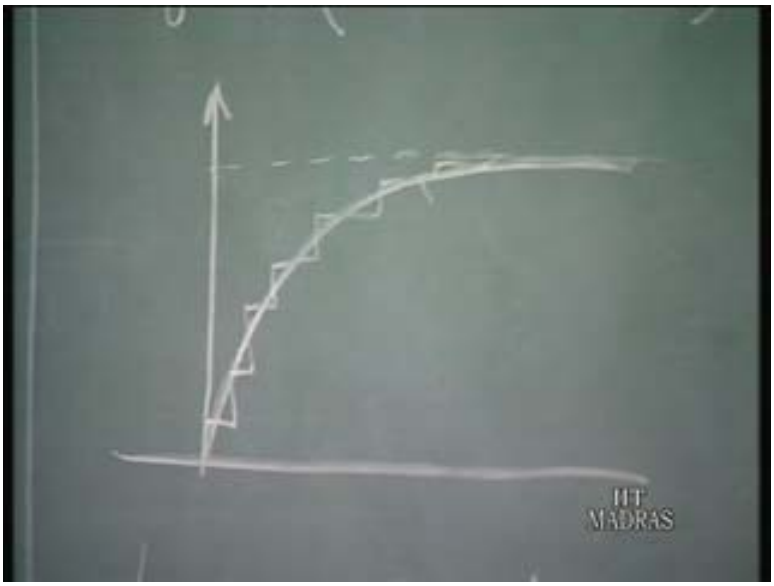

Transmission analysis will give you something like this whereas if you just replace the line by a lumped capacitance you get something like this. So this C model which we have here that is replacing the line by the capacitance is valid when you have R_S very much greater than R_0 that is the source resistance is very much greater than R_0. Now in this case of course we can neglect the actual resistance of the line because the source resistance is so high, it plays a dominant role. This is valid when R_S is very much greater than R_0. Now when R_S lies between 10 times R_0 and R_0 then we cannot really neglect the resistance of the line also.

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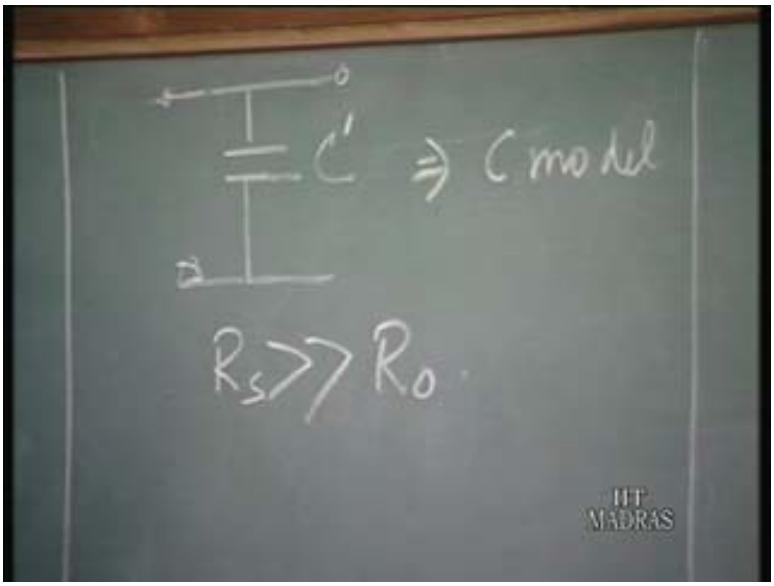

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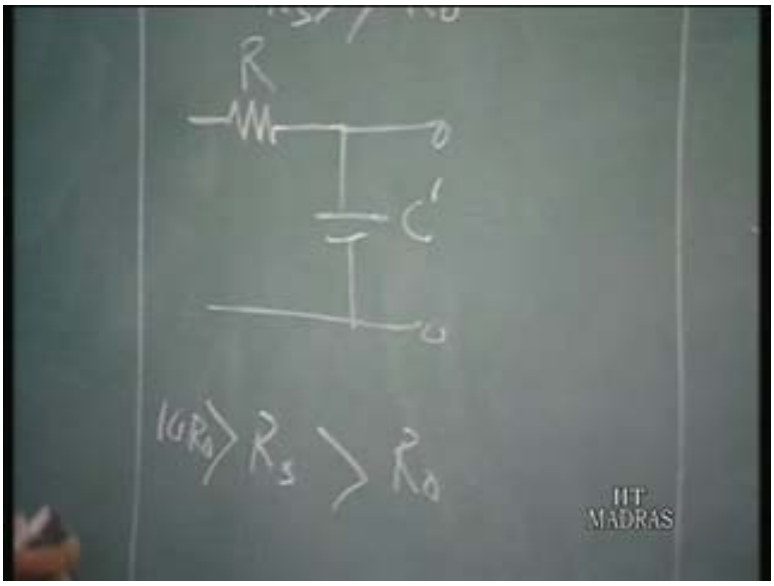

Then we have a model and what we can do is we can use the resistance of the line, the line can be replaced by resistance and capacitance R_C. This is called the l model because of the shape of the model. This is the resistance of the line, this is the total capacitance of the line but this type of model does not give very correct results because we know that the resistances and capacitances are distributed but this is using as a lumped values. What is done is a three section pi model is generally used which is given like this. You have C by 6, R by 3. The line can be replaced by what is called a three section pi model where you have these capacitances here.

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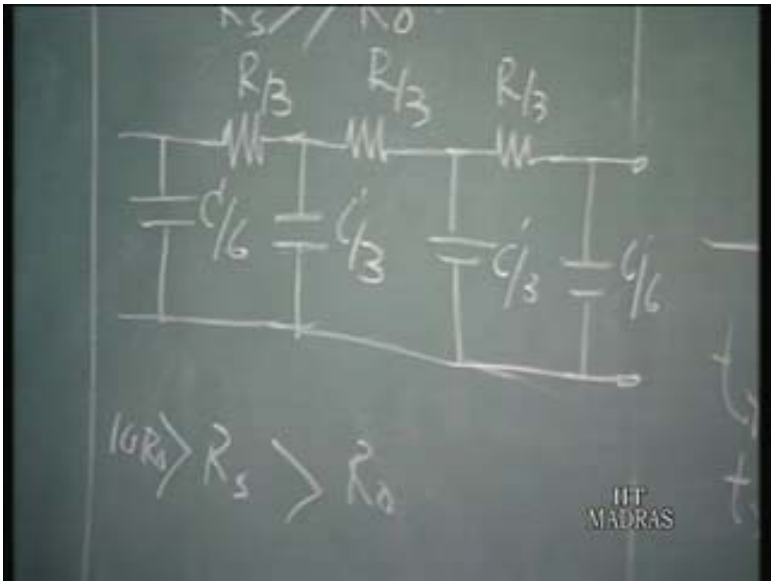

These are resistances of the line. Basically we do not have a single resistance and capacitance but this is distributed and we find that this gives the more accurate delay values for the line. In fact if we take the lumped value that is only one resistance and one capacitance then it is going to something like this is for lumped.

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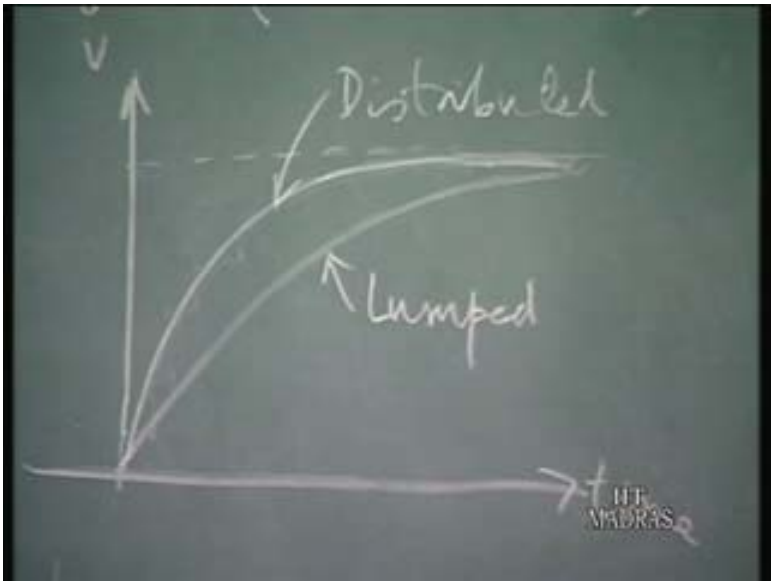

If you take a distributed value it goes like this. This is voltage versus time, so this is distributed. This gives the more accurate representation and the lumped representation gives a higher delays than what is to be expected normally.
This is called the three section pi model or the $p_{3.}$ model and this can be used for this situation. When the source resistance becomes less than the characteristic resistance, we have to go for transmission line analysis. In fact we must remember that the transmission line analysis is always correct. It always gives the best results but only that in many cases it may not be necessary to go into the transmission line analysis. We can use these simple models to get results which is similar to the transmission line results and with much less computation time so that is the advantage. So just briefly to conclude I had given a table showing the different models and when to use the particular model. For example if we take a look at this table, now suppose this shows the values of $R_{S.}$ by $R_{0.}$, this is the values of $R_{S.}$ by $R_{0.}$.

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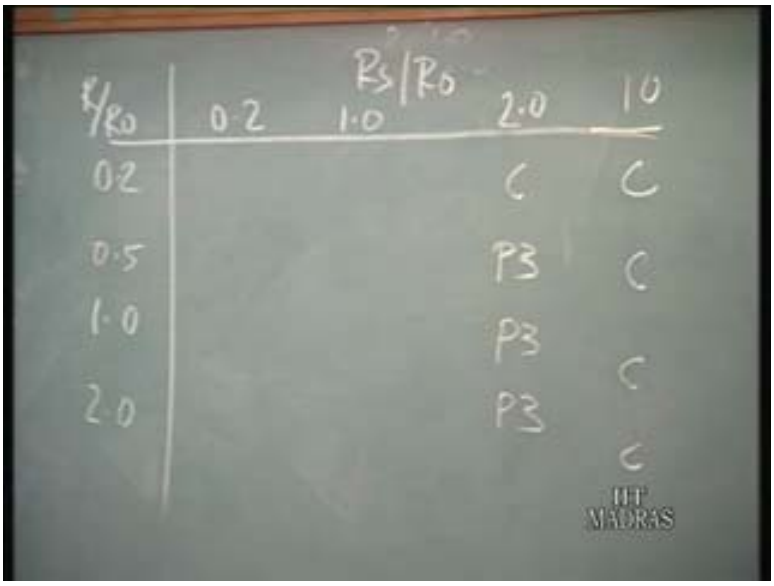

Suppose $R_{s.}$ by $R_{0.}$ is equal to 10 then we have to take the capacitance model. So this is 10, let us take some values 2, 1 and then 0.2. These are for different values of $R_{s.}$ by $R_{0.}$, here I am showing different values of R by $R_{0.}$. That is the actual resistance of the line when compared to $R_{0.}$, 0.2, 0.5, 1 and 2. Now here of course this means that R is very much less than $R_{0.}$. So in fact when you go for this situation here that is $R_{s.}$ by $R_{0.}$ is equal to two, you should actually take the C model but we should actually take the $p_{3.}$ model but since R is very small here we can take the c model.

That is we in fact neglect the resistance of the line. In all this situations when $R_{s.}$ is very much greater than $R_{0.}$, we can take only the capacitance of the line but when $R_{s.}$ becomes comparable to $R_{0.}$, you must take the $p_{3.}$ model that is the three section pi model. When $R_{s.}$ and $R_{0.}$ become comparable and when $R_{s.}$ becomes less than $R_{0.}$, one has to go for transmission line analysis. For transmission line also we have two models, one is the normal one section transmission line which we have already seen but when the resistance of the line becomes comparable that is it is a lossy transmission line, we have to go for what is called a four section transmission line model.

That is basically we have structure like this. This is a four section transmission line model, so these are all transmission line, this is a characteristic impedance $R_{0.}$ and delay $t_{d.}$ by 4, $R_{0.}$ $t_{d.}$ by 4, $R_{0.}$ $t_{d.}$ by 4, $R_{0.}$ $t_{d.}$ by 4. This is R by 3, R by 3, R by 3 so together these three make up which is equal to R, the total resistance of the line.

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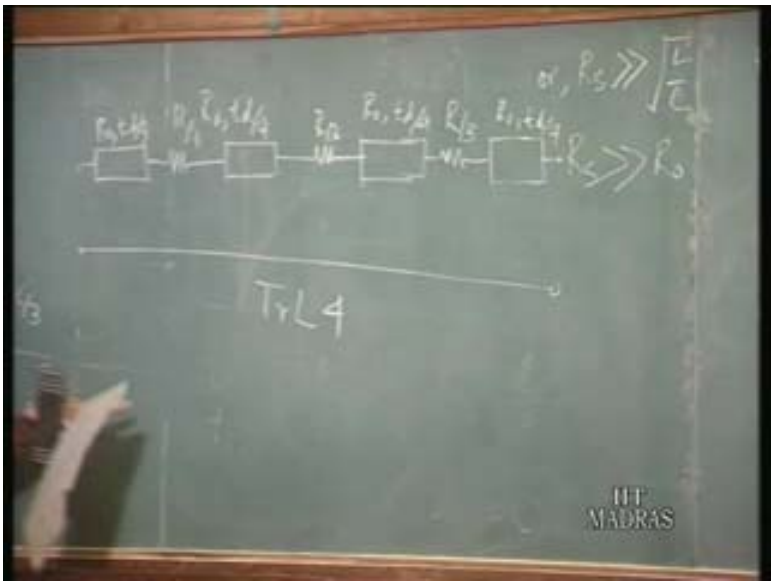

You have a four section transmission line model, this is called trl transmission line four model. Now if you have one transmission line section that will be the trl one model. When the resistance of the line is small, you can take the one section transmission line model but if the resistance of line becomes large, we have to go for the four section transmission line model which includes the effect of the resistance of the line that is basically considers lossy transmission line.

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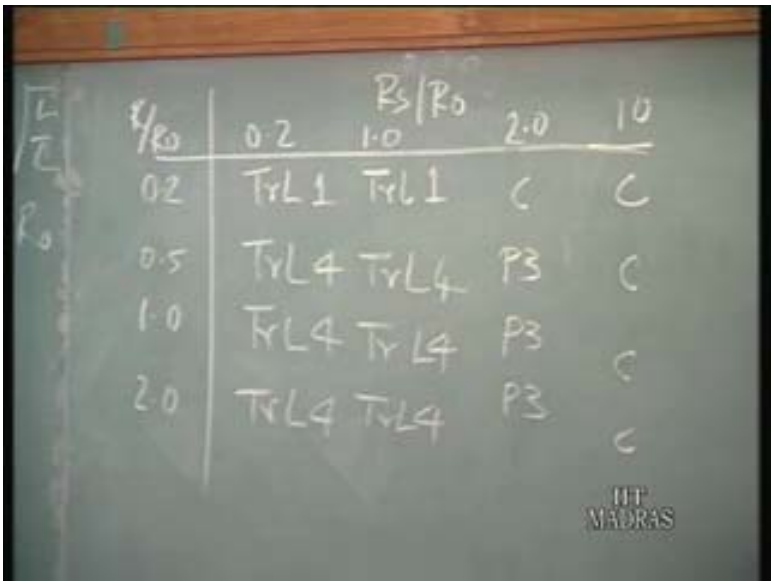

This table gives the different models which can be used for different situations. Again I would like to reiterate that the transmission line model is always the most accurate but it takes more amount of time to do analysis. When we have particular situation when it is possible to get the same results using just a lumped capacitance, it would be a waste of time to go for transmission line. This capacitance model would suffice. When we do an analysis we have to look at the particular situation and see which model would give us the best results in the shortest amount of time, simulation time.

This table we can do the simulation in the shortest possible time. For example we can just take a capacitance model in some situation and get the same result as the transmission line model and in a much shorter smaller amount of time. That is we should always go for that. So with that we come to the end of this discussion on this effect of interconnections and we have seen that interconnections give rise to lot of delays and as well as distortions. We must be aware of that, we must use the correct model to simulate the circuit. That is include the interconnection model which are available in circuit simulators such as spy's and then simulate the circuit to get the best results. Otherwise when we fabricate a circuit you may get results which are totally unexpected and we would run into problems. Interconnections play an important role also in digital circuits and that must be emphasized especially when the rise times become small that is in modern day high speed digital circuits.

Thank you.