Digital Integrated Circuits
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Lecture -39

Buffered FET logic; Schottky diode FET logic

In the last class we had started our discussion on MESFET based logic circuits and we had discussed two logic families that is the direct coupled FET logic and the super buffer FET logic both of which use a combination of enhancement and depletion mode transistors. Now it is sometimes difficult to fabricate both enhancement mode and depletion mode transistors in the same wafer, I mean you require a more complicated technology for that and also enhancement mode devices are more difficult to fabricate. It requires a higher degree of accuracy in all the technological processes. There are other logic circuits which use only depletion mode transistors and they are technologically more easier to fabricate and that is why they are quite popular also. In today's class we shall take up two such logic families which use only depletion mode transistors. We shall start with the inverter and in this case since we are only using depletion mode transistors we have two depletion mode MESFET's.

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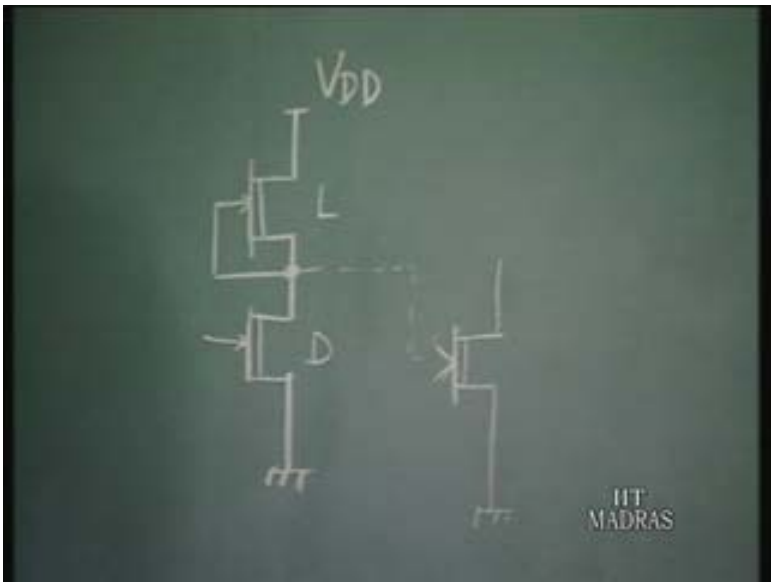

This is the driver transistor and this is the load transistor and for the load transistor, the gate to source is shorted and so V_{GS} is equal to zero and by adjusting the V_{DD} we can again ensure that the load transistor is always in the saturation region. Now this circuit has a certain problem. Suppose this has to drive another similar inverter.

Now if you are driving a similar inverter what is going to happen is since this voltage here at the output of this gate is always going to be positive because there is no way this voltage can go negative. The input voltage to the next stage inverter is always going to be positive. Since this is the depletion mode device, in order to turn this transistor off we require to have negative voltage at the input. This output voltage since it does not go to negative values, it is unable to turn off the input transistor of the next stage so that is the problem. How do you solve the problem? The way to solve the problem is to use a level shifting arrangement. To do that we use two diodes which are used as level shifters and we have what is called a pull down transistor which is again a depletion mode device with the gate to source shorted. Here we have a negative supply voltage minus V_{SS}.

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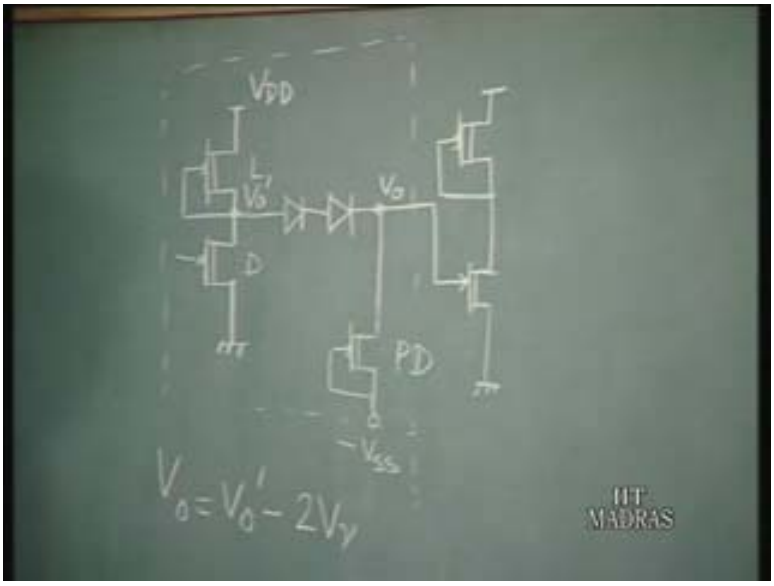

A current will always flow through this pull down device. What is going to happen because of this drop across the diodes, so this voltage here is going to be level shifted by two diode drops. If we call this output voltage $V_{O.}$ prime say, this actual output voltage here is going to be $V_{O.}$ and $V_{O.}$ is always going to be $V_{O.}$ prime minus twice we can call it $v_{gamma.}$ where $v_{gamma.}$ is actually the cut in voltage of the diodes. There is going to be a level shift between these two devices.

Suppose this voltage can be positive but the $v_{output.}$ can now go negative. Now this output voltage is going to be fed as input to the next inverter here. This is the input stage of the next inverter. The basic circuit for this logic family is going to be this where we have an inverter followed by a level shifter. How to find out the input output characteristic of this inverter? Again we follow the same procedure that is we can do it graphically by drawing the output characteristics of the driver device. We draw $I_{D.}$ $V_{DS.}$

for the driver device and then what we have to do is to draw the load line as usual to find out the input output characteristic.

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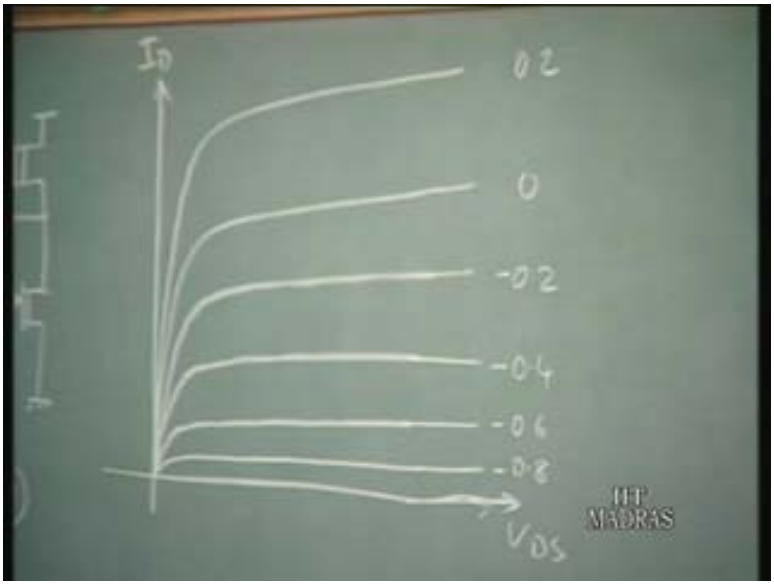

Now let this be the characteristics of the driver transistor. Before we go ahead let us now fix certain values for this device. Now let us put V_{DD} is equal to 3 volts, let minus V_{SS} is equal to minus 2 volts. You have a plus 3 volt power supply, you have a minus 2 volt power supply. All these are circuits using only depletion mode devices which must have a dual power supply that is a positive power supply and a negative power supply. You have V_{DD} minus V_{SS}. Now as we have already said that the channel length of each transistor is always maintained at the minimum value. We have the driver transistor length is equal to length of the load transistor and is equal to the length of the pull down transistor.

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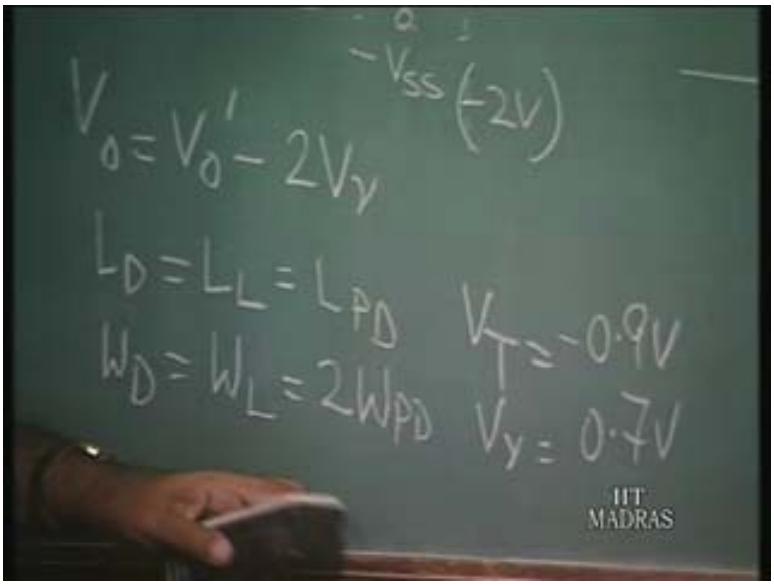

But the width of the transistors will be adjusted. Now suppose we have the width of the driver transistor is equal to the width of the load transistor is equal to twice the width of the pull down transistor which means that the pull down transistor has half the width of the driver and load transistor. In all other respects all these depletion mode transistors in the circuit are identical except the widths of the transistors. Now let the threshold voltage of these transistors be minus 0.9 volts and let V_{gamma} that is the cut in voltage be 0.7 volts. Now in this characteristics since the threshold voltage is minus 0.9, we can put minus 0.8, minus 0.6, say minus 0.4 minus, 0.2, 0, plus 2 like that. These are the gate to source voltages for which these are the characteristics.

Now how do we draw the load line for this structure? Normally we draw the characteristics of the load device starting from V_{DD} here and inverting it along the x axis but here the small difference is that you see because of this pull down structure or level shifting structure, a current is constantly going to flow through these devices. For this we have the load current, the current of the load transistor is equal to the current of the driver transistor plus the pull down current.

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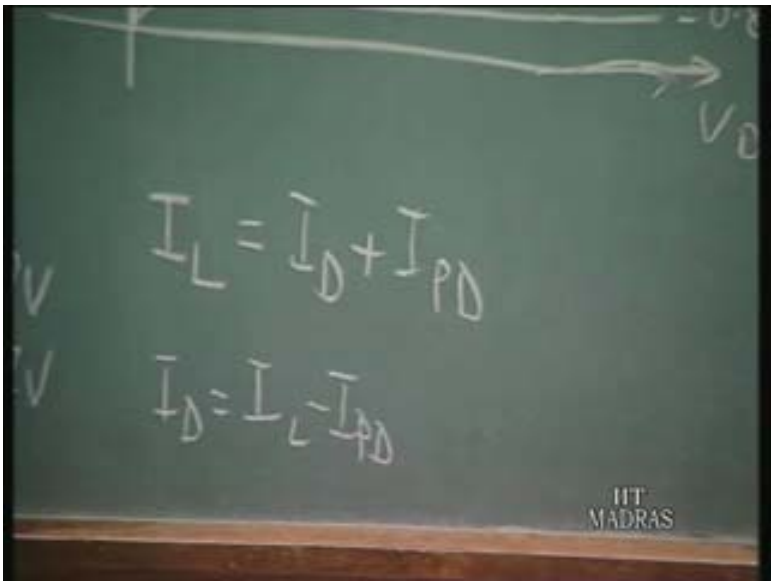

The load current is equal to driver current plus the pull down current which means effectively that I_D is equal to I_L - I_{PD}. I_D is equal to I_L - I_{PD} that is the driver current is equal to load current minus the pull down current which means that the driver current is not equal to the pull down current and this must be taken into account while drawing the load. Now suppose let us take that this is equal to 1 milli ampere.

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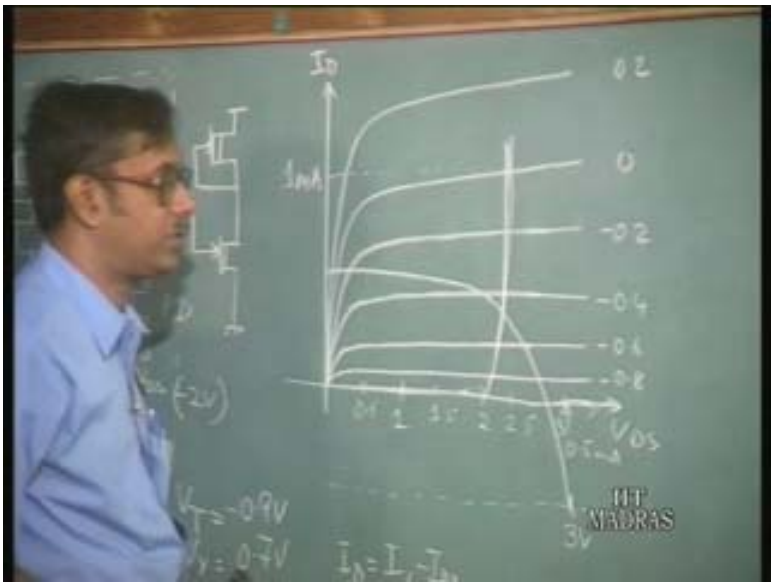

That is when V_{GS} is equal to zero, the current flowing through the device is approximately 1 milli ampere and for the pull down device everything is identical except the width of the device is half. For the pull down device when the gate to source voltage is 0, the current flowing through it would be half of this current that is you have half a milli ampere, 0.5 milli ampere would be the pull down current. If you now look at this expression so I_D will be I_L minus the pull down current which is 0.5 milli ampere. To draw the characteristics what we have to do is we have to shift it down by 0.5 milli ampere. If this is say 0.5 milli ampere now we have to take the V_{DD}, this is say 3 volts and draw the characteristics from here.

This is the origin and so the load characteristics would be something like this. This is the characteristics of the load device, this is shifted down by 0.5 milli ampere which is the current flowing through the pull down device. Now the intersection of this set of characteristics for the driver device and this characteristic for the load device is going to give us the operating point. There is another constraint here that since the input voltage here cannot rise above 0.7 volts that is the output voltage of this inverter here cannot rise above 0.7 volt because it is going to be clamped by the input schottky diode of this depletion mode MESFET. The maximum value is 0.7 volts, here the maximum value of the output volt is going to be 2.1 volts because of the two further diode drops. We also draw the characteristics of the diode here. If this is 2 volts, this can be 1 volt, this is 3 volts, so 1.5, 0.5 say this is 2.5 and so on. This is the characteristics of the three diodes together so the output voltage cannot exceed this value. The output voltage is always going to be limited by this value here. After having drawn this, we can now find out the input output characteristics.

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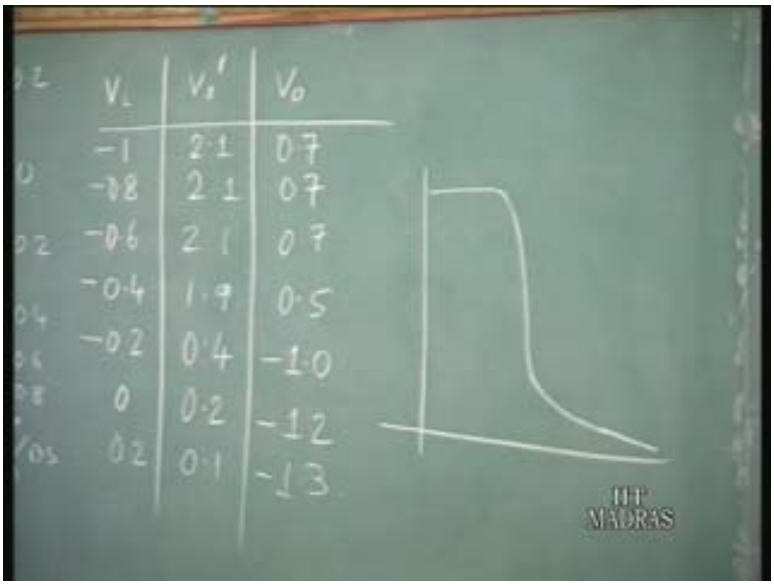

Let us put $V_{o.}$ prime is the output voltage at this point here that is of this two transistor section that is before the level shifter and $V_{o.}$ is the actual output voltage which is shifted by 1.4 volts. Now if $V_{i.}$ is less than the threshold voltage of the input of the transistor here say it is say minus 1 volt, so this current is 0. Now the point of intersection is here but since the output voltage cannot exceed this, $V_{o.}$ prime is going to be 2.1 volts, 3 diode drops and this one is going to be 1.4 volts less.

Now if you take minus 0.8 volts, it is still the point of intersection is here which is beyond this point so again we take it as 2.1 volts which is 0.7 volts here. If it is minus 0.6 again the point of intersection is going to be here which is beyond this curve. Again if it is minus 0.6, it will be 2.1 and 0.7. Now if we go to minus 0.4 let us see. This is minus 0.4 curve, the point of intersection is here which is on this side of this curve. The output voltage is going to be almost equal to 2 volts say 1.9 volts, if it is 1.9 volts so the output voltage actually falls to 0.5 volts here. Again if we take the next curve that is minus 0.2 volts, we find that the output voltage has dropped significantly.

The point of intersection is now here (Refer Slide Time: 14:37) so which may be for minus 0.2 volts, this is going to be around 0.4 volts so this output voltage is now going to be minus 1 volt. Now if we go on increasing this voltage say zero, the point moves to this, so you have 0.2, minus 1.2 and so on. If you go to plus 2, it may be 0.1 and minus 1.3 and so on. What we find is that from this characteristics here that as the input voltage is increasing from minus 1 volt to 0.2 volts, the output voltage initially is at 0.7 volts which means that it is going to turn on the output driver transistor and then it starts falling and then when the input voltage exceeds 0 volts, the output voltage falls below minus 0.9 volts which is the threshold voltage of the input transistor, so it is going to turn off the next driver transistor of the next stage.

Basically you have a characteristics which is flat initially then it falls and then keeps falling. The important point here is the output voltage goes below threshold voltage of the output transistor and so it cuts off the output transistor. Again when the input voltage is minus 1 volt, for the next stage output voltage is going to be high. We see that this structure is going to behave as a good inverter. We have seen the inverter structure for this particular logic and seen that the input output characteristic behaves as an inverter. If we want to make a NOR gate from this inverter, thus we follow the usual procedure that is we have similar transistor in parallel with the driver transistor and so when any of these two inputs are high, the output at this point is going to be low which means that it follows the NOR configuration.

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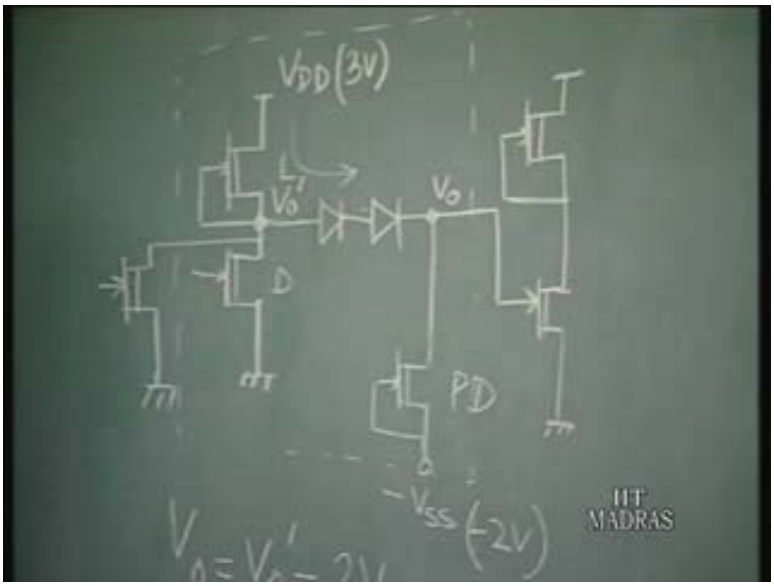

We see that this is okay from the static characteristics point of view and we have a NOR structure but this particular circuit has some problems. Now let us look at the problems. This problem is mainly during the switching period. Suppose both the inputs are low and then suddenly one input goes high then which means that the driver transistor turns on and the output voltage has to be pulled low. What happen is in this case when this turns on, this output goes high, the pull down action is taking place. This input here goes quite low this and the pull down is going to be taken place mostly by this pull down transistor.

On the other hand when we look at the pull up configuration that is when both these transistors go off then the pull up is taken care of by this load transistor. The load transistor must drive a current here in order to switch on the output or turn on the output transistor here, the next transistor. It is has to supply a large current but since the pull down transistor is always on, large part of current flows into the pull down transistor and there by the delay is quite high. Because you see that this load transistor,

the gate to source voltage is always zero volt. So irrespective of the conditions the load current does not change whereas for a driver transistor the gate to source voltage, so if the input voltage goes high to 0.7 volts there is a large current here.
During the switching period, it can provide a large current but in this case the load transistor because it's gate to source voltage is always zero volt so its current is limited and a part of this current is going to flow into the pull down transistor so the current available for turning on the output transistor is very small. In order to improve this circuit what is done is we have another configuration which is quite similar. This input part remains the same, this is a load transistor again with the gate to source shorted this is the inverter.

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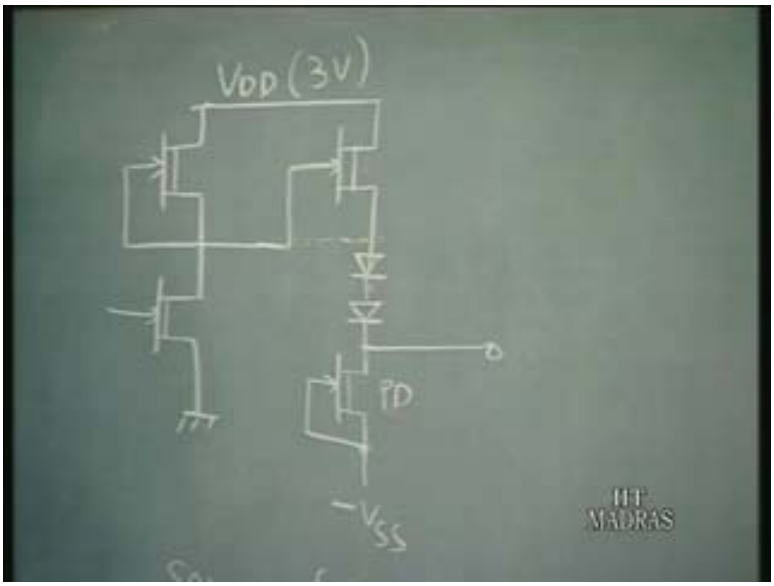

We have another transistor here so this output goes into the gate of this transistor then we have the two diodes which are used for level shifting and this is the pull down transistor whose gate to source is shorted and this goes to minus V_{SS} and the output is taken from this point (Refer Slide Time: 21:00). Now if you look at these two structures here, one is this structure here and then this structure here we find that if we short this two points, that is we don't have this transistor then we get back the original structure. Basically what we have done is we have introduced another transistor here.

Now this transistor is called a source follower transistor just like you have the emitter follower in a bipolar transistor, source follower and it can be designed such that the gate to source voltage of this transistor is always zero volts. How do you do that? This is the pull down transistor, always a constant current is flowing through it because this transistor is always in the saturation region and the gate to source voltage is zero. It is in the flat part of the characteristics so this transistor has a constant current. Now if we have an identical transistor here just like the pull down transistor then what happens is

this transistor since it is identical to this and the same current is flowing through this and this transistor is always in saturation. That is always true because if this is 0.7 volts here, this is the maximum value it can be 0.7 volts because it is limited by the input voltage of the next transistor.
This is 0.7, this is 2.1 and if the V_{DD} is 3 volts so you have always a minimum of 0.9 volts as the drain to source voltage of this transistor which ensures that this transistor goes to saturation, it is always in saturation. If the same current is flowing through these transistors and these are identical transistors and if the gate to source voltage is zero volts here, this will also be in the steady state. This will also have zero volts gate to source. That means the voltage at the gate and the source are the same. This circuit actually is going to have an identical characteristics of as the previous circuit.

We have a source follower that is whatever is the gate voltage, we have similar voltage at the source. From the output characteristics point of view these are identical but this circuit has a much better performance during the switching period. Now let us draw the input transistor of the next stage. Now let us see what is the difference. Suppose this is at 0.7 volts which means that the output is high.

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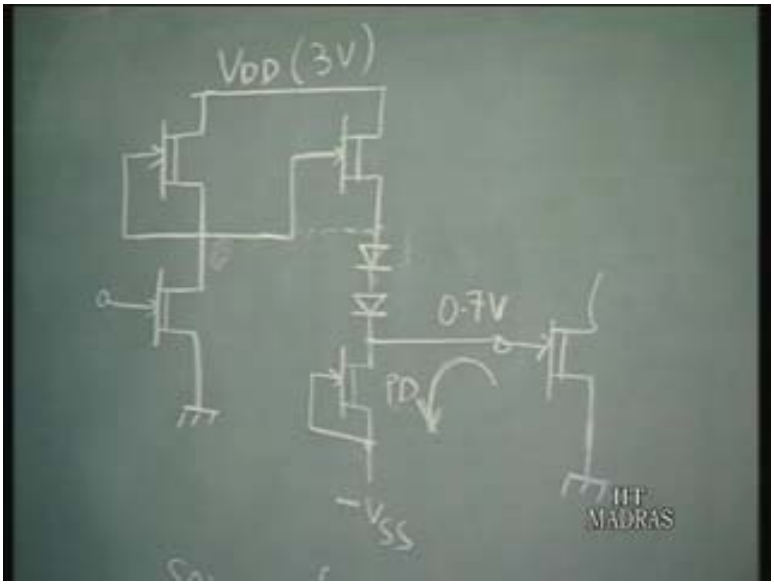

This input goes high at this point, that is the input of this gate it goes high that means the voltage here is pulled down to almost close to zero volts. Now if this is zero volts, this is 0.7 so this point will be around 2.1 volts, so this is close to zero volts. The gate to source voltage during this switching period, this is very large negative voltage which actually cuts out this source follower transistor and since this transistor is cut off there is no current flowing this way. So this pull down transistor is ofcourse on so a current flows in this way (Refer Slide Time: 24:46) flows comes out of the input of this output transistor and discharges the input capacitance of this output transistor and so the output

voltage is going to fall. Here there is no clash of currents so this pull down transistor is on, the source follower is off and the full current of the pull down is used to switch off this output transistor. On the other hand suppose this voltage is negative say minus 1 volt that is less than the threshold voltage so this transistor is off.

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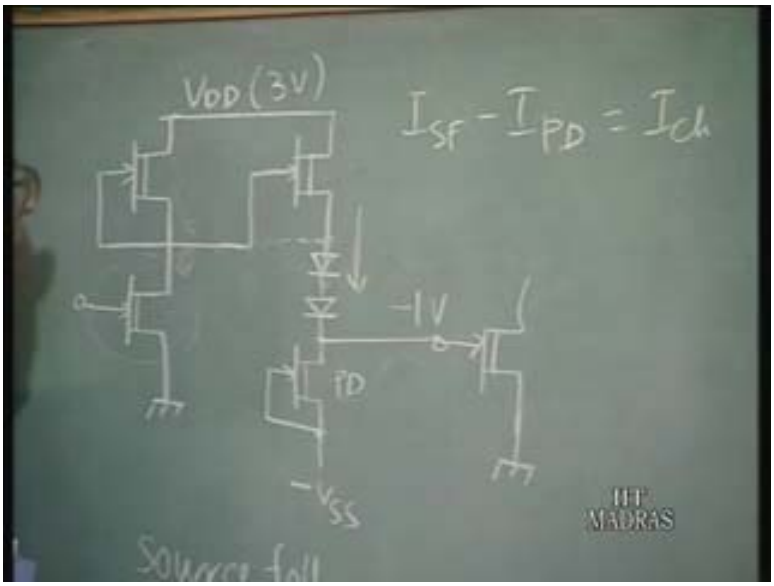

Suppose this also goes negative, so this transistor is cut off. The input transistor is cut off suddenly then what happens is this output voltage is going to close to the V_{DD}, it tries to approach V_{DD}. Since this is minus 1 volt so this will be plus 0.4 volts at the source of this source follower transistor, now this gate voltage can rise. It is not constrained as in the previous case to zero volts. This gate voltage can rise and you have 0.7 volts across gate to source in that switching period. There is a large current flowing here.

The source follower current is going to be very large because the V_{GS} is going to rise to 0.7 volts and this source follower current I_{SF} minus the $I_{pull\ down}$ which is also going to be substantial, this current is used to charge. The charging current is going to be the source follower current minus the pull down current is going to be charge whereas the discharging current is just a pull down current, the charging current of the output capacitance. In the charging case the source follower V_{GS} is 0.7 volts so basically I_{charge} will be equal to the source follower I_{SF} at V_{GS} is equal to 0.7 volts because it is going to rise to 0.7 volts.

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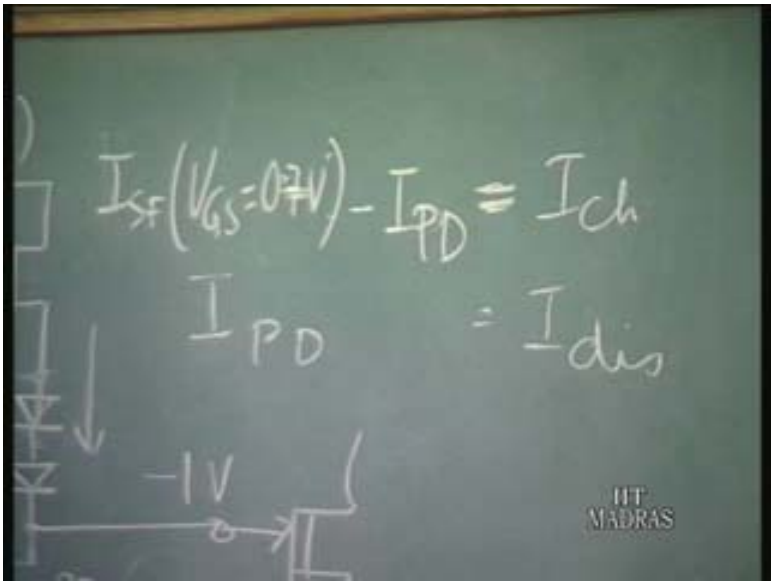

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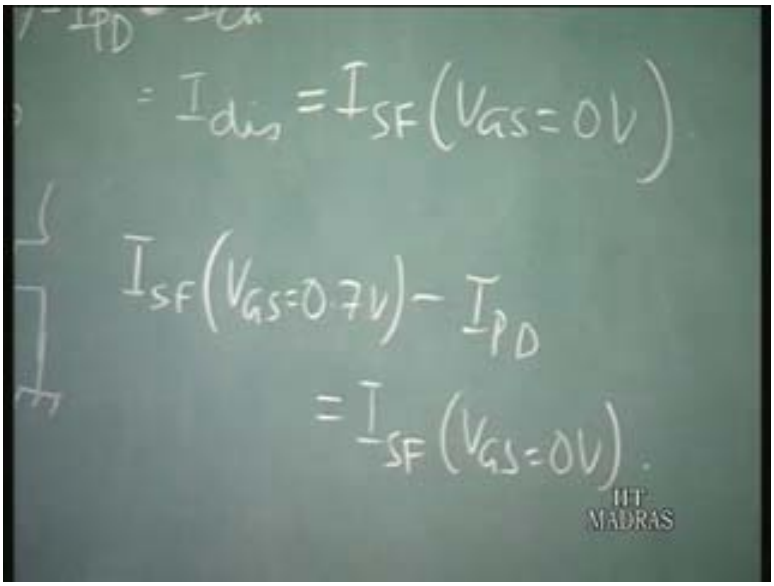

So 0.7 volts minus $I_{PD.}$ which remains a constant. Basically this $I_{PD.}$ is equal to $I_{source\ follower.}$ at $V_{GS.}$ is equal to zero volts that is how we have designed it. If we design in such a way we can now see that if we want $I_{charge.}$ is equal to $I_{discharge.}$, $I_{source\ follower.}$ $V_{GS.}$ is equal to 0.7 volts minus $I_{pull\ down.}$ is equal to $I_{source\ follower.}$ $V_{GS.}$ is equal to 0 volts. If we design the transistor in such a way that the source follower current at $V_{GS.}$ is equal to 0.7 volts minus $I_{pull\ down.}$ which is actually the source follower current at $V_{GS.}$ is equal to 0 volt, if this is true then it is equal to the $I_{source\ follower.}$ at $V_{GS.}$ equal to 0 volt then the charging and discharging times can be made equal which was not possible by the previous circuit.

This circuit by introduction of the source follower here is a much better circuit compared to the previous circuit is an improvement on that because from the speed point of view because during the switching period, you have larger currents to charge and discharge the output capacitances. This particular logic family is called the BFL which stands for buffered fet logic and this is a very popular circuit for cases where you have only depletion mode devices.

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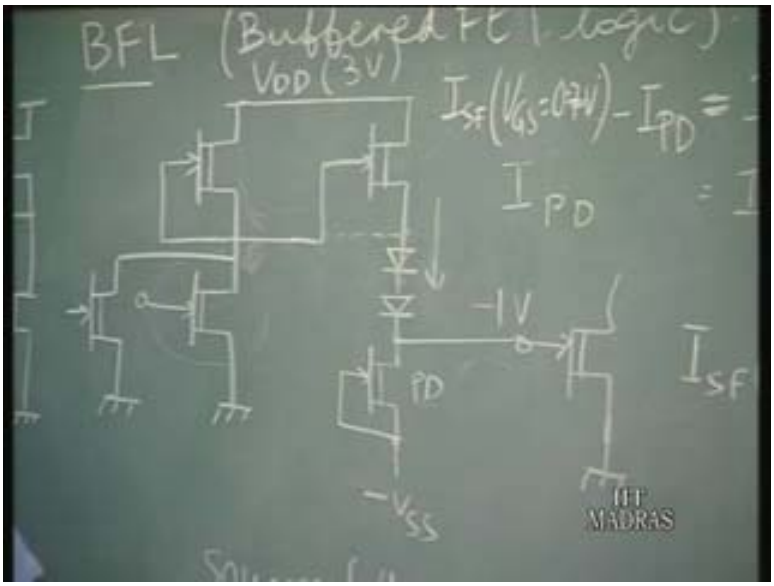

Of course you can now make the NOR gates just like in the previous circuit by adding transistors in parallel to the driver transistor. This circuit is the buffered fet logic circuit and the basic circuit for this logic family is the nor gate and with the nor gate, you can make other complicated circuits. This circuit again just you neither have a usual nor section followed by a level shifter with a source follower which is used to increase or enhance the driving currents for charging and discharging the output capacitance.

That is why this circuit is called the buffered fet logic. This is the one of the logic families using depletion mode transistors and it is quite popular. I will just discuss one

more logic family which also uses only depletion mode transistors which is also quite popular. This particular logic family use a schottky diodes for logic operations and is called the schottky diode fet logic or SDFL for short. This logic family as I said also uses only depletion mode transistors.

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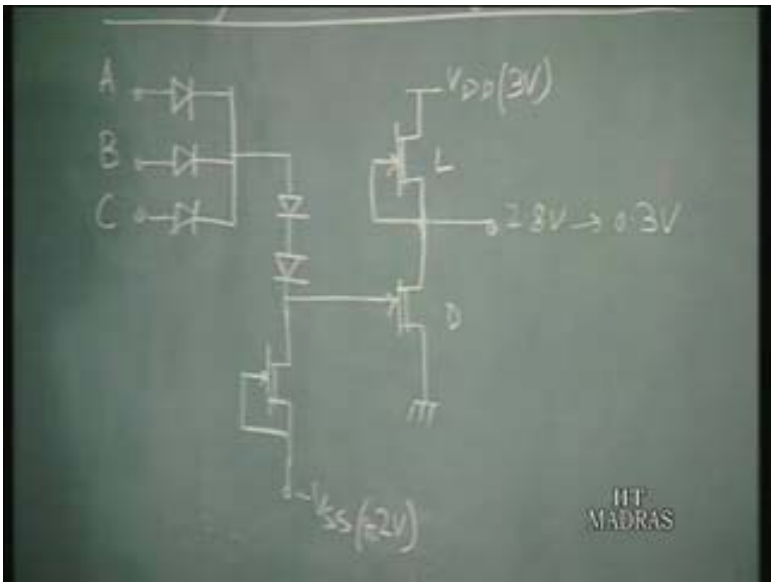

It actually uses schottky diodes to perform the logic operation. The advantage of using a schottky diode is that the schottky diode occupies much less area compared to the other devices, fet's and there by the area requirement is less and so in fact the schottky diode fet logic can be used for large scale integration purposes because it requires much less area compared to the other logic families. Basic circuit is like this. Suppose you have a circuit like this, these are all schottky diodes we have three schottky diodes like this and then this is for the logic operation. Then again you require level shifting because as we said in a depletion mode in all depletion mode logic family because you have to change from positive voltages to negative voltages so that the input transistor can be cut off, you require a level shifting.

Again this is followed by a depletion mode device with a gate to source shorted. This is minus V_{SS} so this is the power supply voltage. If you look at this section here, now if you have three inputs a b c this is nothing but an OR section that is when any of the

inputs goes high, the output is going to go high. Suppose this goes high, the voltage at this point is going to be high. When all the inputs are low then the output voltage is low.

This is then followed by an inverter because we require a NOR or a NAND for normal logic operation. So as universal logic gate, this is a inverter. This is V_{DD}, again you have a dual power supply as in the previous case which is inevitable if you have all depletion mode structure. This is one of the draw backs in fact of all depletion mode circuits. This is the inverter. Now you have a logic section, this is the logic section followed by a level shifting section and followed by an inverter. Now if you look at this, now this output voltage again if you take this as 3 volts say this is minus 2 volt, V_{DD} is 3 volts, V_{SS} is minus 2 volts. Now the output voltage can go high close to V_{DD} when the driver transistor is off.

Then the output voltage goes to say close to V_{DD} then what happens is if we have a similar gate, this is driving a similar gate which means that the input voltages for this logic family can go as high as close to V_{DD} but as this goes close to V_{DD} this input voltage is high that means say 3 volt. If it is 3 volt then this 1, 2, 3 diode drops this will be 0.9 volts but this cannot exceed 0.7 volts.

This 0.7, 1.4, 2.1, 2.8 so basically this output voltage in this case is limited to 2.8 volts. When this goes to 2.8 volts, the input voltage is high and the driver transistor is fully conducting but on the other hand when this driver transistor is fully conducting then what happens is this voltage goes close to 0 volt. This voltage will go close to 0 volt say 0.3 volts. Then the input voltage when it is 0.3 volts if you assume that this is the input to next stage, when the input voltage is 0.3 you have 1, 2, 3 diode drops. The voltage at the gate of the driver transistor is 0.3 minus 2.1 volts so it is minus 1.8 volts which ensures that this driver transistor is cut off.

This driver transistor is cut off and the output voltage is going to go high. We see that the logic levels are compatible. That is when all the input voltages are low here, it would ensure that the driver transistor here is off so the output is going to be high. When all inputs are low the output is high, this is a NOR gate and you get $\overline{A+B+C}$ the whole bar. When any input goes high then this driver transistor is on and the output goes low. When this goes high, this is around 0.7 volts here so this is going to pull down the output and the output is going to go low.

Here we have a NOR gate so this logic is performed using mostly schottky diodes and as we said the schottky diodes has less area so this is suitable for large scale integration. In fact you can have a lot of variations using the schottky diode fet logic family for example you can have OR and invert type of operations say for example if you have circuit like this, so these are the say 4 inputs. This is A, B, this is C, D and you have to follow up with a level shifting circuitry followed by pull down transistor.

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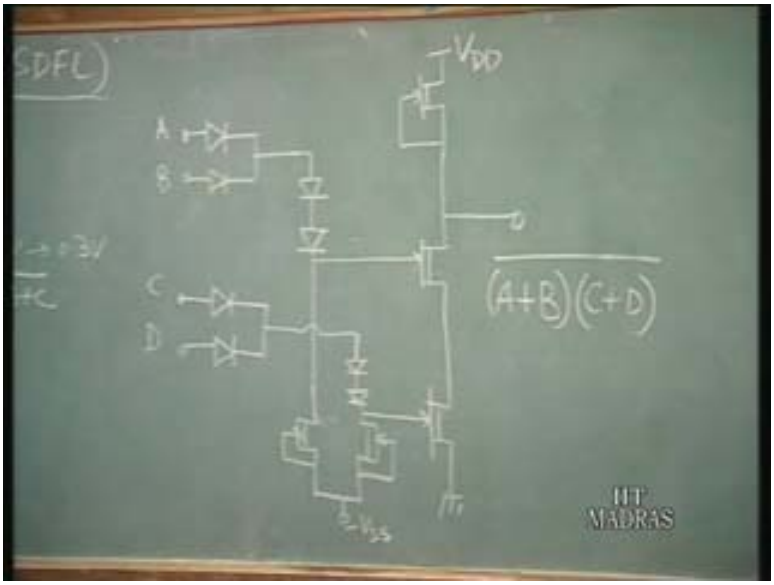

Here again you have another set of level shifting circuitry followed up by the pull down transistor. This is minus V_{SS} and so this point and these points they actually go to the input of this section. This is like a NAND configuration so here again we have the load transistor. If you look at this circuit now the output is going to be low, when both these driver transistor here turn on and when are both these transistors going to turn on? When either A or B is high and C or D is high. The logic which is performed here is A or B and C or D inverted. That is when either A or B is high then this particular transistor conducts and when either C or D is high then the lower transistor here conducts.

When both these transistors conducts then only the lowers section is going to conduct and it is going to pull the output down. This particular logic function is achieved in this case. Now you can have even further complication, you can also introduce. Suppose you have another section on the other side. I shall draw it like this. This is the another set of depletion mode transistors and again you have a four more input say this is one another input here, you have two more inputs here.

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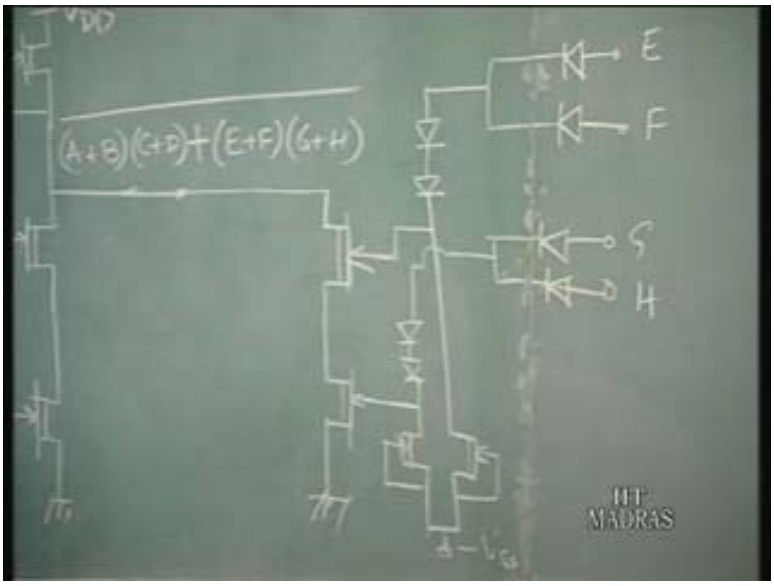

Again similar as before, what we do is we have level shifting and pull down transistor and from here again you have another two diodes for level shifting followed by the pull down transistor. These are always parts of the circuits minus V_{SS}. Now from here you have this output going from here it goes here. So if you call this A B C D then this is E F G H. Now what you have is in fact this is not required. In this particular configuration when is the output going to go low? The output is going to go low when either this section conducts or this section conducts, when either of these two sections conduct then the lower part conducts and the output is going to go low.

When is any of these sections going to conduct? When both these transistors say if this section is going to conduct, when both these transistors are on and if this section is going to conduct then both these transistors have to be on and again for any of these transistors to be on, any of the inputs connected to that particular transistor must go high. Then for this particular structure the logic we have is (A or B) and (C or D). This will ensure that both these transistors here conduct. For both the transistor here to conduct, you have E or F and G or H and if any of these two conditions are satisfied then the output is going to low.

You have an OR function here and then since the output is going to go low when any of these conditions are satisfied, you have a bar here. The logic which you achieve is (A or B) and (C or D) or (E or F) (G or H). You see that one can achieve very complicated logic circuits using this schottky diode FET logic by connecting schottky diodes basically in different configurations. Again to reiterate the advantages of circuit is that is it uses schottky diodes mostly and schottky diodes occupy less area, small area and so they are suited for large scale integration. You can have lot of complicated logic circuitry using less area and so it is more suited for large scale integration. Also

schottky diode as we have already discussed are majority carrier devices so they are quite high speed devices as well.

The disadvantage of this particular logic family is that one major disadvantage is if you look at this, the input is always going to draw current irrespective of whether the input is high or low because you must have these diodes on, 0.7 volts for that there must be current flowing. This current has to be driven by the output of the previous gate. The output of the previous gate which is driving this gate is always loaded by this particular gate and ofcourse the loading is going to be more, if you have a more fan outs. The loading is going to dependent on fan out, so all this must be taken care of while we are designing these logic circuits.

In today's class, we have discussed two logic families using depletion mode transistors. In last class we had discussed two logic families which used a combination of depletion mode and an enhancement mode transistor. Of course I would like to conclude that the logic circuits which we discussed last class that is which uses both depletion and enhancement mode transistors are better in lot of ways in the sense that you have single power supply. You have lower power dissipation because you just require 1.5 volts for the circuit operation, one single power supplied 1.5 volts. They are also quite compact in the sense especially the direct coupled FET logic in the sense you require very few transistors but you have to pay for it in terms of improved technology because you must be able to fabricate both enhancement mode and depletion mode transistors simultaneously.

On the other hand these logic family which we discuss today use only depletion mode transistors. They does not require so complicated technology but you have to pay for it. They are not as fast as the logic circuits which we discussed last class that is using both enhancement mode and depletion mode and of course you have to have two power supplies and usually more number of transistors so that way there is a tradeoff. This is about FET logic family. There are of course other logic families also, in fact there are logic families which imply only enhancement mode transistors and some other logic families but we will restrict our discussion to these logic families which appear to be more popular in the FET logic family.

Thank you.