Digital Integrated Circuits
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Lecture -38

Direct Coupled FET logic;
Superbuffer FET logic

In the last class we were discussing the MESFET, a device which is generally used in compound semiconductors. We saw that the device consists of an n type channel on semi insulating material which depends on whether you are using gallium arsenide or indium phosphide, you will have semi insulting gallium arsenide or indium phosphide.

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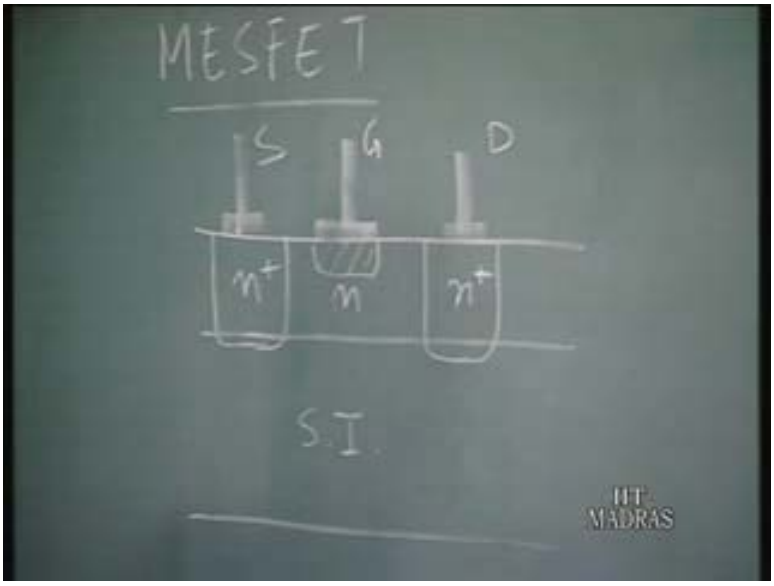

You have heavily doped regions for the formation of the source and drain so here we have the gate which controls the current. You have the source, drain and the gate. There is a depletion region between the source and the drain in the channel region and the gate voltage actually controls the thickness of this depletion region and thereby controls the current. Now we have seen that you can have two types of MESFET's the enhancement type and the depletion type. The enhancement type is the one which is normally off that is with zero gate voltage, there is no current flowing. The symbol of this device is like this and this is enhancement mesfet and you have the depletion mesfet which is normally an on device and the symbol is like this.

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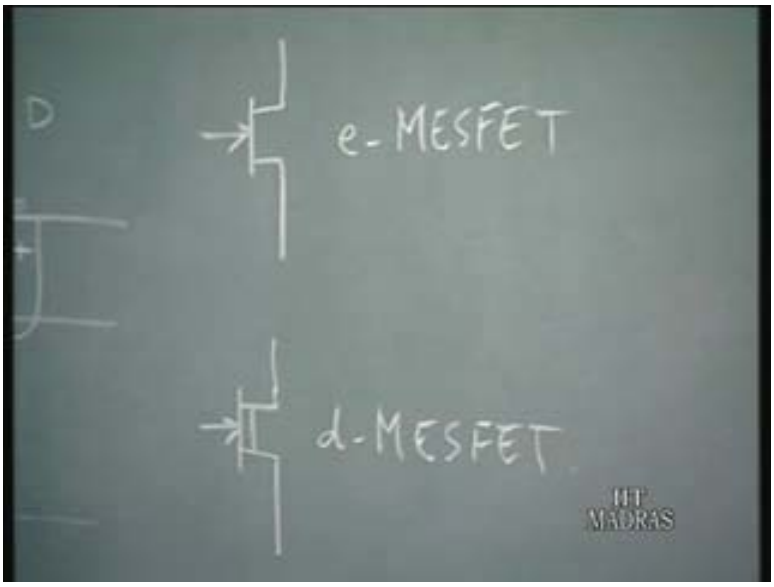

Finally we have also seen the small signal equivalent circuit of this device. It consists of current source between the drain and source. So this is the drain, this is the source this is given by g_m v_{gs}, the drain resistance R_D and the capacitances between gate and source C_{GS} and the capacitance between the gate and drain C_{GD}.

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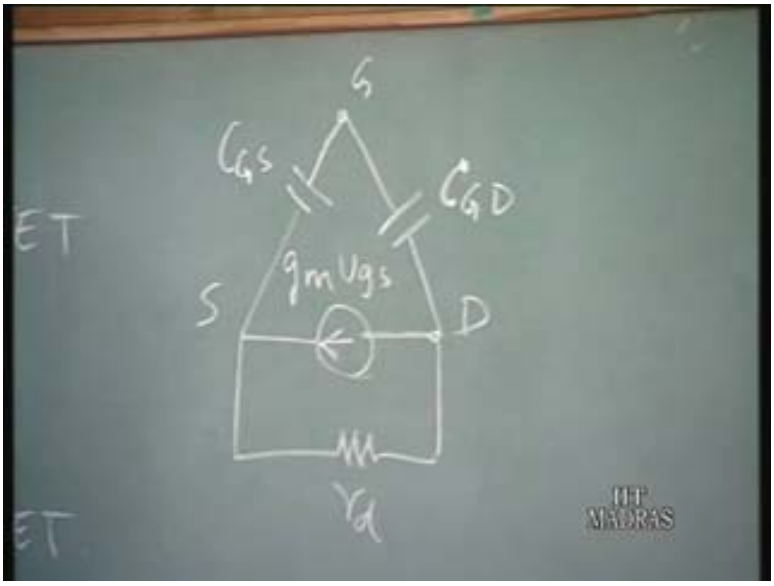

That is what we had seen in the last class. Let us try to look at some values of g_m that is the trans conductance. The drain current of this mesfet can be given by I_D is equal to that is the cross sectional area of the device which is equal to the width of the device into this thickness which is nothing but so if the depletion width is d and the total thickness of the n region is t so that is going to be t - d.

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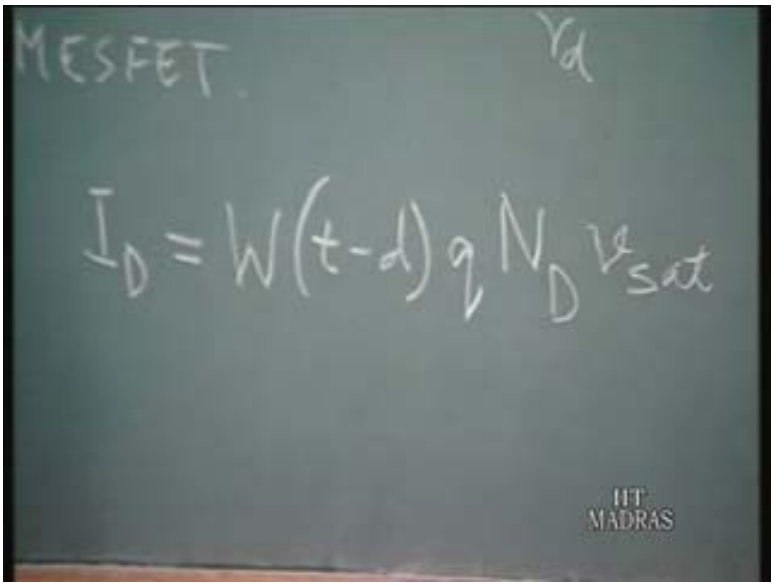

If the width of the device is given as w, so w into t - d is the cross sectional area, q the concentration of the carriers N into velocity. We assume that the carriers are flowing at the saturation velocity which is correct for modern day devices which are very short channel lengths and therefore very high electric fields. Now the g_m is given by g_m is equal to del I_D del v_{gs} which can be written as del I_D by del d where d is the thickness of the depletion layer to del d by del v_{gs}.

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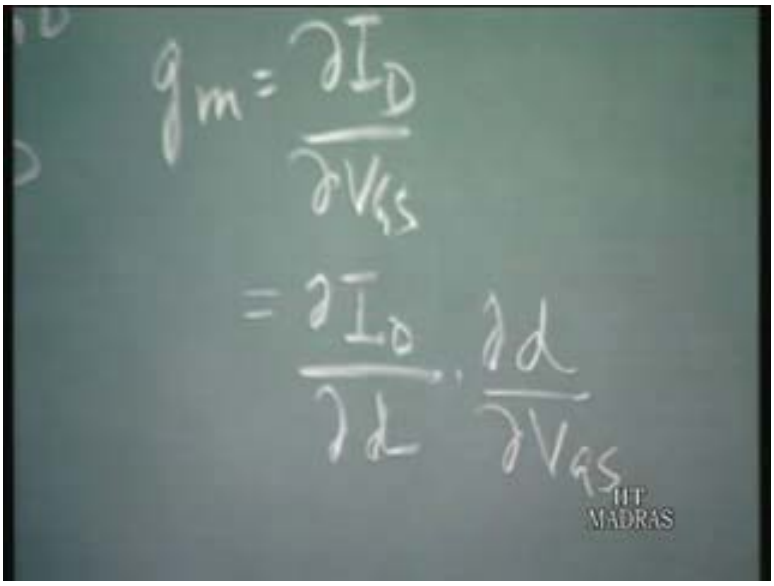

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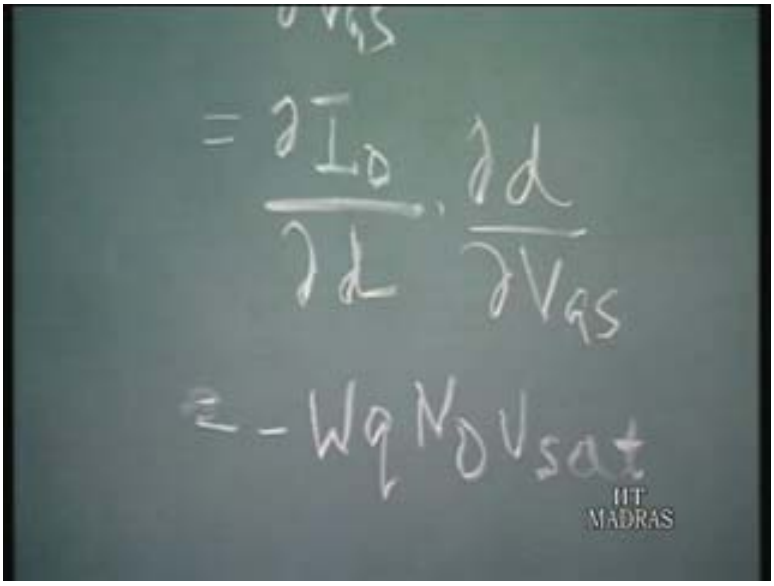

Now from this relation del I_D by del d will be equal to minus w q N_D V_{sat} and now we have to look at variation of d with respect to v_{gs}. If we assume that the depletion layer width is almost a constant from the source to the drain end, we can write that d is equal to twice epsilon that is the v_{bi} is minus v_{gs} by q N_D. This is the drop across the depletion region.

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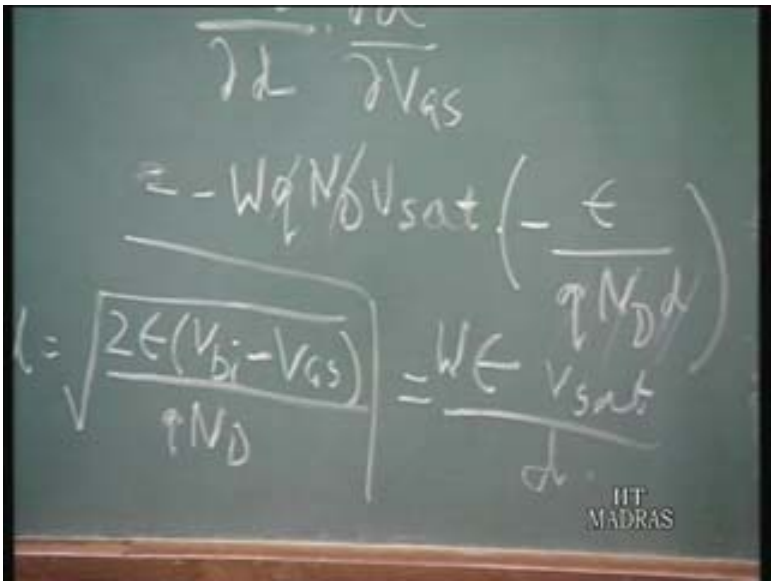

Now this gives rise to del d del v_{gs} which will be equal to minus of epsilon by q N_D into d which gives us g_m is equal to, this N_D will cancel, q will cancel. You have w epsilon v_{sat} by d. This is the g_m of the device, g_m is equal to w epsilon v_{sat} by d.
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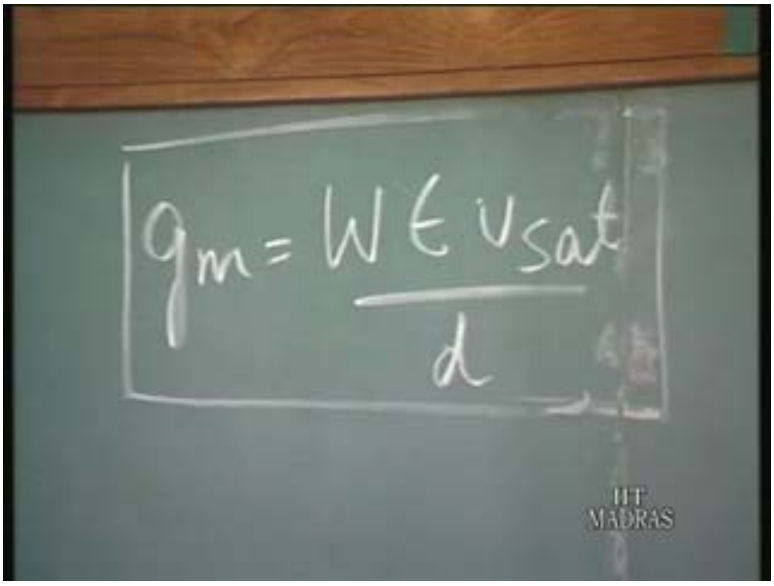

Now let us consider a MESFET and we apply a gate to source voltage v_{gs} and a small signal, a small v_{gs} and then we short the drain to source and then the current flowing in is I_G and the drain to source current is I_D.

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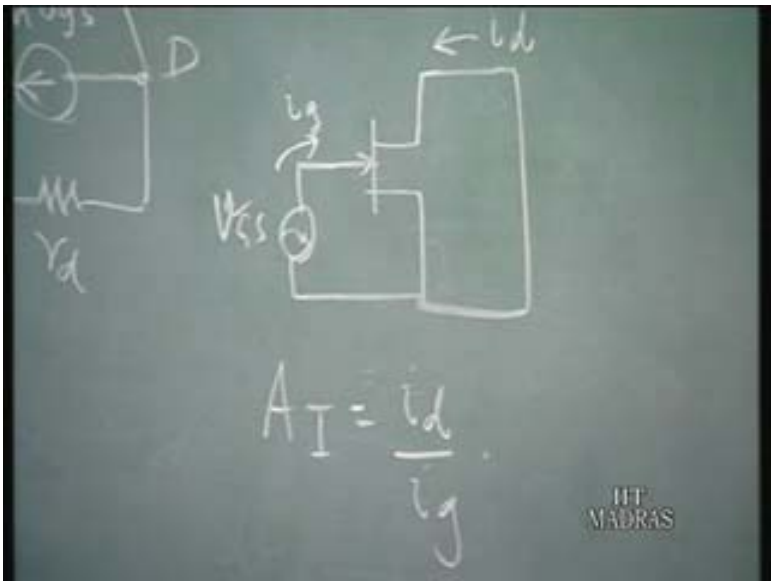

Now the current gain of this is A_I is equal to I_D by I_G. An important parameter for MESFET as well as for many other devices is the f_T. f_T is defined as the frequency at which the current gain goes to unity. Now let us see how we can obtain this value of f_T. Now in this circuit if you look at this we have applied the small signal v_{gs} between the gate and the source. The source is grounded so v_{gs}.

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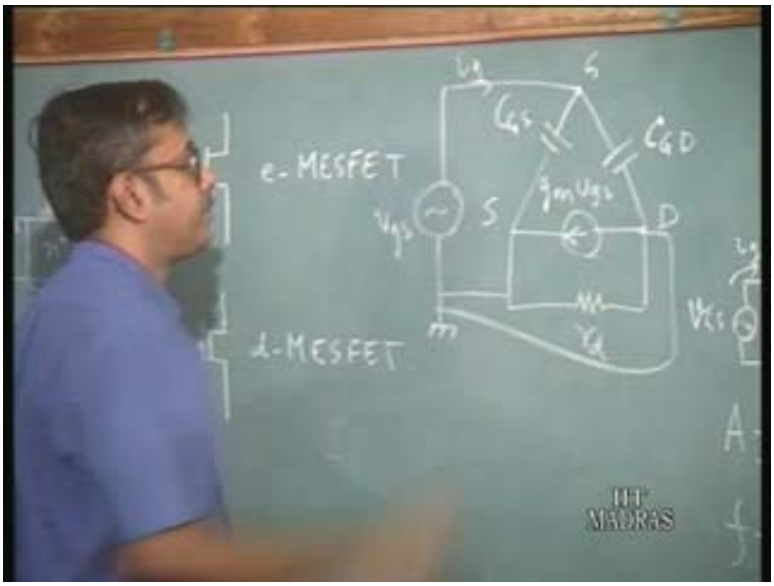

We have shorted the drain to the source and so I_G is the current flowing here. I_G will be given by, this is the two capacitance here in parallel. So you have I_G is equal to j omega C_{GS} plus C_{GD} into v_{gs}. What is I_D?

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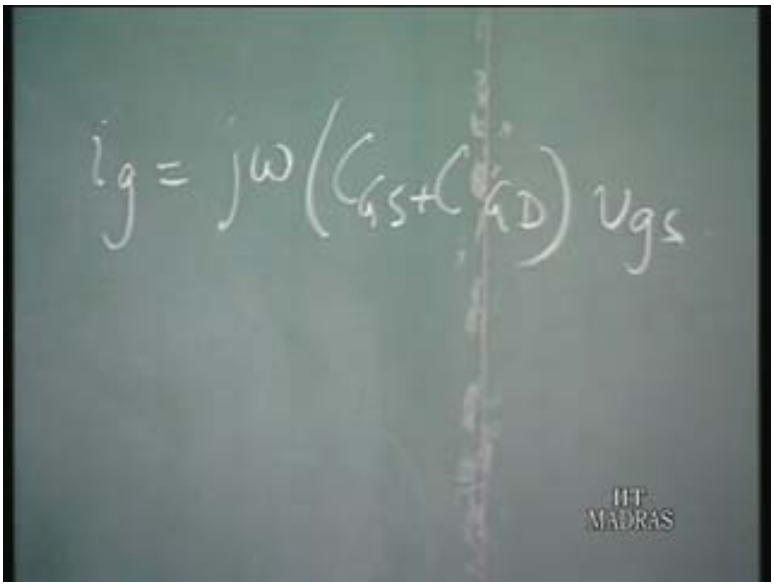

I_D is equal to g_m v_{gs} therefore A_I modulus of the current gain is equal to g_m by omega C_{GS} plus C_{GD}..

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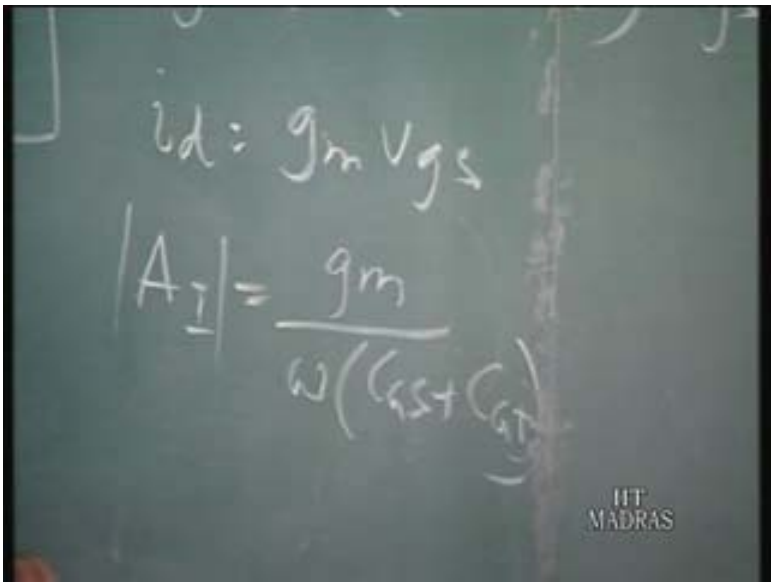

Now C_{GS} plus C_{GD} that is the total capacitance can be written as C_{GS} plus C_{GD} is equal to w into l that is the area epsilon by the depletion width.

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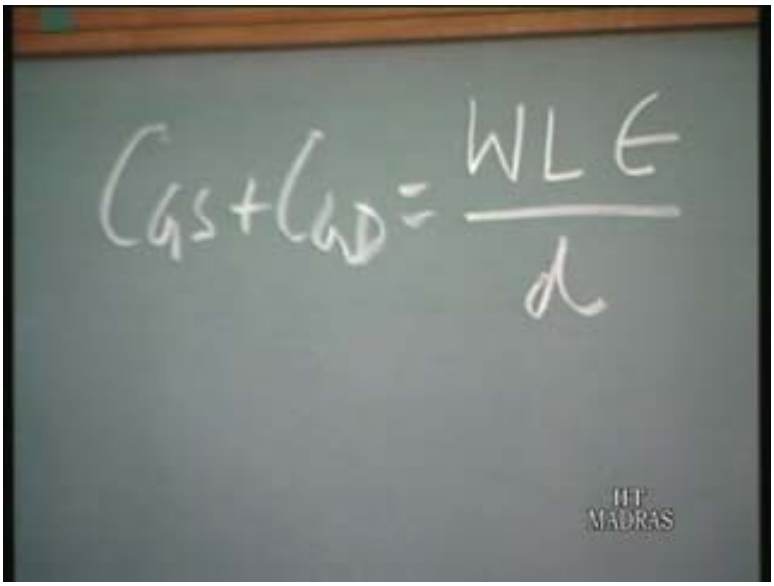

Now if we substitute it here what we get is, the value of g_m we already know w epsilon v_{sat} by d. Now we have C_{GS}, so you have omega here d into w l epsilon into d. This d will cancel, w will cancel.

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Epsilon will cancel and we are left with v_{sat} by omega L. This is the current gain v_{sat} by omega L. The frequency at which the current gain goes to unity is given by f_t is equal to v_{sat} by twice pi L.

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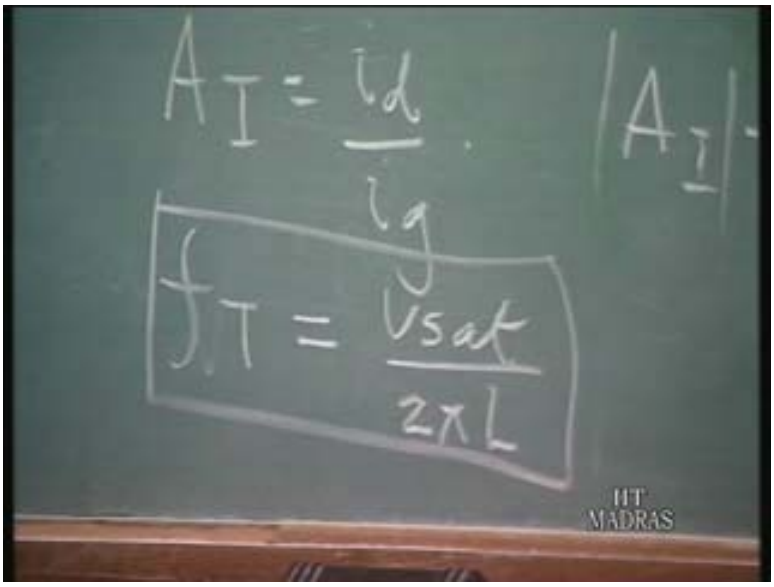

The frequency at which the current gain is going to go to unity is v_{sat} by twice pi L. This is the f_t of the device. Now usually the v_{sat} of the MESFET is around 10 to the power 7 centimeter per second. So if you have L of 1 micron which is 10 to power minus 4 centimeter.

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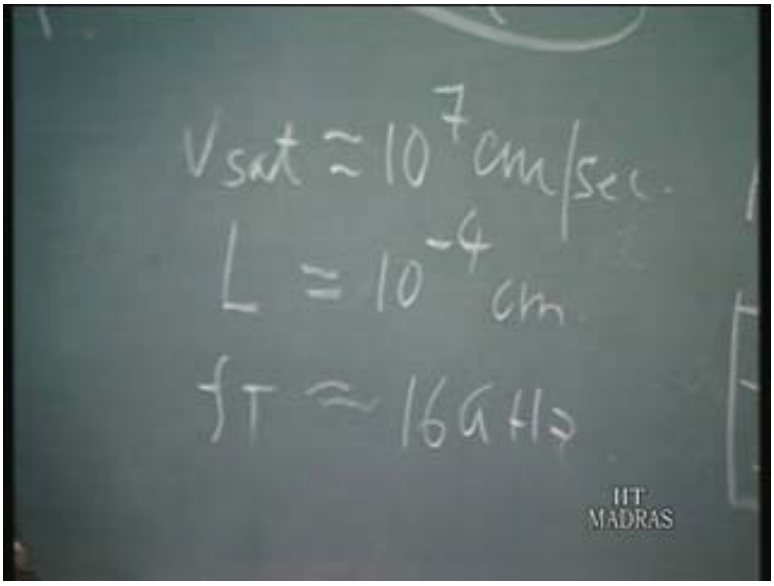

Then f_t will be according to this formula which will be around 16 giga hertz. Important thing to note here is that f_t is inversely proportional to L. If you keep on reducing L,

the f_t will go up. If you go from 1 micron to 0.1 micron, f_t will go from 16 gig hertz to 160 giga hertz. Of course what will happen is if you go on reducing L then there are other parasitic which may come into picture. In fact in this A_I relation, if you assume that there is a parasitic capacitance that is instead of g_m by w C_{GS} plus C_{GD}, if you assume that A_I is equal to g_m by w C_{GS} plus C_{GD} plus c some parasitic then the f_t value which you will get can be written as 1 by f_t is equal to 1 by v_{sat} by twice pi L + 1 by g_m by $c_{parasitic}$.

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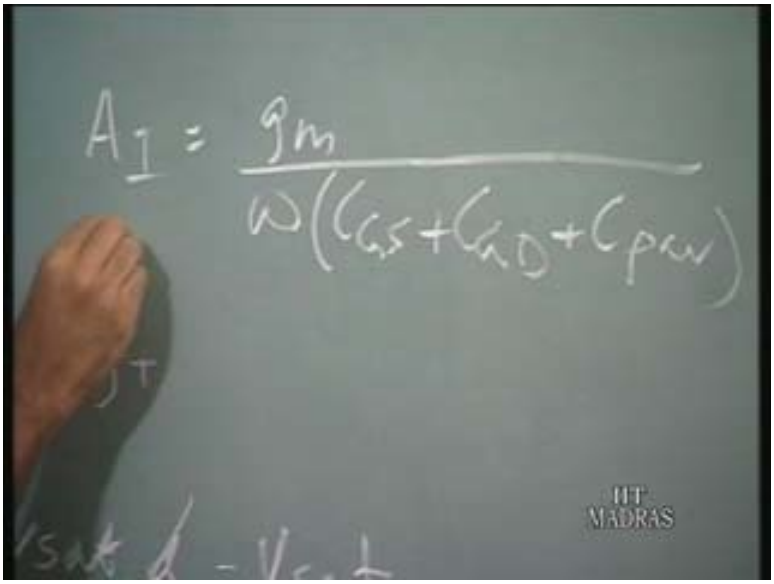

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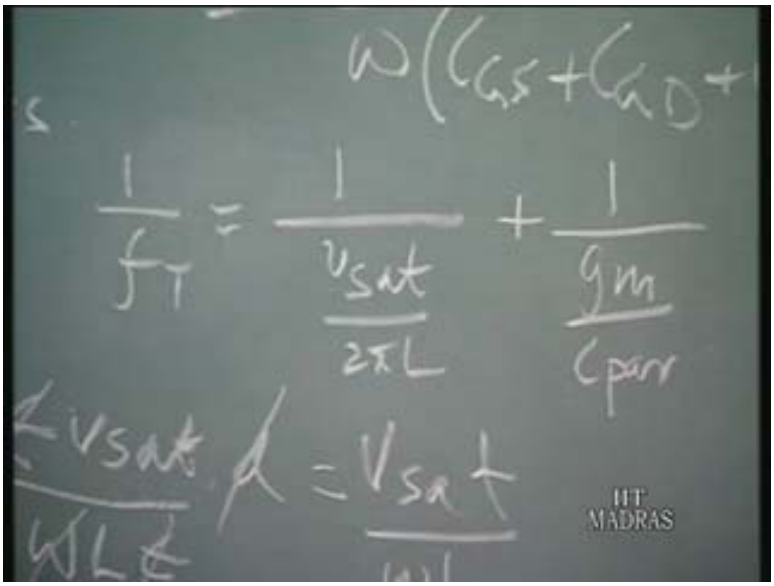

What happens is when the parasitic capacitance is small, this term is going to be quite large so it is actually, the f_t is controlled by this term, f_t is going to be v_{sat} by twice pi L but when by reducing the channel length when this term becomes large then this is the smaller term here so this is going to play a dominant role and the f_t of the device is actually going to be a controlled by the parasitic capacitances. If you go on reducing the channel length, you may not get a reduction in the f_t after a while because of the importance of the parasitic.

One thing important to note again here is that the g_m plays a role here. If the g_m of the device is high then the effect of the parasitic is in fact reduced. To achieve a high f_t, you must reduce the channel length of the device and after a while ofcourse if you keep on reducing the channel length then the f_t is determined by the parasitic. It is also important to reduce the parasitic capacitances. Coming back to this expression here, f_t is equal to v_{sat} by twice pi L, since the f_t of the device which is inversely proportional to L we must always make an effort to reduce the channel length as far as possible. If we have a circuit, the channel lengths of the MESFET's must be made as small as possible. So that has to be the minimum afforded which the technology can take.

If you have a one micron technology, the channel length of all the devices are kept at one micron. You see that the widths of the devices do not come into picture because the f_t is not controlled by the width. You can look at it this way that if we increase the width of the device it is true that the input capacitances go up but again the currents are also going to up because the current is proportional to width. So you have a larger current driving a larger capacitance. The time required to charge the capacitance or discharge the capacitance remains the same whereas if you increase the channel length of the device, you increase the capacitance without corresponding increase in current, so the f_t will go down.
Basically the channel length must be retained at the minimum so that what is done in any MESFET circuit, the channel lengths of all devices are maintained at the minimum value and we play around with the width of the device to design a better circuit. With this background we shall start our discussion on MESFET logic circuits and as usual we shall take up the inverter first and then try to see how these circuits involving inverters can be modified to form other gates. The inverter circuit you have is very similar to the other inverter circuits, the MOS family. A simple inverter would have a MESFET and a load resistance, we call the drain resistance. The input voltage is applied here and the output voltage is here.

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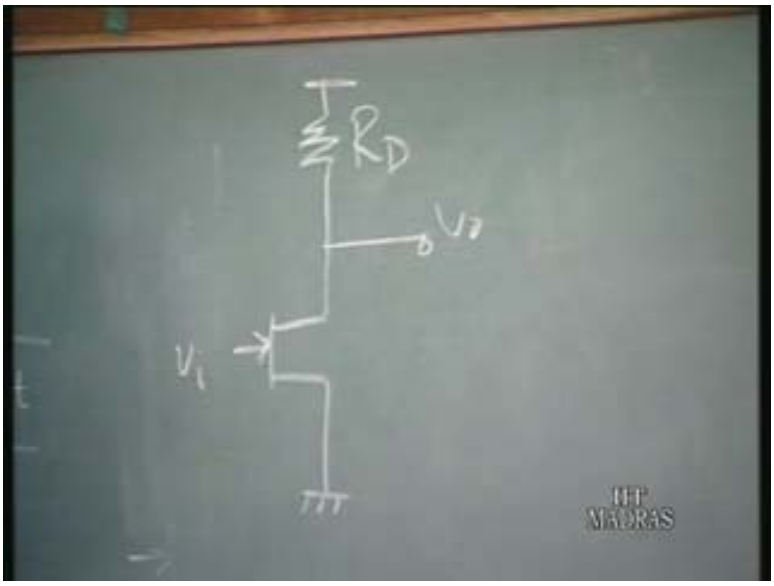

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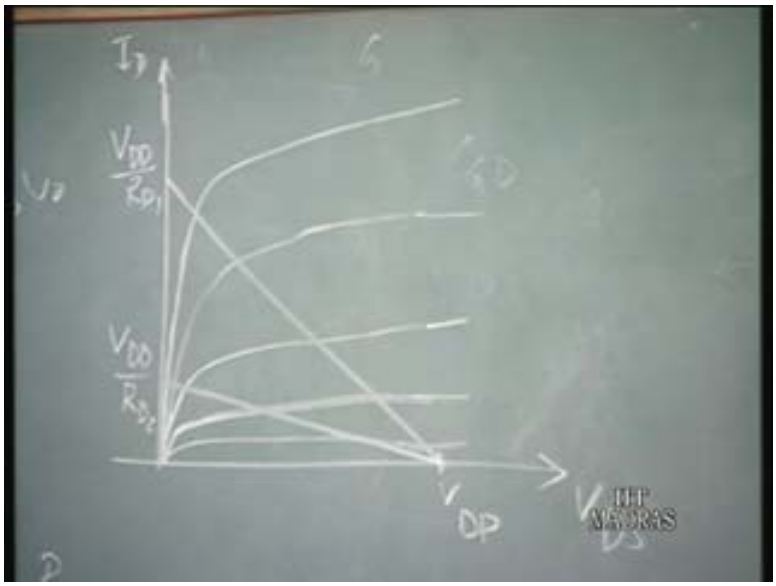

The way to find out the input output characteristics is also quite simple and similar to other logic circuits. That is we first draw the drain current versus the drain to source voltage that is the output characteristics of the device which looks like this and then we draw the load line. Now if this is the resistance, the load line is going to be something like this and this value is V_{DD} by R_D and this is V_{DD}.

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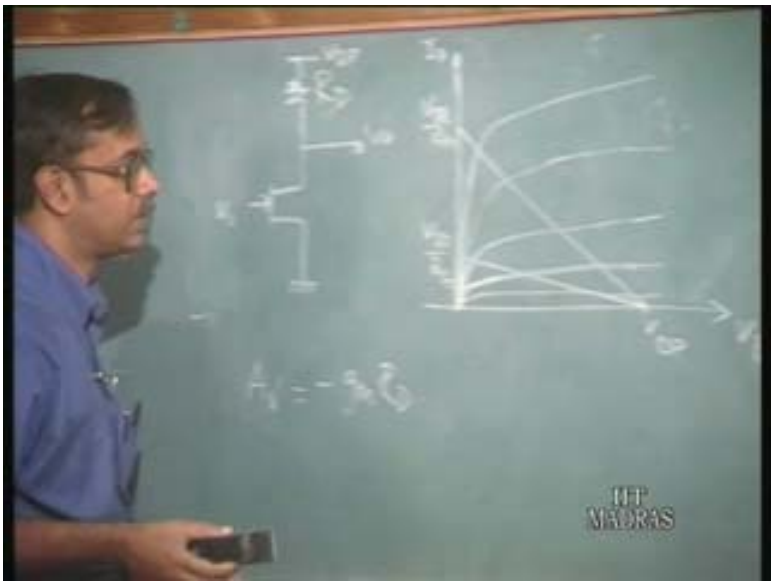

Now this also behaves as an amplifier and the gain of the amplifier, voltage gain is equal to minus $g_m R_D$. For a good inverter, the gain of the amplifier must be high. That is the transition from the high state to the low state must take place at a rapid rate that is for small change in the input voltage, we must have a sharp transition from the high to the low level. This depends on R_D, this is suppose a low value of R_D, if you have high value of R_D then the load line is going to be something like this, here it is going to be V_{DD} by R_D. Say this is R_{D1} this is R_{D2}, R_{D2} is at a higher value than R_{D1}. Now if you increase the value of R_D it is expected that the gain may go up from this relation but that is not true because this g_m also depends on the current. If we are increasing the value of R_D the device is going to operate at a lower value of current as we see here and the g_m is proportional to the current. So at the low values of drain current the g_m is lower.

In fact we do not get a high gain as such, as we could expect from this relationship. This resistance as a load usually is not a very popular circuit. The circuit which is used generally is having an active device depletion mode MESFET as a load and which has its gate to source shorted and the driver device is another MESFET here.

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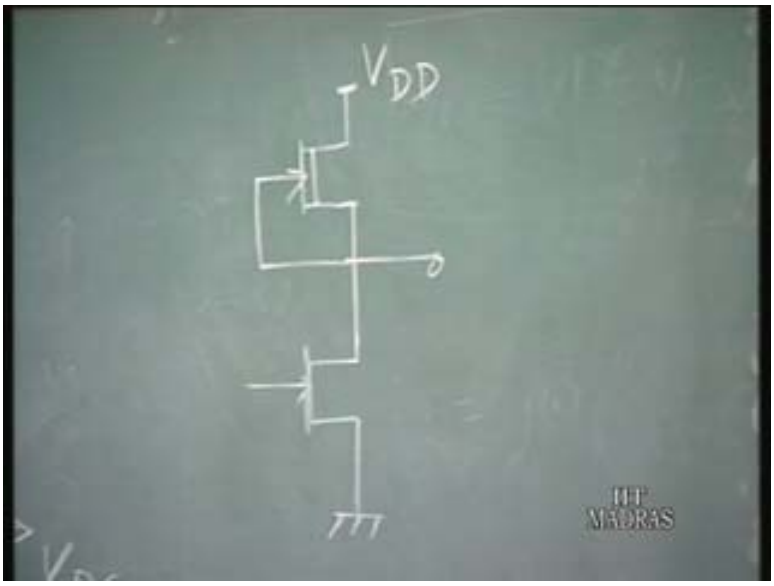

Now this driver device can be an enhancement type device, it can be a depletion type device, it does not really matter at this point. If you consider this device here, now the load line which you have is actually going to be the characteristic of the driver device. This is the depletion mode load with v_{gs} equal to zero. Now since this is the depletion mode device it is a normally on device, so even for v_{gs} equal to zero the device is going to conduct. The characteristic of the device at v_{gs} is equal to zero should be used as the load line. It may be something like this, so this is the load line. This is the depletion load. Now if we look at this curve, if you want to plot the input output characteristics v_i the output.

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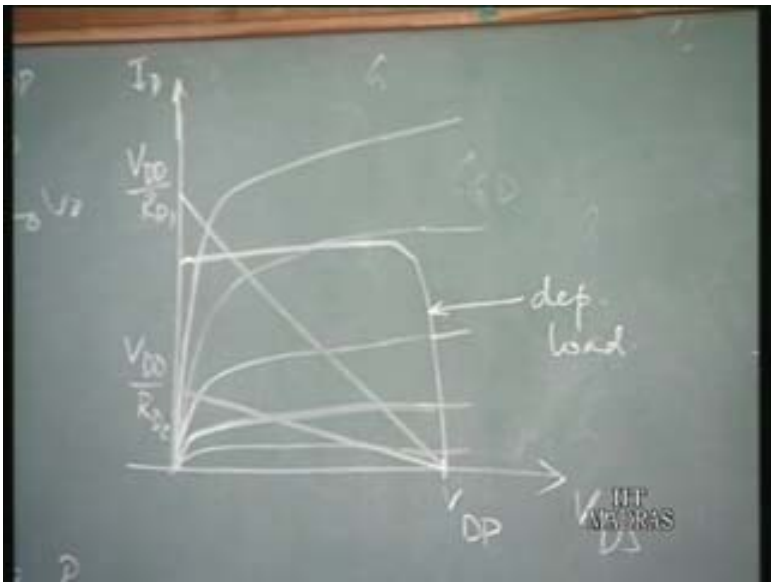

When v_i is low that is the gate to source voltage is low and the operating point is given by the intersection of the IV characteristics of the driver device and the load line. At the low voltages, output is nearly equal to V_{DD} and then what you have is in this region where the load characteristic is almost flat, for a small change in the input voltage the output voltage changes drastically from a high value to a low value. If you take two very closely spaced curves, one curve here and another curve here, for a small change in gate to source voltage the point of intersection changes from here to here. The output voltage falls sharply so you have something like this and then it falls sharply and then if you go on increasing the gate voltage, there is a small change. This is the input output characteristics of the inverter here which has a depletion mode load.

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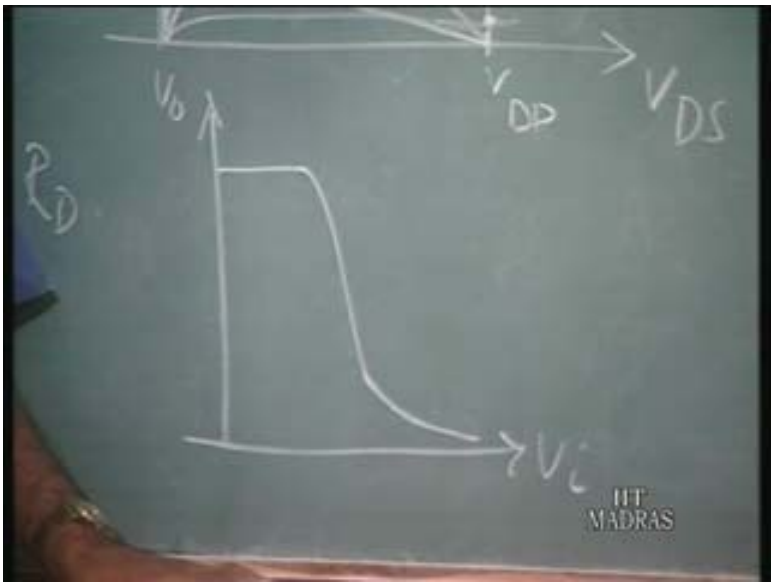

Now the advantage here is if you look at it, the important point of the characteristic is this region and in this region the IV characteristic is almost parallel to the x axis so it actually behaves as a very high resistance. At the same time the operation takes place at a high value of current so what you have if you go back to this relationship A_v is equal to minus g_m R_D. Since the transition from the high level to the low level takes place at a high value of current, g_m is high. At the same time the effective drain resistance is also very high because the IV characteristics is almost parallel to the x axis, so both of them are high and you have a very high gain. This gives rise to a characteristic like this and we have a very high gain at this portion that is in the transition region from the high to the low level.

Of course one point is to be noted in this circuit, since the load device is always on it is not going to be off like a CMOS, the output voltage does not really go to a zero value. It approaches zero for high input voltages but it does not really go towards zero value. This is the circuit of the inverter which we shall take up and is usually used in all

mesfet logic circuits and several modifications are made for realizing different types of logic families. We shall first take up the logic family which is called DCFL which stands for direct coupled FET logic.
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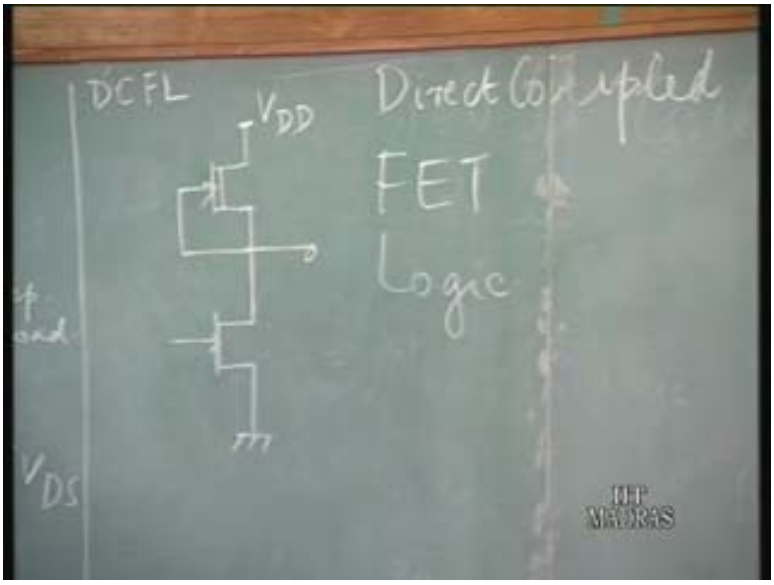

Now this circuit consist of an inverter, this is the basic inverter for this logic family. It consists of an enhancement type driver transistor and a depletion type load transistor where the gate to source of the load transistor is shorted. If you take such a circuit and consider that this is connected to the input of another gate that is basically one inverter driving another inverter, let us look at characteristics of this logic family.

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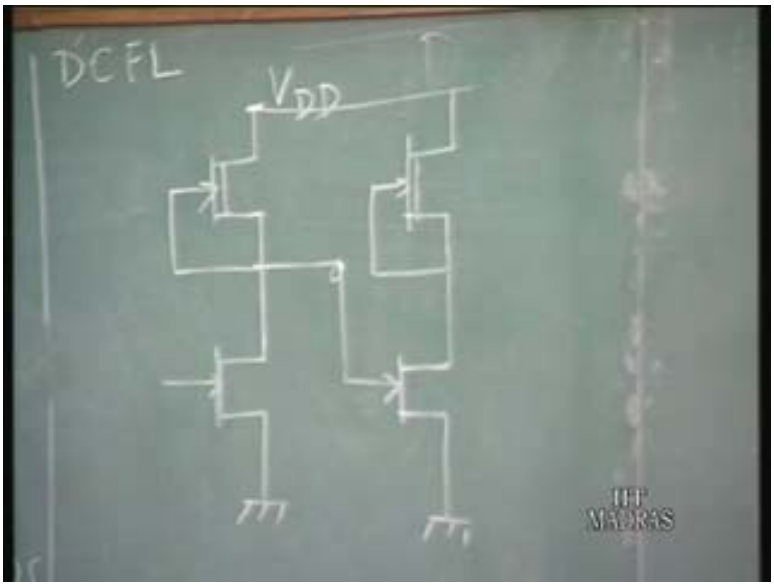

Let us go back and draw the load line again. Draw the characteristics and the load line to obtain the input output characteristics. We have the IV characteristics of the driver transistor and what we do is we draw the IV characteristics of the load which is a depletion mode load at v_{gs} is equal to zero.

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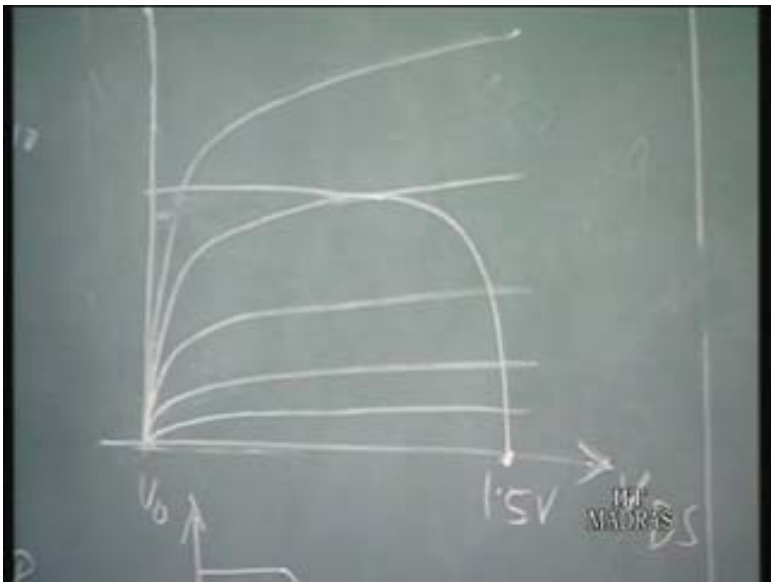

This is the characteristic of the load device. Now in this circuit let V_{DD} is 1.5 volt that is usual voltages at which the DCFL direct coupled fet logic circuits operate. Now another point to note here is that this output of this inverter is actually driving the input of the next gate. If we come back to the cross section view of the MESFET what we have is a schottky diode.

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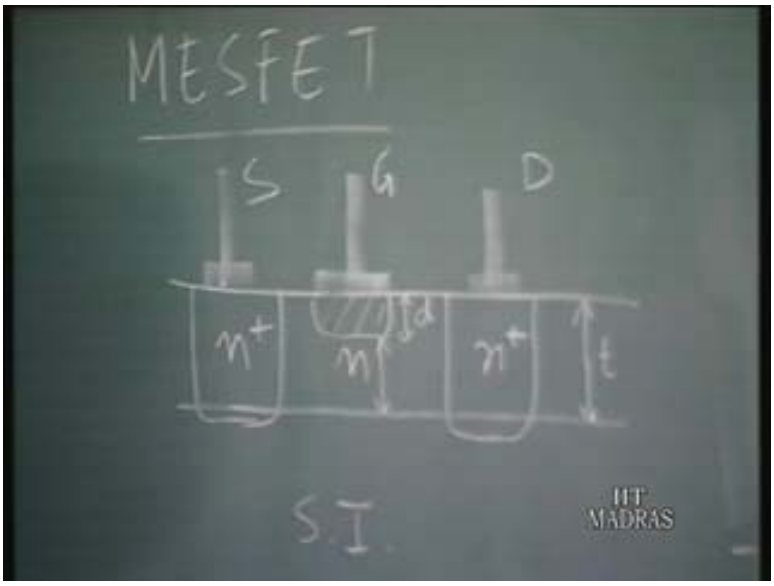

A schottky diode is a metal semiconductor junction diode and it behaves as a normal diode, the characteristics is like a normal diode and it has got a cut in voltage. If the voltage across the device, forward bias across the device exceeds the cut in voltage, there is going to be conduction. If the characteristics of the schottky diode is just like another diode, it is something like this.

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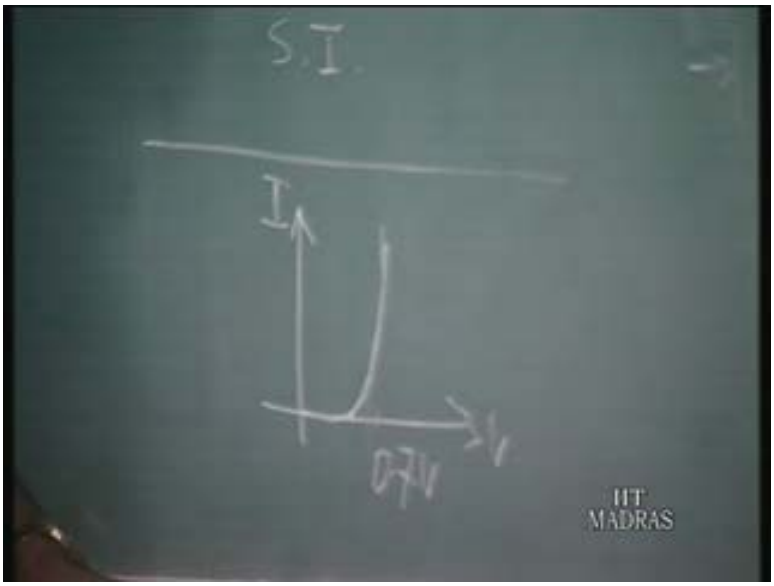

Once the input voltage exceeds this value then there is going to be conduction and the voltage is clamped to almost this value. For a compound semiconductor like gallium arsenide, the cut in voltage here is around 0.7 volts which means that if the input voltage, the gate to source voltage cannot exceed 0.7 volts because there is going to be

heavy conduction and the input voltage gets clamped at 0.7 volts. If you come back to this circuit here, it means that the output voltage of this inverter here is going to get clamped at 0.7 volts. This voltage here cannot exceed 0.7 volts because it is connected to an input here which has a diode here with a cut in voltage of 0.7 volts. What we do is in this figure here, we draw another curve like this which is actually the characteristic of the diode and this is around 0.65 or 0.7 volts say 0.65 volts, let us put it like that.

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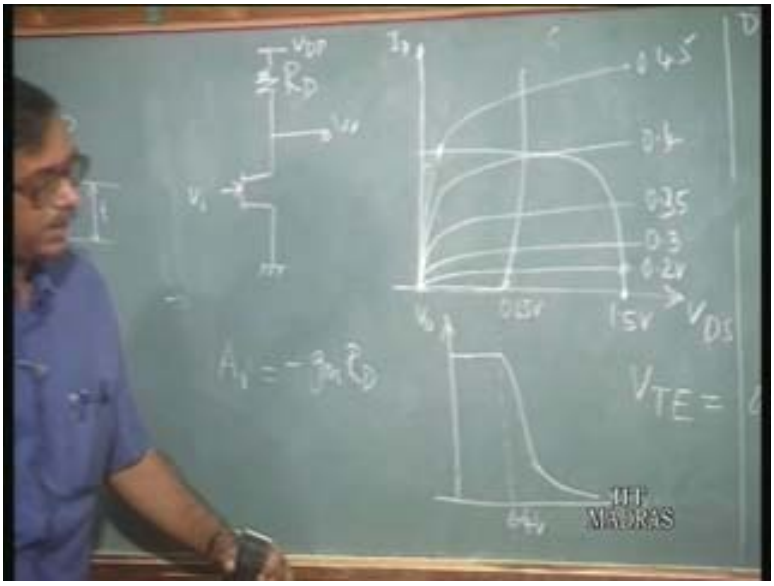

What happens is this output voltage of the device cannot exceed this value. Now this is the maximum value that the output voltage can have because it is going to be clamped by this. Now let us assume that the V_{TE} that is the threshold voltage of the enhancement mode device is 0.15 volts. This can be 0.2 volt, this can be 0.3 volts, this can be say 0.35, 0.4 like this. Now I am just drawing some values of the input voltage for which these are the characteristics. Now what happens is if you look at this, when input voltage is 0.2 volts this is the curve, the point of intersection is here but the output

voltage can be at this value, it cannot be this value (Refer Slide Time: 30: 02). The output voltage is going to be clamped at almost 0.7 volts.

If we go increasing the input voltage 0.3 volts again this point of intersection is here but the output voltage is actually going to be here because it cannot exceed this value. It cannot be more than this value, 0.35 again it is here. The output voltage is almost a constant, it remains a constant given by this curve. So at 0.4 volts also it is here. So it is 0.4 volts but then what happens? If we now exceed the input voltage slightly above 0.4 volts, say this one is 0.45 what happens is the point of intersection of this and this comes here (Refer Slide Time: 30:45). So from 0.4 to 0.45 the output voltage falls from 0.7 volts to a very small value. Here this can be around 0.4 volts, this is 0.4 volts so it has fallen sharply as we go above 0.4 volts. Then this is the very small value.

If we go on increasing the input voltage, the points of intersection will move little slightly and the input voltage will keep falling. This is the output voltage characteristics of the DCFL inverter where this is 0.7 volts. The logic high is 0.7 volts and the output voltage keeps falling as we increase the input voltage. You see that we have a flat characteristics that is because of the fact that the output voltage is clamped to 0.7 volts and then there is a sharp drop and then it gradually approaches zero.

Now the important point for this inverter is that the output voltage, so when the input voltage approaches 0.7 volts that is when the input voltage is high, the output voltage should be low enough. If we go to look at this inverter, when the input voltage is high may be 8, the output voltage is low $V_{L.}$ and this low value must be less than the threshold voltage of this device which is as we have assumed 0.15 volts say. So $V_{L.}$ must be less than 0.15 volt so that this device is turned off and then when this device is turned off, the output can again approach $V_{H.}$. This is the design criteria that when input is high output voltage should go below the threshold voltage of the inverter. Now how do you control the output voltage at this point? The logic low value, how do you control? It is controlled by the ratio of the widths of the driver and the load transistor. This is the driver transistor, so it has width $W_{D.}$, this has the width $W_{L.}$ that is the width of the transistor.

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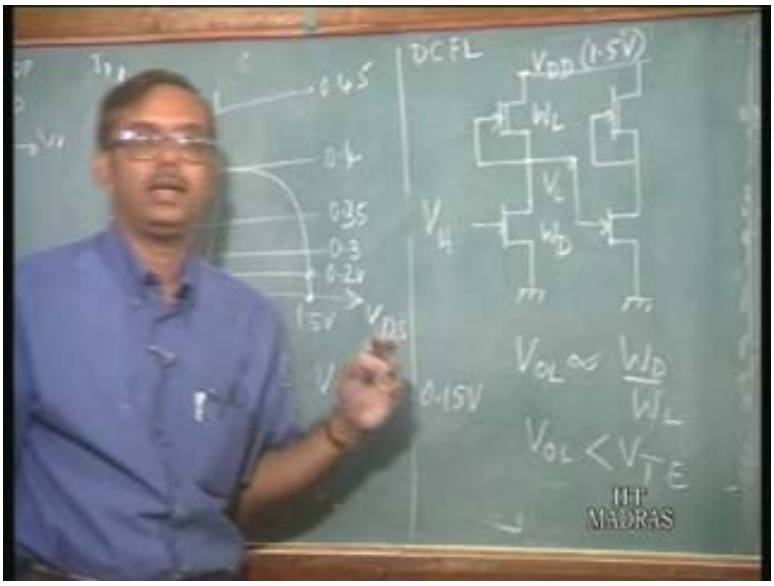

As we have already said the channel lengths of these devices are the same and equal to the minimum value afforded by that technology. Now V_{OL} the logic load is proportional to W_D by W_L. If you make the width of the driver device larger compared to the width of the load device then the output voltage is going to fall. That is how we can make the output voltage lower but ofcourse we do not want to make the width very large because that is going to increase the input capacitance of this device and which is going to slow down this device. But we want V_{OL} should be less than V_{TE}. Now we cannot make V_{TE} very large either that is the threshold voltage of the enhancement device we cannot make it large in order that V_{OL} will always be less than V_{TE} that is not possible because if V_{TE} is large what happens is the current or the g_m of the transistors are proportional to V_{GS} minus V_{TE}. The g_m of the transistors is proportional to V_{GS} minus V_{TE}.

Now if V_{TE} is large and V_{GS} maximum can be 0.7 volts so you see that g_m of the device which is proportional to V_{GS} - V_{TE} is going to be small. We want V_{TE} to be small so that V_{GS} minus V_{TE} is large so you have a high gain of the device. The design of a good circuit is we want V_{TE} low at the same time, we want V_{OL} to be even lower. That is why we have to increase W_D by W_L but we should not make it too large because that is going to effect the speed of the circuit. You should make it just enough so that we get high speed at the same time a good characteristics. This is the inverter circuit using in the DCFL logic family. Once we have the inverter we have to go for other logic circuits. The basic logic circuit in the DCFL is going to be the NOR gate. In the NOR gate we have another device in parallel, this is also like a MOS logic circuit, this is the same thing which we do in case of MOS.

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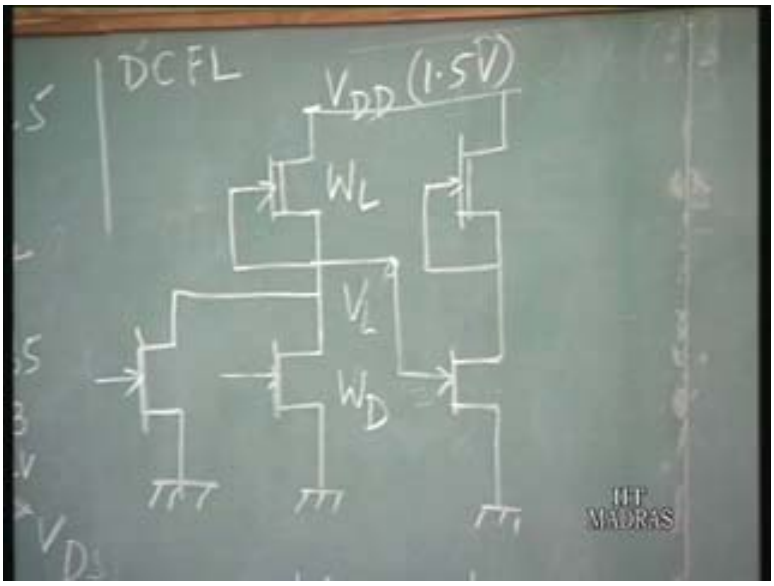

We have another driver transistor in parallel so what happens is when any of these inputs are high that particular transistor is going to conduct and it is going to pull down the output which means that when any input goes high output is low. That is the function of a NOR gate that when any input is high output is low. We may connect a number of input transistors in parallel so if you want a three input NOR gate we have three transistors in parallel and so on. The DCFL logic family is a popular logic family in MESFET logic family. There are many advantages one is of course the simple circuit.

Circuit is very simple, it requires very few transistors as such and it is actually suitable for very large scale integration because of this factor. Also you require a very low power supply voltage just 1.5 volt power supply sufficient because if we look at this curve here, we are only operating in this region that is from 0 to 0.7 volts. We just put 1.5 volts because this transistor must be in a saturation region, the load transistor. If we bring it closer, if you say make it 1 volt then in this region it may not be in the saturation region from zero to 1.7 volt. We just require a power supply voltage sufficiently large so that we have this transistor in the saturation region so the load line actually is almost parallel to the x axis. We just require about 1.5 volt. The low power supply voltage ensures low power dissipation. So you have simple circuit, less number of transistor low power dissipation both of which are important factors in large scale integration.

One problem of course is that you require both enhancement and depletion mode transistors on the same chip which may create problems. You require a superior technology for that but ofcourse technology is something that this people have mastered now and lot of circuits are being in fact made on using this DCFL concept. In fact I will just give you an example in a recent paper, they have referred to a 100 k gate array. That is a gate array which consist of 100 k transistors that is 10 to the power 5

transistors. Such a large number of transistors on a single chip using gallium arsenide technology that is quite remarkable because although for silicon this may not be so great but for gallium arsenide this is quite an achievement. I just give you the features, process 0.5 micron.

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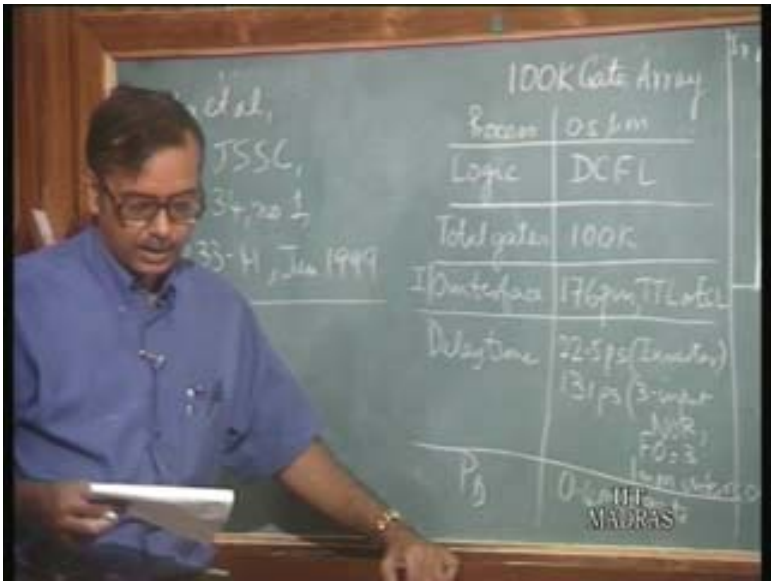

It uses 0.5 micron technology which means that the channel lengths are 0.5 micron, logic DCFL direct coupled FET logic, total gates 100 k which is 10 to the power 5 that is 10000 gates, I/O interface 176 pin TTL or ECL both are available so whether you want TTL or ECL both types of interfaces are available. Delay time 22.5 picoseconds for an inverter and 1131 picoseconds for three input NOR and with fan out of three and one millimeter interconnect. So with all this, the interconnect line is one milli meter long so you have three input NOR gate, fan out is three and one millimeter interconnect line, the delay time is 131 picoseconds.

Finally the power dissipation is 0.4 milli watt per gate. This is a gate array which has been realized using direct coupled FET logic. This shows that direct coupled FET logic is nowadays being seriously thought of as a means of realizing very high speed logic circuits. I just give you the reference also, it is A. Ohta etal, this is IEEE journal of solid state circuits, volume 34, number 1, page 33 to 41 January 1999. This is a recent effort and they have really realized a large scale integrated circuits using DCFL and they have realized lot of circuitry using this gate array.

We have seen that this DCFL is a circuit which can be used for high speed circuits and in fact it has been used to realize high speed circuits and large scale integrated circuits but there is one major problem with DCFL which we shall now look into. When the input goes high then what happens is suppose the input goes low, the output was high.

At this point the output was high. Now when the input goes high, the output is going to go low. For the output to go low what we must have is the output capacitance here which is the input capacitance of this next gate that has to be discharged and the discharge should take place through the driver transistor. The driver transistor must discharge it but the problem here is that the load transistor is always on. The discharge current say $I_{discharge.}$ is actually the driver current minus the load current. That is the load current is always on, so the driver current minus the load current is going to discharge.

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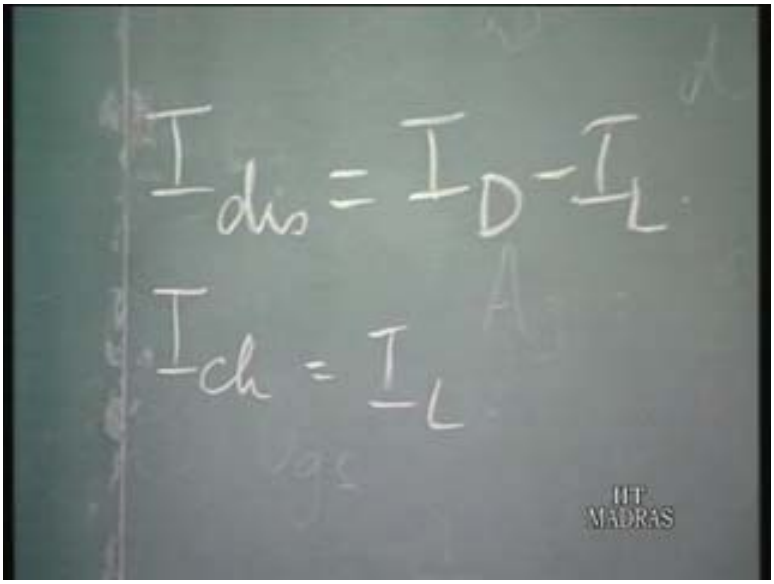

Since the load current is quite appreciable, the discharging current is quite small. On the other hand when you take the other transition that is when the input goes low since the low input is less than the threshold voltage of this device, this device is off. The output capacitance can be charged by the load transistor, the full current goes to charge the load transistor so the charging current is equal to I_L. There is a very large disparity between the on times and off times of this device. The off times that is the time required to discharge the output capacitance is quite large compared to the on time of this. How to improve this? There is another logic family which is actually a derivative of this logic family which can be used to improve the performance. What is done is in that logic family, we have another two enhancement mode devices and the output of the first stage goes as the input here to the input of this enhancement mode device.

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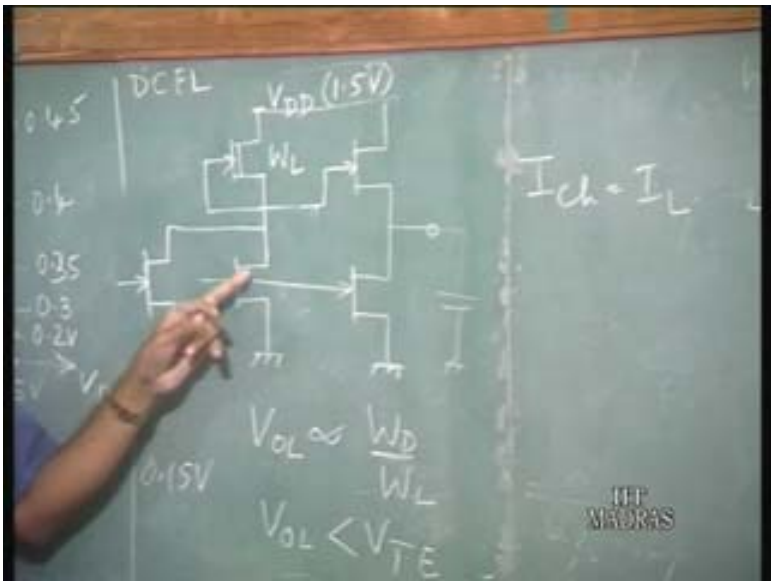

The driver of the two are shorted so this is the output here. Now all this three are enhancement mode devices, we have one depletion mode device. Now if the input is low then both these driver transistors are off. This transistor is on which means that the output goes high which turns on this transistor here, that is the load transistor of the second stage and since this transistor is on, it is going to pull up the output capacitance. Output capacitance, the charging current now is equal to I_L. Now look at the other situation when the input is high. When the input is high, both the lower transistors that the driver transistors are on.

Now this is an inverter, this behaves as an inverter. what is going to happen is this output here is going to go low and as this output goes low, this transistor the load device of the second stage that is going to turn off. In the second stage which is actually driving the capacitance, the load device is off. The discharging current is only the $I_{discharge.}$ is equal to $I_{driver.}$. The charging current is the current of the load device when this is off, the lower device is off and the discharging current is the current of the driver device, the load device is off.

Basically you have a sort of CMOS type of thing where only one device is on and one can achieve an equal rise and fall times. This is called the super buffer FET logic. The name is SBFL, its called the super buffer FET logic. It is a faster logic compared to DCFL because we do not have especially when the output capacitance is discharged we do not have the load transistor on.

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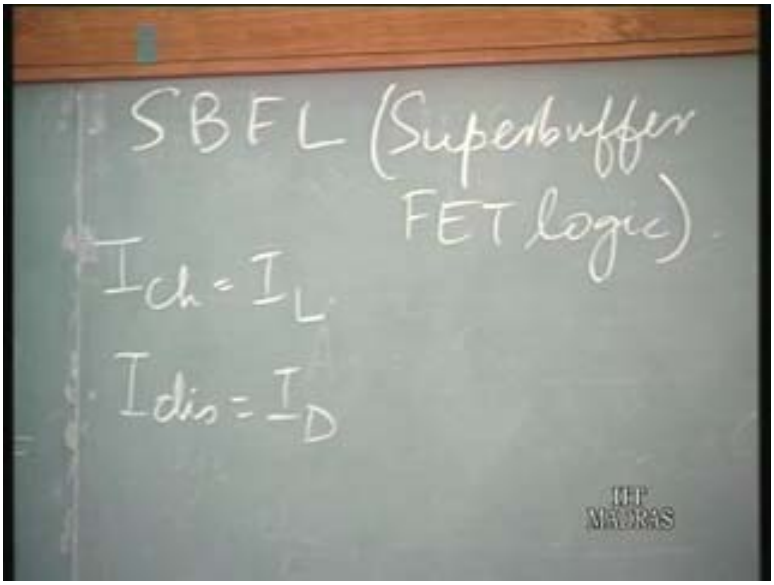

The output capacitance can be discharged fast. This is a faster logic family compared to DCFL but you have to pay in term of extra number of transistors. This is the basic inverter circuit of the SBFL where you have three enhancement mode devices and one depletion mode device, so four transistors make up the inverter. If you want to have a NOR gate basically the circuit what you have is you would have a first stage three input nor gate.

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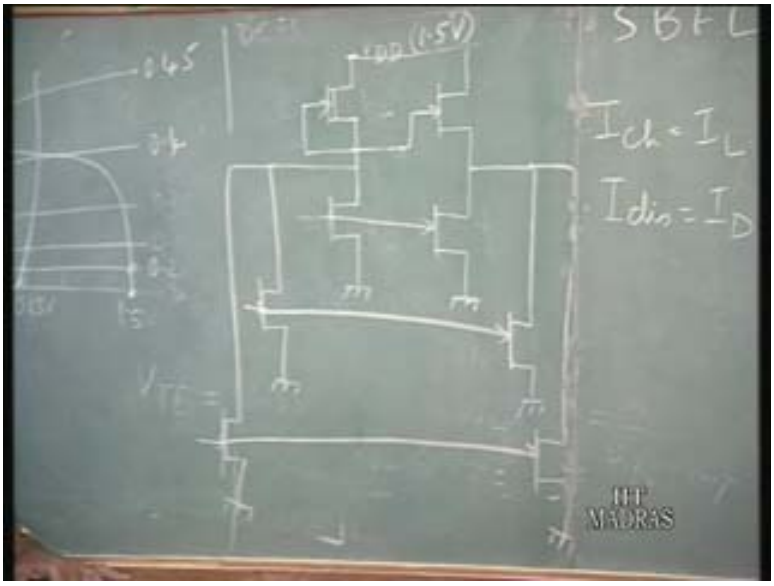

I draw it like this. Now this output of this nor gate is here, the three input nor gate all this three enhancement mode devices, the output of this nor gate goes to here and then you have other transistors in parallel, another MOSFET enhancement mode devices parallel. This is a three input nor gate just like normal DCFL nor gate, three input nor gate and the output is fed here and there is an another nor gate structure here. When any input goes high, the lower part will go off, the lower part will conduct here so that the output goes low this is turned off and similarly there is another transistor here which goes off. It is going to conduct, it is going to discharge the output capacitance where this is off (Refer Slide Time: 49:24).

When all inputs are low then this transistor, the load transistor here turns on which makes this on and all these are off because basically they are the same inputs connected here. The output load can be charged through this load transistor. Basically we have a three input nor gate here, we require eight transistors compared to the four transistors required in the case of DCFL. Again this is going to be a faster logic circuit compared to the DCFL but again we have to pay for it in terms of the number of transistors and this super buffer FET logic is also going to have equal rise and fall times which is not the case in the case of DCFL. We have looked at the two logic families here DCFL and its derivative, the super buffer FET logic we shall consider some other logic circuits in the next class.