Digital Integrated Circuits
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Lecture No # 34
BiCMOS SRAM

In the last class we were discussing CMOS static RAM and we also introduced the concept of BiCMOS static RAM and today we shall continue our same discussion. We had seen that if you take the block diagram of a memory of a CMOS static RAM, when we convert it to BiCMOS static RAM we retain the CMOS.

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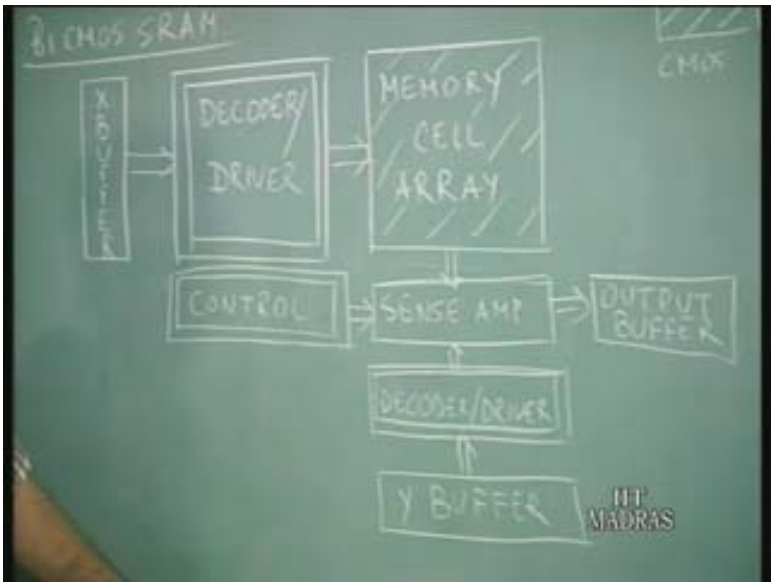

For example in the memory cell array because of the fact that the CMOS is a more dense circuit that is it requires less area, at the same time the power dissipation is less. We would retain the CMOS for the memory cell array, the decoder drivers are BiCMOS because the BiCMOS is capable of driving very large capacitive loads and we have a very large capacitive loads. The word lines and the data lines represent very large capacitive loads.

Then the sense amplifier on the other hand is completely bi polar in the sense that because of the fact that the bi polar transistor has a very large trans conductance and is able to sense very small voltage differences between the data and data bar lines. The buffers here are shown as bi polar because many of these BiCMOS memories have ECL type of inputs which means that the voltage levels are the same as that for an ECL that is you have negative voltages as in an ECL. This must be converted to the levels which are understood by a CMOS circuit because the memory cell is basically CMOS.

What is done is the negative voltages are retained but it is converted to CMOS levels which we shall see in today's class. The control circuit is also BiCMOS in the sense it contains both bi polar and CMOS components and the output buffer because again it is an ECL type of I/O interface. The output buffer is bi polar because the output is an ECL type of voltage levels. With this type of modification, the CMOS memory can be converted to a BiCMOS memory and this gives rise to lot of improvements especially in the speed or the reduction in the access time in the memory that is the delays are very much reduced. Here we show a comparison of the delays of a CMOS and a BiCMOS memory, this is in fact I just give the reference.

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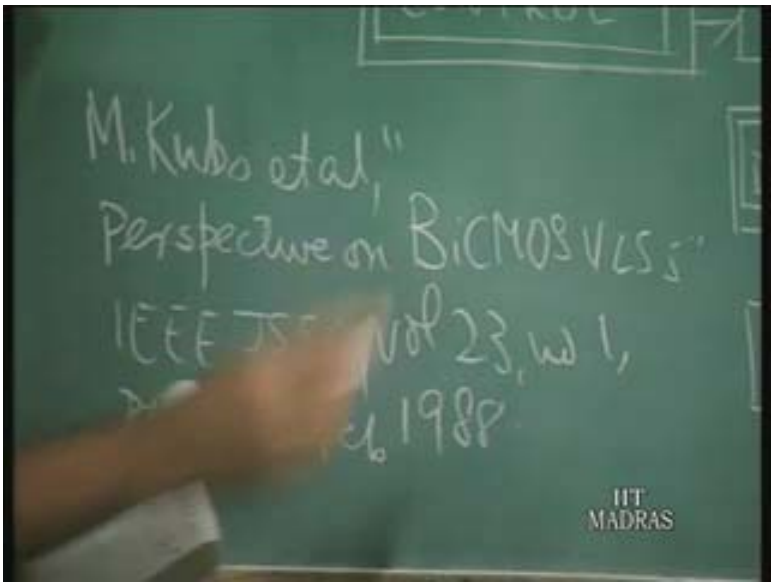

The reference is M. Kubo etal, the name of that paper is perspective on BiCMOS VLSI IEEE journal of solid state circuits, volume 23, number 1, page 5 to 11, February 1988. In that paper what they do is they make a comparison of the delays of the various elements in a memory, they compare the delays of a CMOS memory with that of a BiCMOS memory. The delays can be broken up into different delays through the various regions of the memory.

For example first you have the input buffer, the delay corresponding to an input buffer then you have to decode whatever address has been floated, that address has to be decoded. There is delay for the decoder. Then the output of the decoder must be driven through the memory array that is you require data driver for example the entire word line represents a large capacitance so that you require a driver to change the word line voltages. There is a large delay involved in that and then once you select a particular cell, the contents of that memory cell must be sensed by the sense amplifier. First, you select a memory through the decoders, you select a particular cell then by driving the

word line and then there is a sense amplifier to sense the contents of the memory and then the output of that sense amplifier must go to an output buffer. There is a delay component for that.
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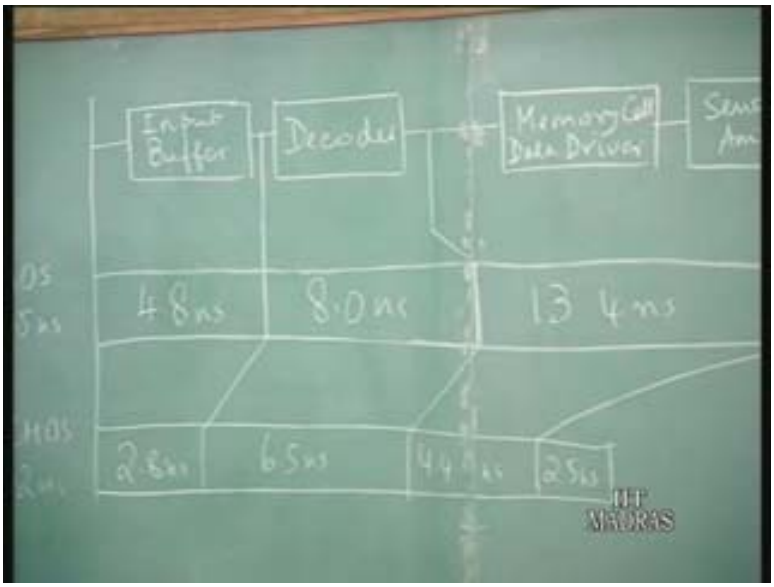

These are the different delay components in the memory. What they have done is they have analyzed the total delay and broken up into different components. For example if you take a CMOS memory, this is for a 2 micron technology (Refer Slide Time: 07:02), it is rather an old technology but at the same time it gives a very good comparison. They do not specify the size of the memory in the paper but anyway let us see. The delays are for a CMOS 4.8 nanosecond at the input buffer, 8 nanosecond for the decoder and the major part of the delay is for the memory cell data driver and sense amplifier. Total of 13.4 nanoseconds and finally the output buffer 2.3 nanoseconds.

If we now compare for a BiCMOS, you find that the input buffer the delay is reduced from 4.8 nanoseconds to 2.8 nanoseconds. The decoder from 8 nanoseconds 6.5 nanoseconds but the major reduction is in the delay for the data driver and sense amplifier. The data driver is now a BiCMOS driver and the sense amplifier is a bi polar sense amplifier. Here the 13.4 nanoseconds for a CMOS is reduced to 4.4 nanoseconds only 4.4 only. There is a major reduction here and the output buffer of course this 2.3 nanoseconds has slightly increased to 2.5 nanoseconds because again the voltage in the case of the BiCMOS, again what happens is you have to convert the CMOS levels to ECL levels. There is a slightly larger delay but if you compare the total delays for the CMOS while it is 28.5 nanoseconds, it has gone down to 16.2 nanoseconds for a BiCMOS.

You see that there is a large reduction in delay, if we convert a CMOS static RAM into a BiCMOS static RAM by making the necessary changes that is by introducing bi polar

transistors judiciously and in different regions. What we shall do in today's class is we shall take up the different components in a BiCMOS memory and see what are the changes that take place or the changes that we must make in the CMOS static RAM in order to improve the performance.

Firstly let us take the memory cell array. In the memory cell array we have said that this is going to be a CMOS just like as in a CMOS static RAM but there is a small difference. In BiCMOS static RAM's, the cell which is used is slightly different from a CMOS static RAM cell. Instead of the normal 6 transistor cell which is used in CMOS static RAM, we have a 4 transistor cell, it is like this. This is the cell which is used, this is the word line, this is the data line. What we see is that the inverter here is not the conventional CMOS inverter that is it does not have a PMOS load but it has a resistive load. You basically have two inverters back to back as in the case of a CMOS cell, 6 transistor cell but what we have is a resistance load. Now this resistance is made of poly silicon and if the undoped poly silicon can have very hi large resistances, in fact these resistances are of values as large as 10 giga ohms. These are very large resistances.

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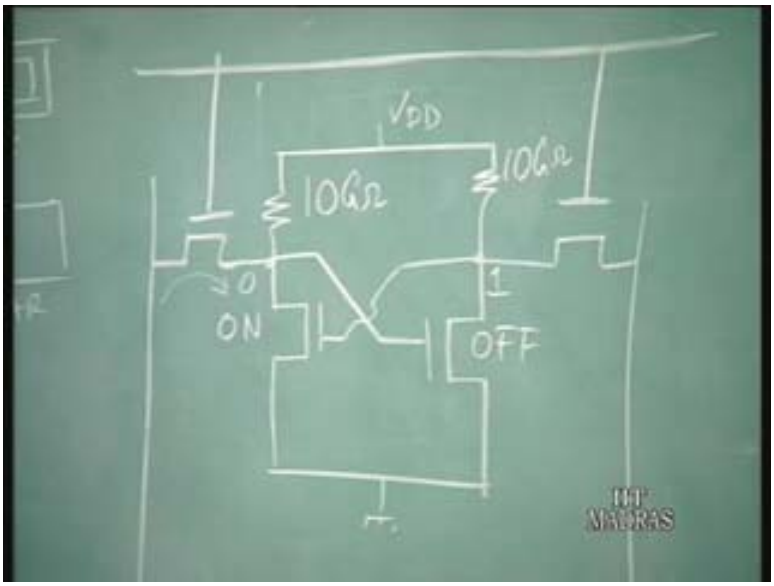

Now if these resistances are very large, the current which flows is going to be extremely small. If you have 10 giga ohm resistance, the currents will be less than nano amperes. Even if you have an inverter like this, the power dissipation is not going to be high. Now the problem with this type of cell would be that since this resistance is very large, a current flows through this resistance. The current is going to be extremely small. If this data line has to be charged to high, the current would be very small it would take an extremely large time. These resistances cannot be depended upon to pull up the data line voltages. What can be done is if you have a particular configuration, this is on this is off. Obviously this is off means this is logic zero and this is off means

this is logic one. This is the inverter, this output of this inverter is zero, this goes here, this is off which means that this is one and this is one, this is one (Refer Slide Time: 12:26). If this is the condition then if this particular cell is selected, since this transistor is on, this helps to discharge this line voltage but this cannot be depended upon to pull up the line voltage backside.

What is done in this case is that the data lines are pre charged to V_{DD} that is the supply voltage, that is the highest voltage in the circuit. One of these lines is going to be pulled to a slightly lower value because of this on transistor. This is connected to an on transistor, this voltage is going to go down by a small amount and this has to be sensed by the sense amplifier. The pre charge voltage in this case is going to be V_{DD} or the highest voltage in the circuit and then in which case one line is going to be pulled down, the other line is not going to be pulled up. You do not depend upon this resistance in fact to pull up. Now what is the advantage of having the cell like this, four transistor cell? Of course what we do is we avoid the use of PMOS transistors and you know that in a CMOS if you have NMOS and PMOS, in order to fabricate them you have to have two tubs, in one you fabricate the NMOS and the other one the PMOS is fabricated, that takes up area.

In fact this large resistances is a poly silicon resistances, these are folded on top of the NMOS transistors. These are fabricated on top of the NMOS transistor. You have the NMOS transistor and on top of that, you have insulator in between and on top of that you have the poly silicon resistance. These poly silicon resistance in fact do not take up any extra area, they are on top of this NMOS themselves. In fact the area requirement for this cell is almost half that of the CMOS cell. There is a tremendous reduction in area which is the advantage of having this four transistor cell. The other thing is that we do not have extra power dissipation because of this very large resistances, the currents are very small.

At the same time the disadvantage one would expect is that because of this very large resistances, it cannot pull up the voltages. We depended upon pull up the output voltages but since that is taken care of by pre charging the data lines to V_{DD}, there is no need to pull up. Only the pull down is done by one of the transistors, on transistor and because of that differential voltage is created which has to be sensed by the sensor. This is about the memory cell. We shall now take up this part, the decoder driver part and see what are the changes, what are the circuitry which is used in BiCMOS static RAM's and basically the modifications with respect to a CMOS static RAM.

Now let us look at the circuits used in BiCMOS static RAM's, the input side. Now as we said that the inputs are basically ECL inputs in that case the logic high would be say minus 0.9 volts and the logic low would be minus 1.7 volts. What is done is these are what are called ECL receivers. What we have is the differential ECL type of stage here. You have a reference voltage here, depending on whether this voltage is high or low, one of these two transistors is going to conduct and there is a current going to

flow through this resistance. The voltage levels on these two lines is going to be different and then what you have is the next stage which is called the level shifting stage which basically converts this ECL levels to the levels which are understood by this circuit which is nothing but a BiCMOS inverter. This is the standard BiCMOS inverter circuit that we have already seen. This is during the level shifting.

Now let us see how this is done. Depending on the voltages here and this reference voltage is chosen properly then the current flows in either of these two branches. Suppose output voltage let us call this v_{high} and the other one is v_{low} at the two collectors. If v_{hi} that is the high voltage is when there is no current flowing through this resistance here. What is the output voltage here? V_{hi}, it is this is ground and this is minus v_{ee} as in the case of ECL. This is minus 5.2 volts which is the standard voltage for ECL and this side is at ground.

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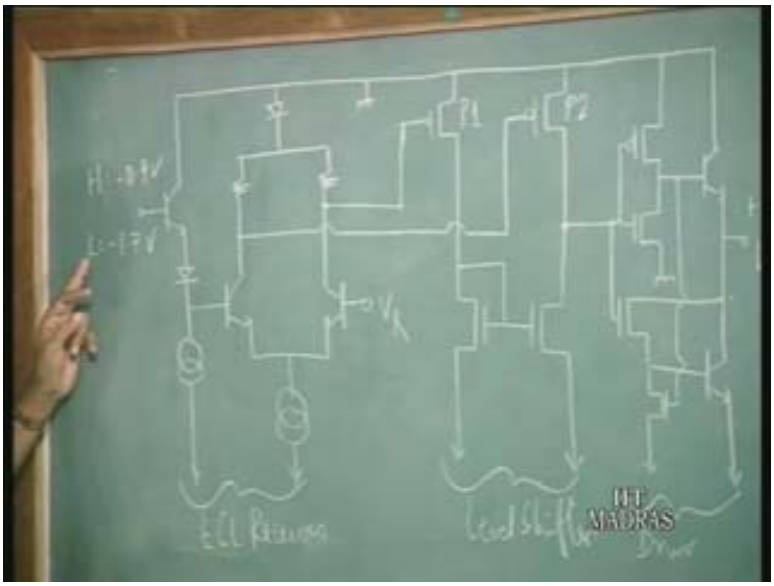

Now you have a diode drop here, there is no current flowing here, v_{hi} can be said which is equal to minus v_{be} which is the diode drop and v_{low} will be minus v_{be} minus $I_E R_C$ where R_C is this resistance value, I_E is actually the value of this current source here. I_E, the entire current flows through this resistance, the drop here is $I_E R_C$. This is now fed at the gate of this PMOS transistor. This one PMOS transistor has a gate to source voltage of minus v_{be} and the other PMOS transistor has a gate to source voltage of minus v_{be} minus I_E R_C. Now if the threshold voltage of the PMOS transistor lies between that is the modulus of that lies between v_{be} and v_{be} plus $I_E R_C$.

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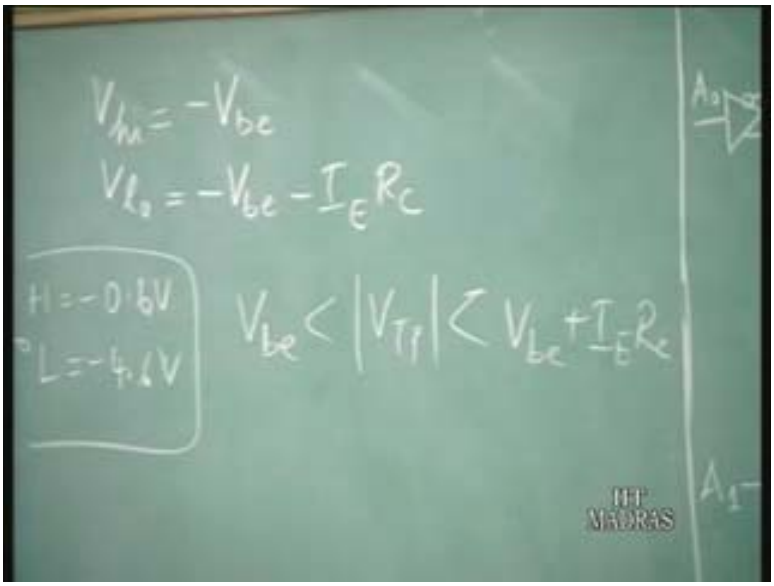

Then what is going to happen? One of this PMOS transistors is going to be on that is conducting and the other one is going to be off. One branch again in this level shifting, one is going to conduct and the other one is going to be off. Now this circuit if you look at it closely, this two NMOS transistors here is in a current mirror type of configuration because both gate voltages of these transistor are the same and also the sources are at the same potential. Now if we consider this current here which is flowing out of this level shifting stages I_{load}, this I_{load} can be written as I_{p2} that is this transistor, this is this current minus this current which we call the current mirror, I_{CM} current mirror. That is the I_{load} that is the current flowing here. This I_{CM} because of this current mirror configuration, this is nothing but the same as I_{p1} because this current is the same as this and the current flowing through this NMOS transistor here is the same as the current flowing through this PMOS transistor P_1.

You can write I_{load} is equal to I_{p2} - I_{p1}. There is a current flowing out here, this is the charging current for the input capacitance of the BiCMOS inverter. This current is

actually the difference of I_{p2} and I_{p1}, I_{p2} - I_{p1}. Now as we have already said there can be two possible cases that is either p1 on and p2 off or p1 off and p2 on. In one case if p2 is on and p1 is off, this I_{load} is going to be positive and the other case if P_1 is on and P_2 is off, I_{load} is going to be negative. If I_{load} is positive that is basically a current flows into the input of this BiCMOS inverter, it charges the input capacitance so that basically logic high at the input, the output is going to be low.

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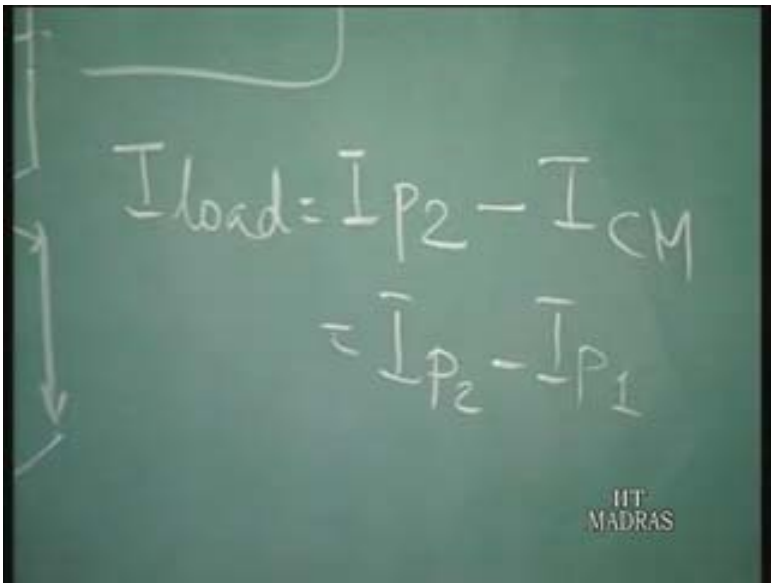

On the other hand if the I_{load} is negative that is basically discharging the input capacitance of the BiCMOS inverter then what happens is this input constitutes as a logic low which means that the output is going to be taken as a logic high. Depending on whether this input is high or low, the current is going to flow in one of these two branches, it makes one side high and the other side low. Again depending on the input, one side will be high and one side will be low. Depending on that either p1 will be on or p2 will be on, the other transistor will be off and depending on that the load current is either going to flow into the input I mean there is going to be a current flowing out which is charging or discharging the input depending on that the output is going to be high or low.

The important point here is that the input here is ECL level whereas here, the current flowing in here charges the input capacitance here. This is a bi polar CMOS inverter.

The output level which you get here is minus as in the case of BiCMOS, there is a V_{be} drop from the logic. This is minus 5.2 here and 0 here, you get minus 0.6 and minus 4.6. High will be minus 0.6, low will be minus 4.6. Basically we convert the ECL level to BiCMOS level. This is basically CMOS level except that it has been level shifted down to negative values. Now once this is done then you can use normal BiCMOS circuits to do the decoding operation. The decoding operation can be done by using normal BiCMOS circuits.

This is one way in a BiCMOS static RAM which uses ECL levels that is you first convert it to BiCMOS levels and then follow it up with BiCMOS circuitry to do all the logic operation needed for decoding as well as for driving through the word line capacitances, we use BiCMOS drivers. This is one way which people have employed in BiCMOS static RAM's.

Another way I shall now talk is another decoding mechanism which uses a different concept. Again the inputs are in ECL level. What is done is first we have say ECL or nor circuit, you know that ECL gates you can have the same output as well as the complement. Basically this is $A_{0.}$. That is you get at the output $A_{0.}$ as well as $A_{0.}$ bar and you know that this is basically the emitter follower which is at the output of the ECL inverter. These are basically ECL gates here, you have ECL gates and this is the emitter followed at the output of the ECL gates. Now we know that the output of the ECL gates because you have emitter followers, you can do a wired operation. You can get logic by doing the wired operation.

For example here what you have is this is $A_{0.}$ bar, we just draw a circuit which takes a two input decoder basically we will have 2 outputs, 2 2 by 4 decoder. These are both $A_{0.}$ bar's and here you have $A_{0.}$ and $A_{0.}$. This is the emitter followers, this multi emitter transistor at the output of ECL whereas here you have $A_{1.}$ bar, $A_{1.}$ bar, $A_{1.}$ and $A_{1.}$. Now what you do is if you take this line, $A_{0.}$ bar and $A_{1.}$ bar is connected here. This is nothing but an OR of $A_{1.}$ bar and $A_{0.}$ bar then here in this line, you connect $A_{0.}$ bar and $A_{1.}$. This is an OR of $A_{0.}$ bar and $A_{1.}$. In this line you have $A_{0.}$ or $A_{1.}$ bar, here you have $A_{0.}$ or $A_{1.}$.

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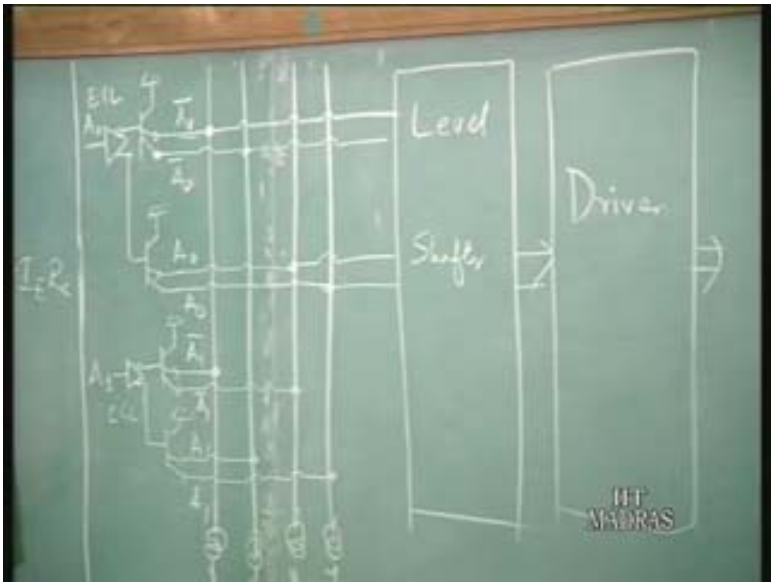

Basically you have all the four combinations, just by doing a wired operation you do the decoding. You have a 2 to 4 decoder, this decoding is done at the ECL level only. It can be done very simply because the ECL you can do a wired operation. This decoder can be realized very simply by doing a wired operation. Here we have current sources of course going to ground. This is a wired operation and then what you do is you do the same thing as you have done in the previous case. Each of these outputs of the decoders are level shifted and using a BiCMOS driver, you drive the memory word lines.

The difference in the two circuits is in one case what you do is you convert the ECL levels to BiCMOS level and then you do the decoding at the BiCMOS levels. The voltage levels of the decoder is the BiCMOS level, you do the decoding using BiCMOS gates. On the other hand what you can do is at the ECL level itself using the property of ECL that you can do a wired operation. You do the decoding itself, you have a 2 to 4 decoder, you have 4 outputs here. You have two inputs, you have four outputs and then each of these four outputs, you have to do a level shifting and then a driver to drive it through the memory cell array. These are the different types of circuits which are used at the input of the BiCMOS static RAM.

The important point here is although at the input you have ECL levels, at the output of the driver you have basically CMOS levels except that it is negative. Voltages are driven negative, it is level shifted down. There is a level shift to a negative values but the voltage levels are still the same as in a CMOS. You have a complete 5 volt, almost a 5 volt if you are operating 5 volts. 3.3 volts if you are operating you will have a 3.3 volt almost a 3.3 volt difference between the high and low logic levels. You can use all the voltage levels shifted down to negative values by the same amount, you can get

basically same CMOS operation but again one must again revert back to ECL levels at the output stage.

Next what we shall do is we shall look at a complete circuit or basically this is the input circuit then the remainder of the circuit we shall look at a circuit for a static RAM and look at how one can read and write in a BiCMOS static RAM. Now let us take up for discussion a particular circuit for a BiCMOS static RAM. Different groups have people of all companies, they have different circuits for BiCMOS static RAM. I have just taken one representative circuit which is from literature and let us just discuss this particular circuit and see how the circuit actually functions.

This circuit which I am going to discuss now is actually taken from this particular paper R.A. kertis etal, 12 nanosecond ECL I/O, 256 k into 1 bit SRAM using a one micron BiCMOS technology. It is from IEEE journal of solid state circuits, volume 23, page 1048-1053, October 1988.

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This is just one of the representative circuits and we shall just go through it, how the reading, writing and different operations are taking place in a particular BiCMOS static RAM. Now as we have seen this is a 256 k into 1 bit static RAM, 256 k static RAM means that there will be 256 k cells. 256 k is actually 2 to the power 18, there will be 2 to the power 18 cells and one has to select one out of 2 to the power 18 cells. If you have 2 to the power 18 cells, there will be 18 address inputs and with the help of this 18 address inputs, one has to select a particular cell.

Let us look at how this is done. What is done is you have columns again just as in any memory cell, you have columns in which we have the cells. In each column there are 128 cells, $x_{0.}$ to $x_{127.}$ here. Each column will have 128 cells. If you have 128 which is 2 to the power 7. If you have 2 to the power 7 cells per column, this is again the four transistor two resistance cell which we have already discussed. If you have 2 to the power 7 cells, there must be 2 to the power 11 columns. What is done, you have a particular decoder which is a 7 to 128 decoder which selects one cell in each of these columns. Now to select one of the 2 to the power 7 columns what is done, you have another two decoders not one decoder but two decoders. What is done is this 2 to the power 11 columns is now divided into two groups, each group consisting of 16 columns.

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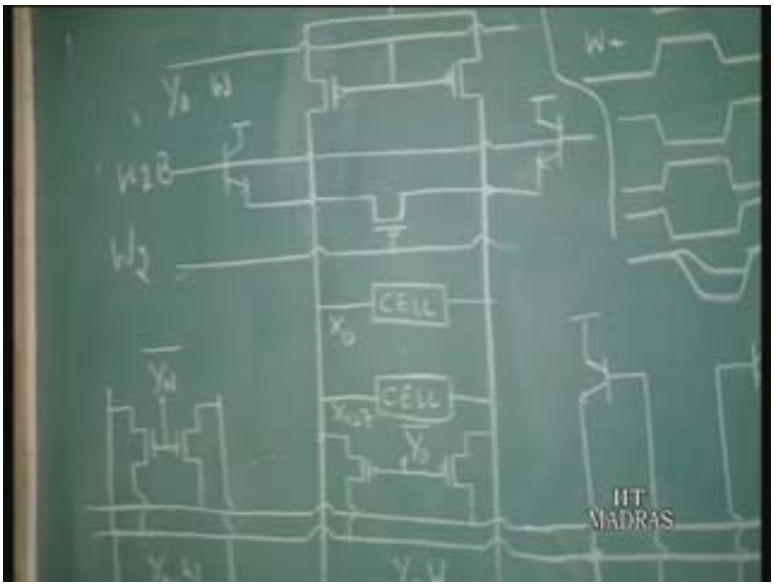

What is done is each of the 16 columns that is 2 to the power 4 columns constitute a group. You have another decoder which is a 4 to 16 decoder which selects one column in each group and then basically you select one cell in each column by one decoder and then you select one column in each group and then you have another decoder, a third decoder which selects one group out of the 2 to the power 7 groups. Basically you have a three dimensional decoding that is you have three decoders for selecting the particular cell. One decoder selects one cell in each column and another decoder selects one column in each of these groups, 2 to the power 7 groups and another decoder selects one particular group so that finally you have selected one particular cell.

Now let us see how this functions? This is the circuit of one column, this is how one column is going to look. Now internally as we said it is a BiCMOS levels, this is a negative voltages as in a BiCMOS memory. $V_{cc.}$ would be actually ground and the negative voltage would be actually minus. Now for reading operation what is done is while you are reading a particular cell then these PMOS transistors here are on. This is on for a reading operation and these transistors actually form the load for these cells. This form a low resistance load for these cells. While we are reading what happens is once we select the cell, these PMOS transistors are on and since we have a very low resistance load, it creates a differential voltage of around 90 milli volts only on these two lines. A small differential voltage of 90 milli volts is only created on these lines and these bi polar transistors are off during reading operation. This 90 milli volts load is differential which has to be sensed.

What is done is this is $y_{0.}$ bar, if this particular column is to be sensed this line goes low so these PMOS transistors are on and this particular difference voltage is available on

these two lines this 90 milli volt differential voltage, when a particular cell is selected. Again here basically y_0 to y_n these are in a particular group, these columns form a particular group. One of these particular columns is going to be selected they are all on these line. On this line you have the difference voltage corresponding to the column in that particular group which is selected and this 90 milli voltage is available here. This part of the circuit is off I will explain later on. This is basically used for writing operation, this part of the circuit (Refer Slide Time: 35:22). This 90 milli volt differential voltage is available here at this point now. These are nothing but emitter followers and then this goes to the input of a differential amplifier.

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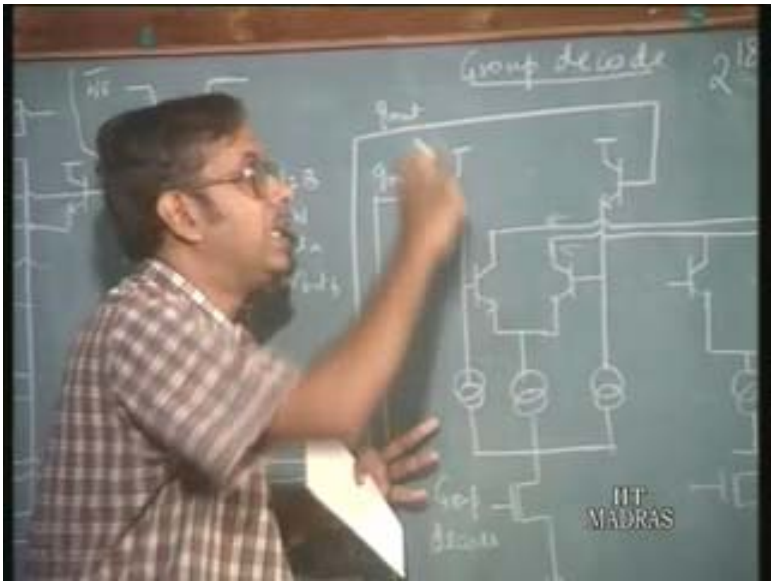

At the input of these differential amplifier these two transistors, the input base voltages they have difference of only 90 milli volts but we have already seen when studying ECL gates that the 90 milli volts difference between the base voltages is sufficient to create a large difference in collector currents. What happens is because of this small difference voltage, one of this transistors is going to get a large current, the other transistor is going to be practically off. There is going to be a large difference in the collector currents of these two transistors. These difference in collector current must be sensed.

Now what happens is this is the sense, we are also doing a group decode, this output which you have is corresponding to a particular group of columns. You have 2 to the power 11 similar groups, this is the output say of another group similar to this and all of them are connected, the collectors of all of them are connected to the same pair of lines here. Now here if you look at this circuits, for this particular differential amplifier here you have a NMOS transistor. Only when this NMOS transistor is on, a current can flow. What happens is you have 2 to the power 11 such groups here and another output

of the decoder is going to select only one out of this 2 to the power 11 differential amplifiers. Only of this 2 to the power 11 differential amplifiers is going to be on.

Although you have a voltage difference at the bases of these two transistors for all these transistors but only one of these differential amplifiers is going to conduct. Basically you select one out of the 2 to the power 11 groups. The current flowing, the difference is actually corresponding to one of the 2 to the power 11 groups and in that group one column and in that column one particular cell. We basically have the information corresponding to the particular cell we have chosen available on these parallel lines.

Now let us come to this part which is the final sense. We have the difference in current which we have to convert into output voltage. Now what happens is if you look at this particular circuit, this is the very interesting circuit, now what happens is there may be a current flowing $I_{c.}$ here which is the collector current of the differential amplifier stage we have already seen. Now this is a fixed current $I_{0.}$, the emitter current of this bi polar transistor here is actually $I_{c.}$ plus $I_{0.}$. Now the $v_{.be.}$, the base emitter voltage of this bi polar transistor is actually related to $I_{c.}$ plus $I_{0.}$ to the current flowing. If the current is small, the base emitter is almost zero then the base emitter voltage is also going to be very small but if the current is appreciable then the base emitter voltage raises. What happens is if you look at the output of this differential amplifier stage, between the two lines only one line is going to carry appreciable current, the other line is not going to carry current.

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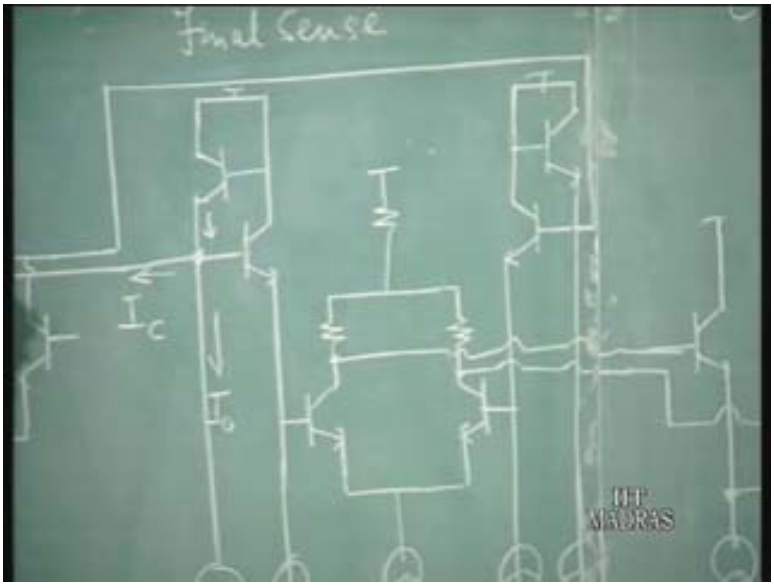

If you look between these two transistor what happens is they are identical. What is going to happen is in one case the emitter current of this is I_0 plus I_c and the other case it is only I_0 because I_c is almost zero. There is going to be a difference in the base emitter voltages of these two transistors and that is what is sensed. What you have is this v_{be} the difference actually, this is v_{cc} say v_{cc} minus v_{be} and then you have an emitter follower. This is nothing but an emitter follower, this is again fed at the base of this differential amplifier.

What you have is here the base voltage depends on the v_{be} drop of this transistor and the base voltage here depends on the v_{be} of this transistor. You have a difference in voltage here between the two base voltages which is then sensed because this is the differential amplifier, any difference in base voltage will result in a difference in current. This is nothing but an ECL stage, what you have is again going to be a difference voltage here between the two collectors which is then again followed up. This is the output buffer basically in the next stage. This is an emitter followers again from the previous stage and then which is fed again through the differential amplifier stage or an ECL stage as whatever you call it and the two voltages are here. Basically you just require single ended output, this output is going to be fed here so whatever information you have is then available at the output.

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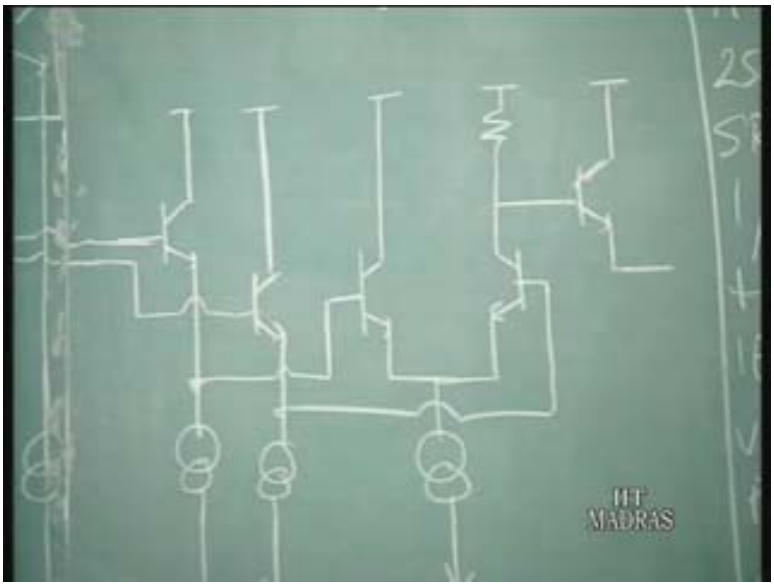

That is how the reading is done. You particularly select one particular cell and that information is passed on to the output. The important point here is that between the two lines, with the help of these NMOS transistors are basically low load resistor, you create a very small differential voltage between the two line, only 90 milli volts. It is very fast because although you have a large data line capacitance, the change in voltage

is extremely small that makes it very fast. Now about the writing operation. While the writing operation is done what happens is this PMOS transistors are all off during the writing operation. Now what happens is the input for the writing operation is from the data lines, you have data and data bar. Normally these would be both high.

Now what is done is one of these lines is going to be pulled down to write either a 1 or 0. Suppose this data line is pulled low, what happens is this goes low, this is available here this is $y_{0.}$ into w, w means write, so the AND of the column select and the write (Refer Slide Time: 42:23). This is selected while writing, this information is available. The zero voltage is available on this line. Now this other line is high. What is the need of this part of the circuit I will just explain. If this line goes low what happens is this PMOS transistor turns on because the gate voltage turns low and so this bi polar transistor turns on.

The other line is $v_{cc.}$ high, there is going to be a $v_{be.}$ drop across this transistor and this emitter voltage of this bi polar transistor is going to be nothing but $v_{cc.}$ minus $v_{be.}$. This voltage is available through this pass transistor on the other line. While you are writing what you do is one of the lines is pulled to low and the other line simultaneously is pulled to $v_{cc.}$ minus $v_{be.}$. This is shown here, I will just amplify it a little bit. While writing what happens is one of the lines go low and the other line is pulled to $v_{cc.}$ minus $v_{be.}$. Why is this, we will see that. As on as the write cycle is over what happens is this data line goes high and then this bi polar transistor are turned on. These two bipolar transistors here would be turned on after the write cycle is over. This is write bar, once the write cycle is over, these transistors turn on and these bipolar transistor helps to pull up the output voltage, pull up the data line voltages.

What happens is this voltage here which are gone low is going to be pulled up very fast by the use of this bipolar transistors and then what happens is the bipolar transistor can only pull it up to $v_{cc.}$ minus vbe because once this line goes to $v_{cc.}$ minus $v_{be.}$ and since the base voltage is $v_{cc.}$ then this bipolar transistor can no longer pull it up because it turns off. Then finally this output voltage is going to rise slowly because after the write cycle this PMOS transistors turn on and then both the line voltages are pulled slowly towards $v_{cc.}$, they move like this. One of the lines is pulled low, the other line is also pulled to $v_{cc.}$ minus vbe. The reason being is that if this was not pulled to $v_{cc.}$ minus $v_{be.}$, the other line remaining like this. One line rises sharply to $v_{cc.}$ minus $v_{be.}$, this is $v_{cc.}$. Now there would still be a difference in voltage of $v_{be.}$ between the two line voltages.

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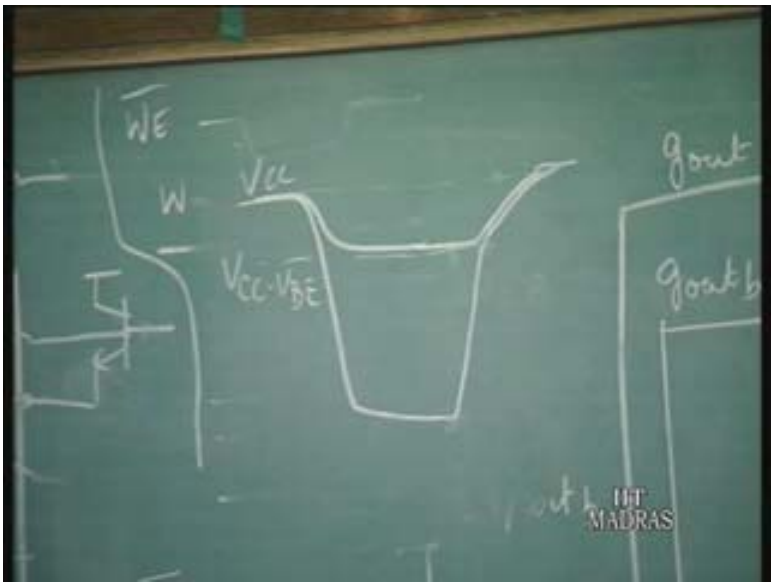

If there is a difference in voltage between the two line voltages, the circuit is not ready for a read operation. For the circuit to be ready for a read operation, the two line voltages must be equalized because we remember that when we are reading, we are actually sensing a small ninety milli volt differential voltage. For that the two line voltages must be equalized very quickly. That is why the other line voltage is also pulled down to v_{cc} minus vbe. Once this line goes to vcc minus vbe, both the lines are equalized and then although both are not equal to v_{cc}, they are rising slowly but both the lines have equal voltage, it is ready for a read operation.

It is ready for a read operation at this instant only. That is a reason why, the other line is going to be pulled down. Basically what happens is while writing, we force one line to the lower potential in this circuit minus v_{ee} and the other line close to v_{cc}. Basically with that we write into the cell, we turn one of the NMOS transistors on and the other NMOS transistor off in that particular cell which is selected by the x decoder. That is

the write operation in this particular memory. Once the write of cycle is over, now the PMOS transistors are on and this particular transistor is there in equalizing the voltages. This PMOS transistors are on and the circuit is ready for a read operation or another write operation. This is how BiCMOS SRAM circuit looks like.

Basically you have this cells which are four transistor cells. These are pre charged to v_{cc}, in this case of course v_{cc} is zero volts and v_{ee} would be minus this 4.8 or whatever. This cell which is a four transistor cell in which one of the transistors would turn on to reduce the voltage slightly because this is a four transistor cell not a six transistor cell. That creates a small difference voltage which is basically being sensed. This is just to give you a flavor of the type of circuit used in BiCMOS static RAM. You have first ECL input which is converted to a BiCMOS levels basically, although the voltage levels are negative. Then with that you select a particular cell, in this case you have a three level decoding and then the sensing is done by bipolar, the small difference is created, only a small difference volts 90 milli volts that makes it so fast. Then this 90 milli volts is then fed to the base of two differential amplifier which creates a difference current which is then sensed, this difference current creates a difference in v_{be} of the two transistors which is then finally sensed and again convert it to ECL level.

This is a circuit of a BiCMOS static RAM and as I said the BiCMOS static RAM is going to be much faster than CMOS static RAM because of these properties. Only a small difference voltage on the data lines is necessary and we are using a bipolar sense amplifier to sense the small voltage. That brings us to the conclusion on this section in static RAM's. Next class we shall actually take up another form of memory which is the dynamic RAM.