Digital Integrated Circuits

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Lecture No # 29

BiCMOS gates

In the last few classes we have looked at the CMOS logic circuit and some of its variations or efforts to improve the performance of a CMOS circuits. Today's class we shall again look at another variation of the CMOS circuit. Now before going into that let us first look at the advantage of a CMOS gate in comparison with other logic families in the MOS family. The CMOS as we know, the major advantage is that it has a zero static power dissipation. That is because under static conditions when the NMOS is on, the PMOS is off and when the PMOS is on, the NMOS is off. So there is no actual current flowing from the supply to the ground. The static power dissipation is zero. The power dissipation only occurs when the output is switched from one level to the other, from output high to output low or from low to high. So that is a hallmark of the good circuit that is the power dissipation, the power is mostly consumed in switching and there is no wastage of power in the static condition.

CMOS also has another advantage that is the output low is not determined by the sizes of the transistor. That is it is basically a non ratio logic in the sense that the output low does not really depend upon the ratios or the widths of the individual transistors which is true in the case of other logic MOS logic families because for example in the logic family with a depletion mode load, the load transistor is always on. The output low will be determined by the widths of the individual transistors. This is not the case in the case of CMOS. So in fact one can use a small dimension, one can use the minimum size transistors because the output voltage is not really determined by the sizes of that individual transistor which of course results in a saving area. That is one of the advantages of CMOS when compared to other logic families.

Now another advantage would be while switching, when the output is to be charged say we have an output capacitance and the output voltage has to switch from low to high that is the output capacitance has to be charged. Then what happens is the NMOS transistor is off and the PMOS is on and the current flows through the PMOS to charge the output capacitance.

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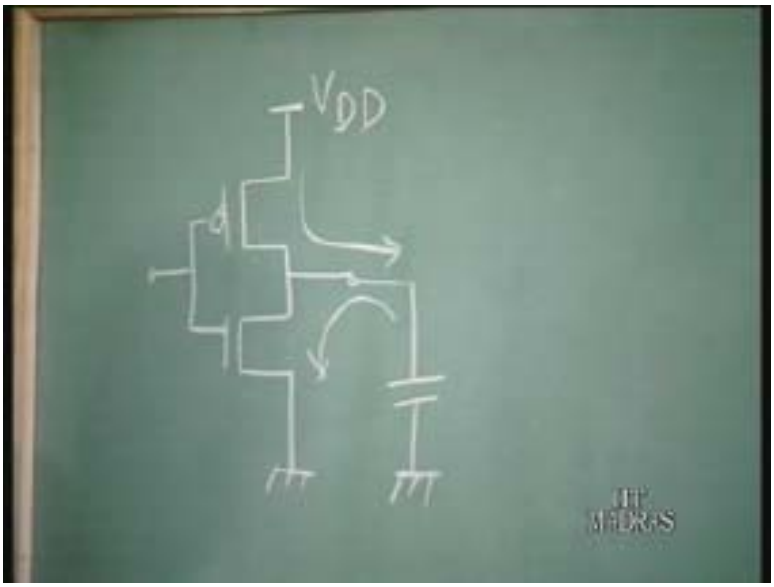

In this case since the NMOS is on, the entire PMOS current can be used to drive the output capacitance. On the other hand when the output has to go from a high to low that is this output capacitance has to be discharged then what happens is that the PMOS is off, the NMOS is on and the entire NMOS current can be used to discharge the output capacitance. Since the PMOS is off, which is not the case of other logic families like again the NMOS logic families where the load transistor would always be on with the result that the current which is discharging the capacitance is the difference of the currents of the driver transistor and the load transistor.

This is a major advantage of course here one must also point out that since the dimension of the NMOS and the PMOS transistors are the same then the PMOS would have a lower current because of the lower mobility of holes. In fact if one has to go for equal on and off times then one has to increase the width of the PMOS transistor but that is a small disadvantage. The major advantages in the case of a NMOS is that you have zero static power dissipation and also we can have almost minimum size transistors and also while switching on and off, since the two currents do not clash, one can have fast switching also. Even with these advantages and also acknowledging the fact that the CMOS has been the main stay of the VLSI for a long time, this is not the ultimate circuit in the sense that there is also a lot of improvements which can take place.

For example CMOS is not the fastest logic family. The fastest logic families are still the bi polar logic family that is the ECL and the main reason for this is that for the bi polar transistor the trans conductance is the highest. The bi polar transistor has a much higher

trans conductance than MOS transistors because of the exponential relation of the output current with the input voltage. So that is a major advantage of the bi polar transistors and also the current drive capability or bi polar transistors is more than that of the MOS counter parts. If one has to drive a large current, one would prefer to use the bi polar transistor because if one has to drive the same current with a MOS transistor, one would require a huge size transistor which would take up a lot of area. Basically the bi polar transistor have certain inherent advantages that is the higher trans conductance as well as larger current drive capabilities which also makes them very highly suitable for high speed logic circuits. On the one hand we have the advantage of CMOS that is zero static power dissipation and some other advantages.

On the other hand we have the bi polar transistors which have certain advantages like being a high speed logic family, by being a high speed device in the sense you have a higher trans conductance. Now if we can have a logic family which derives the advantages of both that is we have on the one hand logic family which has a zero static power dissipation and on the other hand it has a very high current drive capability that is it can drive large currents to charge and discharge the output capacitances. Then of course using the bi polar transistor then of course it would be sort of best of the both worlds. so that is what is attempted in the bi CMOS logic family which is basically a CMOS circuit which includes bi polar transistors in the driving part where use a bi polar transistor to drive large output currents and this is used to speed up the circuit and give better performance.

So we shall discuss this bi CMOS logic circuit in today's class. Let us look at the bi CMOS inverter. What you have is a PMOS is driving a bi polar transistor and then you have an NMOS which also drives another bi polar transistor and this is the input here and you have the output here, this is applied voltage. So you have V_{in} and we have V_{out}. So the input side it is like a CMOS, you have a PMOS and a NMOS which are shorted and connected to the input.

Now what happens is when the input is low say zero volts, this NMOS will be off and the PMOS will be on. Now when the PMOS is on, a current will flow in this direction and this current forms the base current of the bi polar transistor. So if the PMOS current is I_D if you say then the base current of the bi polar transistor is I_D. You would have an output current beta plus one times because the output current is actually the emitter current of the bi polar transistor. So beta plus one times ID that is the current which flows and is going to charge the output capacitances. On the other hand since the NMOS is off then the base current of this lower bi polar transistor is zero, so this lower bi polar transistor is off. So it is not conducting.

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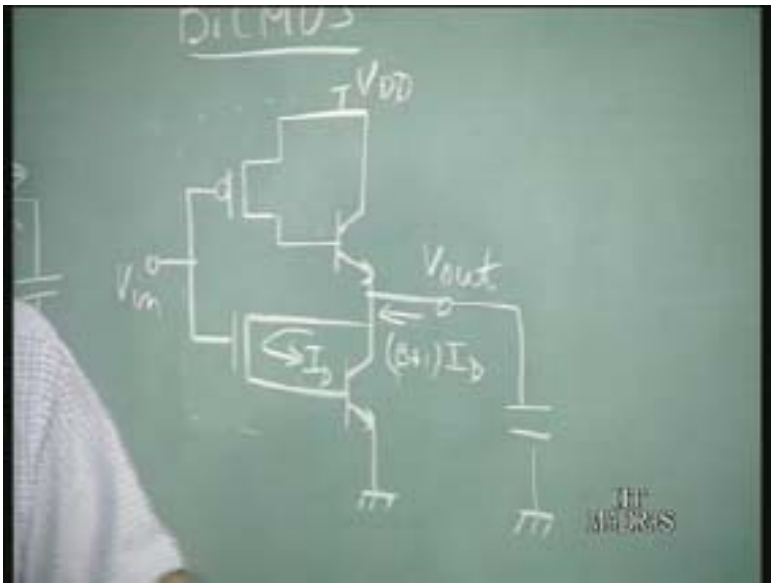

So when the upper bi polar transistor is conducting, the lower bi polar transistor is not conducting. Basically once this output capacitance is charged then there will be no current flowing because although the upper transistor would be in a conducting state, the lower transistor is off and so there would be no static current flowing in this logic gate. On the other hand if you look at the other situation, when the input is high say V_{DD} then you have a high gate voltage for the NMOS transistor here. So this NMOS transistor is on whereas this PMOS transistor is off. Now since this NMOS transistor is on, a current would flow in this direction. Again this current is going to be the base current of this bi polar transistor and since we have a current I_D which is actually the drain current of the of the MOS device.

If the base current of the bi polar transistor is I_D then the total current which is flowing, which is actually going to be in this direction now that is the total current is the sum of the collector current of this bi polar transistor plus the drain current of this MOS. So that is going to be beta plus one times I_D again but it would flow in the opposite direction and it would help to discharge the output capacitance. When the NMOS transistor turns on, a current would tend to flow in a direction which discharges the output capacitance. The discharging current is now beta plus one times I_D. On the other hand since this PMOS transistor is now off because you have a high input, the PMOS

transistor is off then there is no base current for upper bi polar transistor here. So this upper bi polar transistor is going to be off.

So when the lower bi polar transistor is on, the upper bi polar transistor is off. So again in the steady state you would have no static power dissipation. Once the output capacitance is discharge then no further current would be flowing. Because although the lower transistor is in a conducting state, the upper transistor is in a non conducting state.

If you look at the circuit, it retains the advantages of the CMOS in the sense that again when the upper half is conducting, the lower half is off and when the lower half is conducting, the upper half is on. So both upper half and lower half are never on simultaneously in the steady state. So the static power dissipation is zero. On the other hand if you look at the advantages compared with CMOS, we find that the charging and discharging currents are now beta plus one times ID whereas in the case of a CMOS the current which was driving the output capacitances, the charging or discharging the output capacitance was only ID.

We have a gain of beta plus one, although this circuit retains the advantages of the CMOS, it has an additional gain of beta plus one. Since we are now charging and discharging the output capacitances with higher current, the time required to charge or discharge the capacitance would be less in the sense that the operation would be speeded up. So this is going to operate at a much higher speed than the corresponding CMOS.

If you look at the delay curves of the CMOS and the bi CMOS, if you plot the delay, this is the say delay and you have the load capacitance. Now for a CMOS, if it goes like this, we know that the current you can write I is equal to C dV dT so delta V is the logics swing and the time is delta T for the output capacitance to change by delta V and if this of course assumes a constant current is used to charge or discharge the capacitance. So we can write td is equal to C delta V by I.

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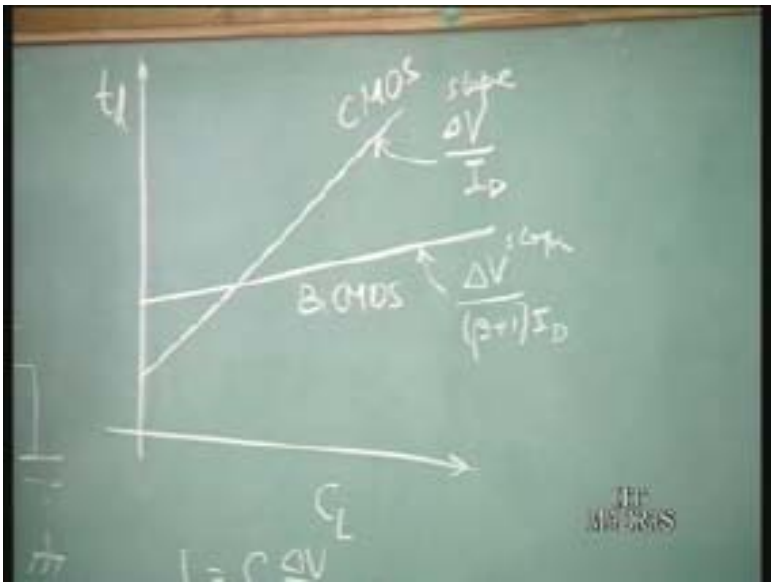

So the slope of this curve is going to be delta V which is the logic swing by I. Now this is for the CMOS whereas for a bi CMOS what we have now is this current which is the current for the ID, if we call the drain current in the case of CMOS, this is a drain currents which are used to drive the capacitances.

Now for a bi CMOS since the current which is now charging or discharging the capacitances is beta plus one times ID, you have a curve like this. This is the slope, the slope of the curve is going to be reduced. So you have delta V by beta plus one ID, this is the slope for the bi CMOS curve. So we see that for the bi CMOS even with a large change in capacitance, the delay does not change by much whereas in the case of CMOS, if you are driving a large capacitance the delay changes much.

Of course initially for very low capacitance the bi CMOS may have a slightly higher delay because of the fact that you are introducing additional components in a bi CMOS but especially for larger capacitances because of the fact that the delays almost flat, for larger capacitances the bi CMOS will be operating with the much lesser delay compared to the corresponding the CMOS. So that is the advantage of bi CMOS compared to the CMOS. There is a small disadvantage which we shall also point out here and we shall discuss in detail some time later.

The disadvantage in this case for the bi CMOS is that when the output voltage for example when we are charging the output capacitance and when the PMOS is on, this bi polar transistor gets a base drive, the output capacitance is getting charged, the output voltage raises but once the output voltage raises to V_{DD} minus V_{BE}, when the output voltage is equal to V_{DD} minus V_{BE} that is V_{BE} is the base emitter drop of the bi polar transistor then what happens is say V_{BE} is point seven volts or V_{ON} of the bi polar transistor. After that if the output were to raise further then the base emitter drop of the bi polar transistor would reduce to below V_{ON} which means that it is no longer

going to be in a conducting state. The output voltage will raise to almost close to V_{DD}. That is V_{DD} minus V_{ON} very fast because of the action of the bi polar transistor. After that what happens is because we require a certain voltage drop across the base emitter of the bi polar transistor to maintain it in the on condition, the output voltage would stop raising any further I mean it will raise but very slowly.

Similarly when the output capacitance is going to be discharged, the current flows through into the bi polar transistor as the drain current of the MOS. Now here again the base voltage of the bi polar transistor has to be around 0.6 to 0.7 volts. Now when the output voltage falls to that value close to 0.6 volts, what happens is this voltage (Refer Slide Time: 19:17) collector voltage becomes equal to the 0.6 volts. It cannot fall any further because then the base emitter voltage is going to be below 0.6 volts which means that this bi polar transistor is going to drop very small current and the discharging becomes extremely slow. Also since the drain current of the NMOS should flow into base of the bi polar transistor, the NMOS would also stop conducting.

The logic swing of the bi CMOS, it is not a full swing that is from 0 to V_{DD} as in the case of CMOS but in the bi CMOS, the output voltage would go from V_{ON} to V_{DD} minus V_{ON}. So the swing is from V_{ON} to V_{DD} minus V_{ON} where V_{ON} is the cutting voltage of the base emitter of the bi polar transistor which would be around say 0.6 to 0.7 volts. If you have a 5 volt operation it would go from say 0.6 to 0.7 volts to around 4.4 volts. So you do not have full swing operation here. That is one disadvantage of the bi CMOS when compared to the CMOS.
We shall look at the implications of this sometime later. In general we see that the bi CMOS as lot of advantages compare to CMOS in the sense that it retains the advantage of CMOS as being zero static dissipation circuit at the same time because of the gain of the bi polar transistor it is a much faster circuit compared to a CMOS. Especially when driving large load capacitances. Then there is one more point to be looked at in this bi CMOS. One advantage is that this bi polar transistor does not really go to saturation. Why? because since the emitter voltage of this bi polar transistor can only raise to V_{DD} minus V_{BE} and this is always at V_{DD} which means that the collector to emitter drop of this V_{CE} of this bi polar transistor is always going to be at least 0.6 to 0.7 volts.

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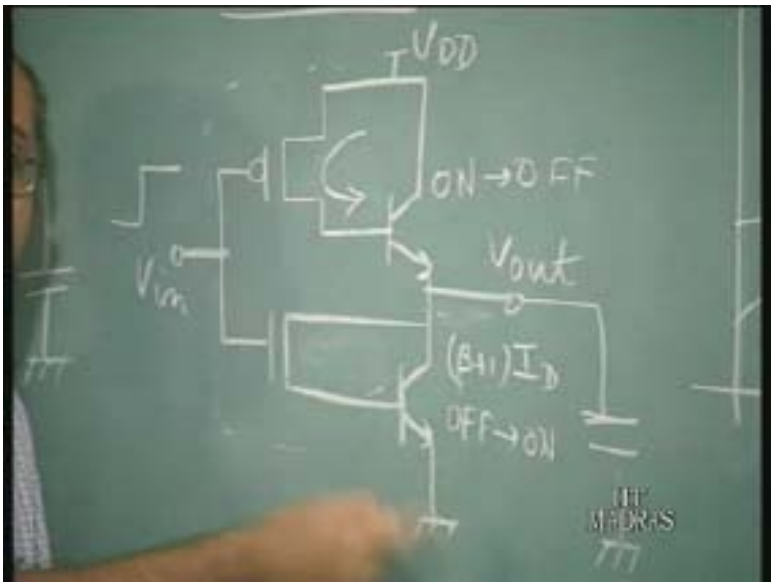

So it does not allow it to go to saturation. In the lower transistor also since the output voltage does not fall to below 0.6 volts are so this collector emitter drop is at least 0.6 volt so it does not go to saturation. But even then what we would like to do is once the input voltage changes state for example from low to high say, then what is going to happen is when the input voltage was low, the PMOS was conducting and the NMOS was off. So this transistor was on, upper transistor was on, this was off. So as this goes from low to high, this should go from on to off and this should go from off to on (Refer Slide Time: 22:36).

Now this on to off should take place very quickly otherwise what is going to happen is, we are having a high speed circuits (Refer Slide Time: 22:47) so we require this off to on should also take place very fast that is output capacitance should be discharged very fast because the lower transistor is going from off to on. So the discharging current is through this lower bi polar transistor.

Now if this upper bi polar transistor does not go off fast then this current is going to actually affect the switching off or the discharging of the output capacitance because the current which is going to discharge the output capacitance is going to be the difference of this current drawn by the lower transistor and the emitter current of the upper transistor, so that is going to be the difference. This upper transistor must switch off fast, so we should ensure that this switching off is done fast.

So how do we ensure that? You see that there is no real mechanism in this circuit for a reverse based current to flow for the bi polar transistor. We have always stressed that when we discussed bi polar logic families that in order to switch off the transistor fast, you must have a reverse base current flowing which draws out the base charge and switches of the bi polar transistor fast. So that is one drawback in this present form because there is no mechanism to remove the base charge.

Now let us see how we can improve this circuit by introducing small changes so that it can switch off fast. What is done is we have a circuit like this. This is the NMOS here, we have the bi polar transistor so this is the input here, there is another NMOS here and this NMOS input is drawn from here. So this is the new inverter.

Now what we have added if we just compare these two circuits. So what we have added in the new circuit here is that we have added an NMOS here and another NMOS here. Now these two NMOS's as we can see are connected to the base of the bi polar transistor and are basically used to draw out the charges from the base of the bi polar transistor, when these transistors have to go from on to off condition. So when you have a similar transition at the input that is low to high, this input then this lower transistor should turn on from off condition and the upper transistor should go from on to off. So what happens is as this goes high then this NMOS transistor is going to turn on from the off condition and this is going to conduct and discharge whatever base charge is there in the bi polar transistor and help it to switch off faster because this NMOS is turning on.

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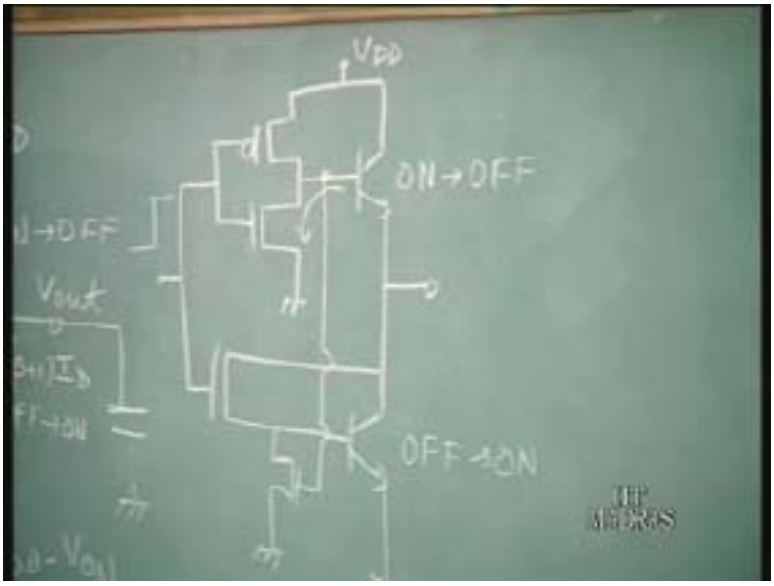

This transistor is going to go from off to on. So basically when this was low, so this is an inverter here you see that we have a CMOS inverter here and the output of the CMOS inverter is actually fed as input here to this NMOS and which is connected to the base of the bi polar transistor. So this is going to draw out the base charge from the bi polar transistor so what happens is when the input is low, this is CMOS inverter, this is high and the input to this NMOS transistor is high so this is on and it maintains this transistor in the off condition. So when this output again goes from high to low then

what happens is this output of the CMOS goes from low to high and this turns on this transistor which helps it to discharge whatever base charge in the bi polar transistor.

So we have two additional transistors here which help to discharge the base charge of this bi polar transistors. So this is the basic form of the bi CMOS inverter. We can also have other logic gates as in the CMOS, for example a NAND gate. Now what we have to do is in the case of a NAND gate, you know in the case of a CMOS we have two PMOS transistors in parallel and two NMOS transistors in series. If we want to have a NAND gate in CMOS, this is the circuit. Now in a case of a bi CMOS what we would do is this which is goes to the base of the bi polar transistor and we have the lower bi polar transistor here (Refer Slide Time: 28:38). So this goes here, this other input actually draw it here. Then the output of this CMOS here in CMOS NAND gate goes to the gate of this NMOS here. This completes the circuit for the bi CMOS NAND gate.

Just I will explain it once more. So there are two inputs here bi CMOS NAND gate A and B. So what happens is when the input in a NAND gate we know the output goes high, when any input is low. When any input is low the output goes high and when both inputs are high, the output is going to be low.

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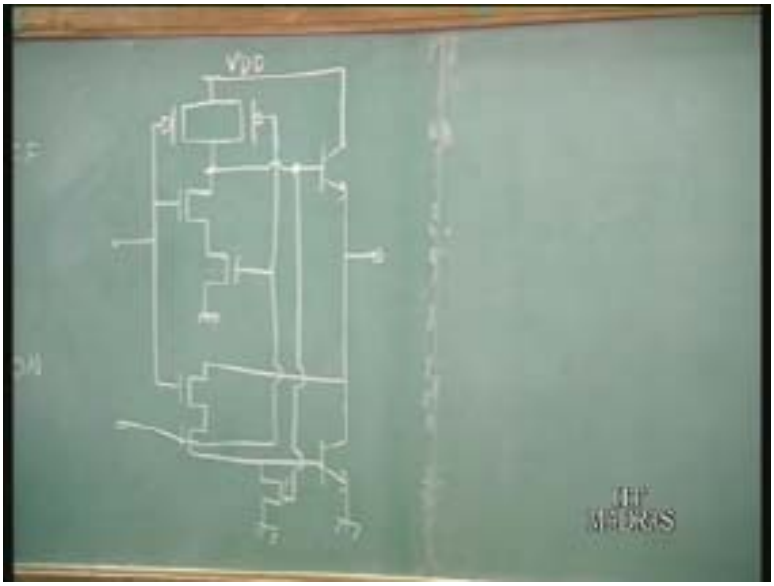

Now when both inputs are high, both this lower NMOS transistors are going to conduct. So both these are conducting as well as these two are conducting. Now since these two transistors are in series say the lower half this is in series, when these are conducting there is a current flowing this way into the base of the lower bi polar transistor and so the lower bi polar transistor is going to be on (Refer Slide Time: 30:20) It is basically going to discharge the output capacitance so the output voltage

goes low. So when both these go high, the output is going to go low and also when both these are high then these PMOS transistors are off.

So this upper bi polar transistor is off whereas these two transistor is also on. These two NMOS are on which enables the discharge of whatever base charge is in the upper transistor. When any input goes low so high to low say here what is going to happen? when this any input goes low then one of these NMOS transistor is going to switch off, is going to go in off condition which means that in the series path is not conducting which means that the lower bi polar transistor is not going to have any base current which means that the lower bi polar transistor is not going to conduct. So the lower bi polar transistor is off. Now at the same time this is basically a CMOS NAND gate. This CMOS NAND gate when any input goes low, the output is going to go high, we have a high here and which means that it turns on the upper bi polar transistor and there is a current flowing in this direction which is going to charge the output capacitance and the output is going to have a low to high transition.

At the same time see, this goes high here, this gate voltage of this NMOS transistor here is going to go high. this turns it on and since this is connected; the drain of this NMOS is connected to the base of the bi polar transistor and current is going to flow out from the base of this bi polar transistor and help to remove any base charge stored in the lower bi polar transistor plus speeding up the switching off of this bi polar transistor (Refer Slide Time: 32:15). So the upper bi polar transistor turns on, the lower bi polar transistor turns off and a current flows out to charge the output capacitance and you have a low to high transition. So this gives the circuit of a CMOS NAND gate. What we basically have is we have a CMOS NAND gate here, this is a bi CMOS NAND gate.

So we have a CMOS NAND gate here, we have the n block of the CMOS here which is actually driving the lower bi polar transistor and then the output of the CMOS NAND gate is driving the gate of this NMOS transistor here which is helping to switch of the bi polar transistor. So now if you look at any bi CMOS circuit, we can actually derive it from the CMOS logic circuit by drawing it in this from. We shall draw a general bi CMOS logic circuit. We have a CMOS gate here so if we are making a bi CMOS NAND gate, we will have to make a CMOS NAND gate. If we have a bi CMOS NOR gate you will have to make a CMOS NOR gate. If you want any other logic function so this is the CMOS equivalent of whatever bi CMOS logic circuit you want to make. So these are the inputs here for that CMOS then the output of that goes to the base of the bi polar transistor and this is connected to the VDD supply voltage.

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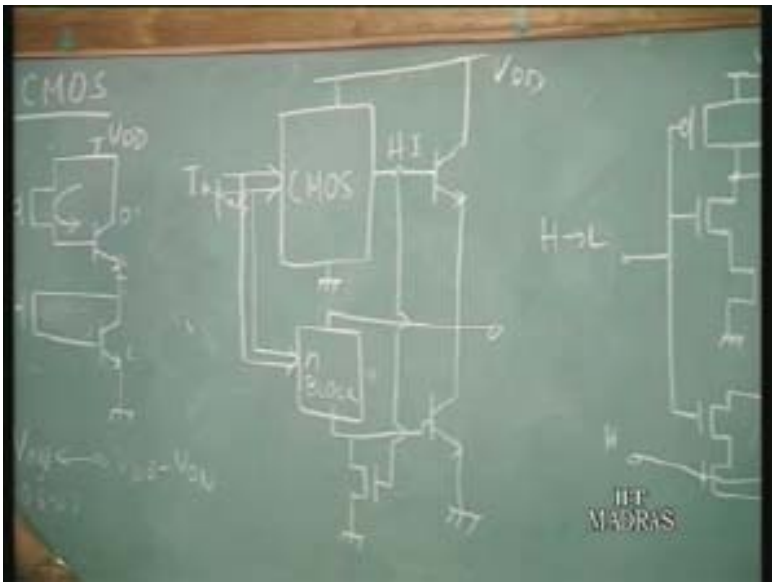

We have another bi polar transistor here and then we have the n block of the CMOS. That is the lower half of this CMOS, the n block is connected to another bi polar transistor and this goes to ground and this goes to ground here and then the output of the CMOS drives another NMOS transistor here. So this goes to the gate of this NMOS which is connected to the base of the bi polar transistor, so the inputs again come here. Suppose we have some inputs and for that set of inputs we must get a logic high say now what happens is this CMOS which is actually also realizing that particular function, so what will happen is this output here is going to go to logic high.

Now when does in a CMOS the output is going to go high when the p block conducts and the n block is off which means that if this output is going to go high here, this n block is going to be off because this is a same CMOS, this is a n block of the CMOS which is the lower half of that CMOS circuit so this is going to be off. Now if the n block is off, the lower transistor is off, you have a high at the base of the upper bi polar transistor which means that it conducts and also the gate of this NMOS transistor here as a high which means that this also conducts which removes the base charge of this lower bi polar transistor. So the upper bi polar transistor conducts, the lower bi polar transistor is off so the output is going to go high and the and the output current is increased by the current gain of the bi polar transistor.

Similarly if for a particular set of inputs, the output should go low then we will have a low here and the n block should conduct because the output is low in a CMOS when the n block conducts which means that the lower bi polar transistor will have a base current which means that this current is going to discharge the output capacitance. Also since this is low here, this NMOS is off which means that it is not really affecting the output, it is not going to have any effect on the circuit. Also since this is a CMOS you have an n block here which turns on. At that n block here in the CMOS is going to discharge whatever base charge is there in this upper bi polar transistor.

So in this case the output is going to go low because the lower bi polar transistor turns on, the upper bi polar transistor is off. So this is the basic circuit of any bi CMOS gate. So any CMOS gate can be converted to a bi CMOS using this particular circuit. Now this bi CMOS obviously has a lot of advantages compared to CMOS as we have already seen but we also said that there was one particular disadvantage that is we are not having full logic swing. This particular disadvantage is it really shows up when we go for low voltage circuits. See up to a long time, the power supply voltages in logic circuits where 5 volts that was a standard which was used but in recent days, the power supply voltages are being continuously scaled down. There are lots of reasons for that one is that as we are going for smaller and smaller devices to improve the speed as well as to reduce the power dissipation, the smaller devices cannot take so high voltages because the electric fields becomes too large with the result that there can be break down problem.

So as we reduce the dimension of the device, we must also reduce the power supply voltages. The power supply voltages are also reduced to reduce the power dissipation. So in order to do that if we reduce the power supply voltages, it really creates problems in the case of bi CMOS. Now if you look at this circuit here, when you have an input voltage whatever input voltage is applied here, if this voltage is now V_{DD} minus V_{BE}, if you have another V_{BE} here (Refer Slide Time: 39:44) so the actual voltage for the NMOS is V_{DD} minus twice V_{DD}. That is also clear here if you go back to this circuit. So if it is V_{DD} minus V_{BE} and you have a V_{BE} here, so what we have is V_{DD} minus twice V_{BE} across the gate to source of the NMOS.

So you know that the current in a NMOS is proportional to V_{GS} minus V_T. So if the V_{GS} in this case is now V_{DD} minus twice V_{BE} in the case of bi CMOS minus V_T squared now but of course you have a current gain of beta is almost beta, beta is high, beta plus one can be approximated as beta.

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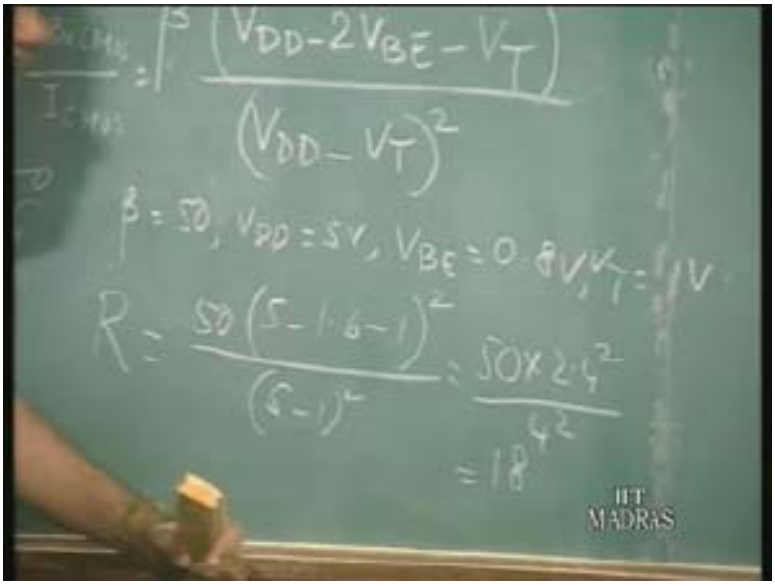

So for a I, for bi CMOS that is charging and discharging current you will have V_{DD} minus V_T whole square. In a CMOS the entire voltage is dropped across the transistor, there is no two VBE drop. Now if you look at a five volt power supply and say suppose when beta is fifty, V_{DD} is 5 volts say V_{BE} is 0.8 volts. This is usually at the higher side but for smaller devices you usually have that and say V_T is equal to 1 volt. So this ratio R let us say will be equal to 50 into 5 minus 1.6 minus 1 squared divided by 5 minus 1 squared. So this is 50 times, this is 2.6, into 2.4 squared divided by 4 squared. So this is basically 0.6 squared that is 0.36, so this will be around 80.

So the current gain which we have due to bi CMOS, although we are having a beta of 50 is only 18 here because this is reduced because of the reduction in the logic swing due to the bi polar transistor. Now this problem is going to be more severe as we go for low voltage circuit. Suppose the V_{DD} is now 3 volts and V_T of course will be also reduced, we have a 3 volt circuits say 0.6 volts then this ratio is going to be equal to say 50 (3-1.6- 0.6) squared divided by (3 - 0.6) squared. So this is going to be 50 into, this is 0.8 squared divided by 2.4 squared, so it is about 5 or so.

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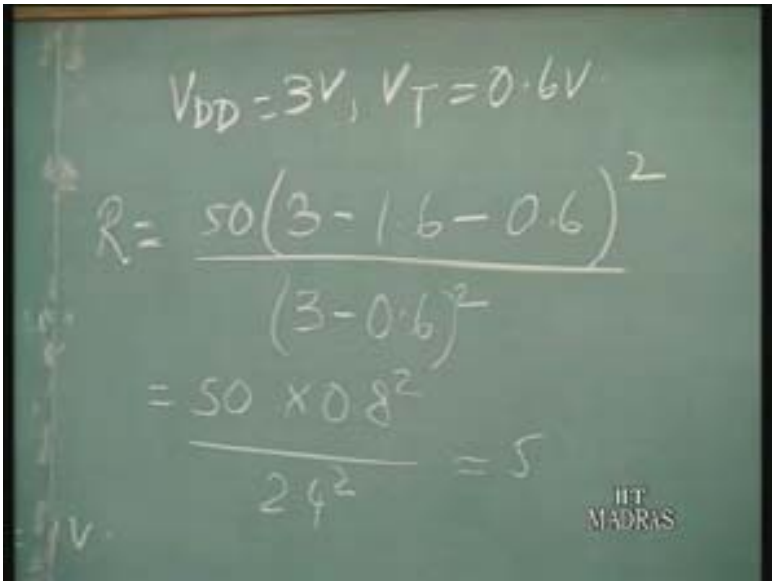

This ratio is further reduced so we see that as we go for low and lower voltage circuits, this ratio is reduced. The advantage of bi CMOS is severely reduced as we go for lower and lower voltage. If we go for say 2.5 volt circuit for example then the bi CMOS would not be as advantageous as a CMOS. There are lot of circuits which has come up which would like to retain the advantages of bi CMOS even at low voltages. So what is done is we have low voltage bi CMOS circuits where an attempt is made for full swing operation. I will just give one example which has been used in the Pentium chip. So what they do is you take a NAND gate, this is basically a CMOS NAND then which goes to the bi polar transistor here and then here the pull down is actually done with the help of NMOS.

So we don't use the bi polar transistor in the pull down because of the fact that at low voltages it is no longer advantages to do a pull down because of the extra V_{BE} drop. One must also remember that here if you go back to this circuit, the difference here is that this voltage here for the NMOS, the source voltage becomes V_{BE}. If you have V_{DD} minus V_{BE} here so it becomes V_{DD} minus 2 V_{BE} across this but here since the source of the PMOS is always at V_{DD}, the gate to source voltage of the PMOS is not so much affected as in the case of NMOS. So what it done here is you put an inverter here and then follow it up with a PMOS. So this is basically the circuit, there are some other additional circuitry here which is for preventing the break down on this transistor but we will not go into that.

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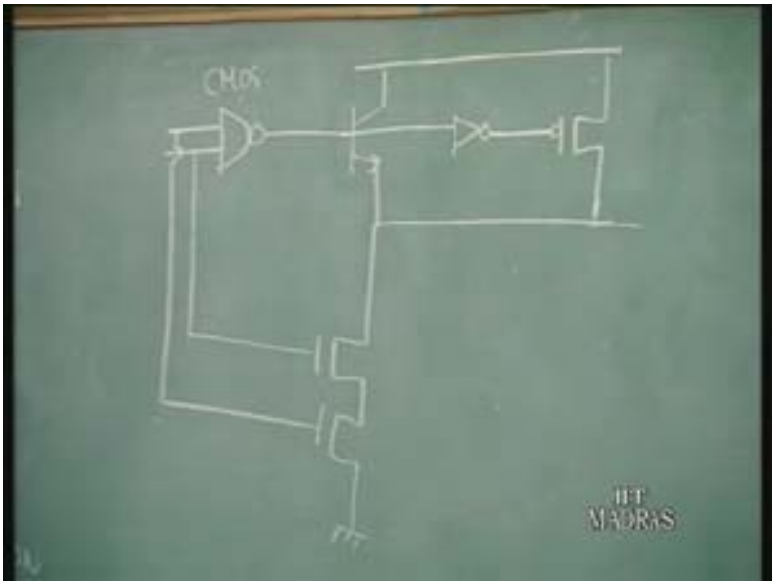

The basic idea here is that these are the two inputs here. Now when the output goes high, the output capacitance is going to get charged up but only up to V_{DD} minus V_{BE} by this bi polar transistor. After that what happens is since this output is high, we have an inverter here, this also CMOS inverter. So this PMOS input voltage is low which turns on this PMOS. What happens is this output voltage goes to V_{DD} minus V_{BE}, the bi polar transistor helps to pull up the output to V_{DD} minus V_{BE}, after that the PMOS is there to pull it up beyond that towards V_{DD}.

The output is going to go to V_{DD} because of this PMOS, at the same time it will also go to zero because you don't have any bi polar transistor. We have full swing operation from 0 to V_{DD} and so a lot of these circuits are being developed nowadays for full swing operation, keeping in mind of the low voltage operation. This is a particular circuit has been used in Pentium in fact there are different variations of this full swing bi CMOS circuits by different groups of people from different companies but what we see basically is for the pull down part, the NMOS goes back to the NMOS. There is no bi polar transistor but for pull up the bi polar transistor is used which helps to speed up the low to high transition of the output. So with that we come to the end of this section on basic bi CMOS circuitry, we shall take up some more applications of this bi CMOS in the next few classes.