Digital Integrated Circuits
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Lecture – 25

nMOS logic circuits (cont.,)
CMOS: introduction

So we shall continue our discussion on MOS logic circuits. Last class we had introduced the depletion mode MOSFET which is a device where channel already exists that is an n channel is there in a depletion mode MOSFET.

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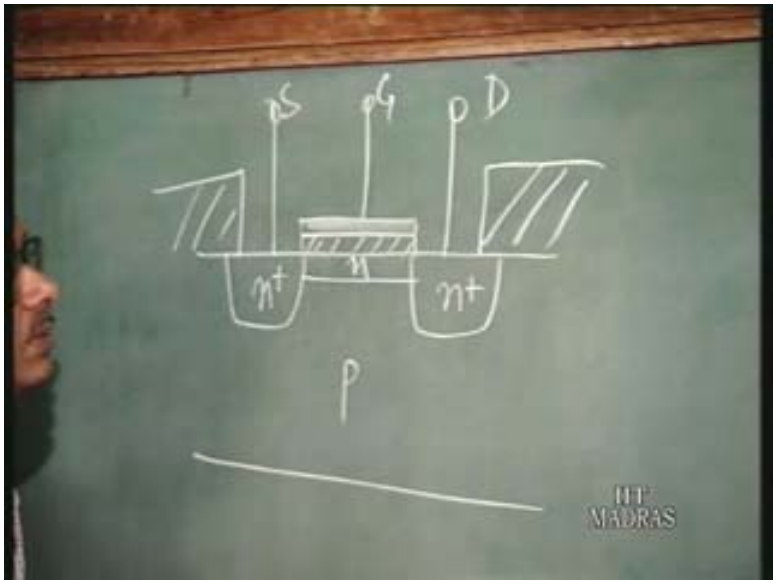

So that between the source and drain there is going to be conduction when drain voltage is applied even when the gate voltage is zero. This is a normally on transistor, the other transistor where the channel does not exist is called an enhancement mode device where it is a normally off device, when the gate voltage is zero the current is zero. This type of transistor is also called a buried channel MOSFET because of the existing already existing channel bc MOSFET sometimes.

As we had already discussed that for this particular device, the characteristic equations that is for the current voltage characteristics is same. One can use the same equations as for an enhancement mode device but the only thing to be noted here is that instead of a threshold voltage for an enhancement mode device here what you have is a pinch off voltage $v_{p.}$.

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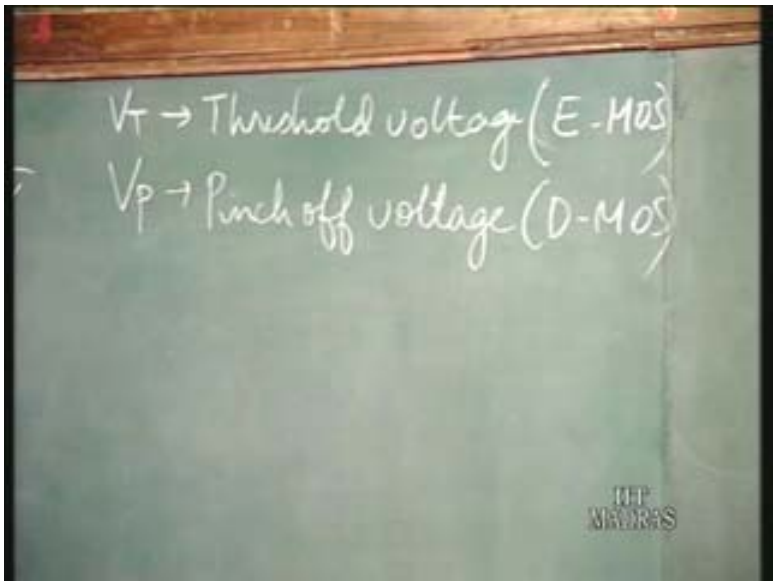

For a threshold voltage, for an enhancement mode device and this is for an enhancement e MOSFET and this is a pinch off voltage for a depletion MOSFET and so when the gate voltage is less than minus $v_{p.}$, suppose $v_{p.}$ is 3 volts when the gate voltage is less than minus 3 volts there is going to be no conduction and when the gate voltage is less negative compared to $v_{p.}$ there is going to be conduction. So from minus 3 volts onwards there is going to be conduction. So if we just look at IV characteristics the current voltage characteristics $I_{D.}$ $v_{DS.}$ for the MOSFET.

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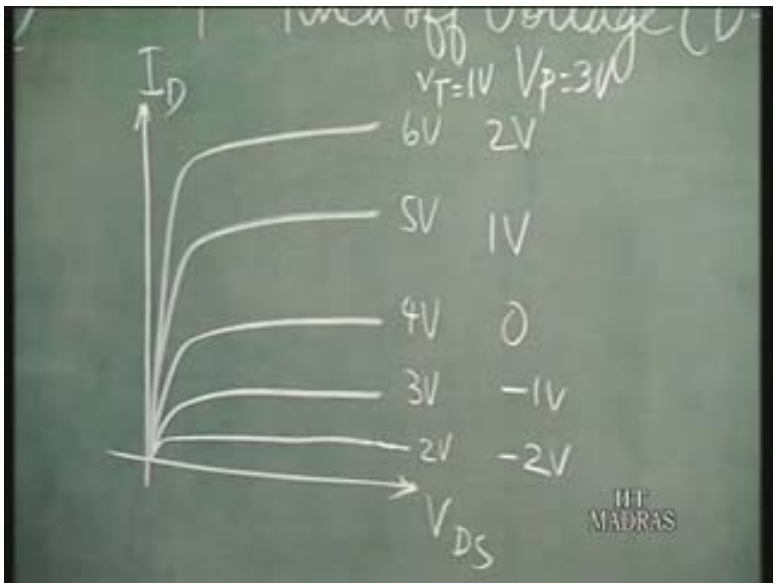

Suppose if this is the characteristic for an enhancement mode MOSFET, so for the enhancement mode MOSFET $v_{T.}$ is equal to 1 volt say. This could be 2 volts gate voltage, 3 volts, 4 volts, 5 volts, 6 volts say whereas if it is the characteristic of a depletion mode MOSFET where $v_{p.}$ is 3 volts. So if $v_{p.}$ is equal to 3 volts say this is a depletion mode MOSFET characteristic then this characteristic might be minus 2 volts, this one for minus 1 volt this is all gate voltages I am writing, this one for 0 volts, this is for plus 1 volts say this is plus 2 volts.

The nature of the characteristics is the same except that you have conduction in a depletion mode MOSFET even for negative gate voltages and even at zero gate voltage there is conduction whereas for an enhancement mode device, you require to have the gate voltage greater than the positive threshold voltage. The nature of the characteristic remains the same. So we come back to the inverter configuration. So here what we are going to do is we are going to use the depletion mode device as the load transistor.

We have already seen a resistance as a load an enhancement mode transistor in the saturated condition, saturated load by shorting the gate and the drain and also enhancement mode device in the linear region characteristics where you apply a constant gate voltage greater than $v_{DD.}$ plus $v_{T.}$. It is always in the linear region. So this is the next alternative where you have depletion mode MOSFET acting as the load transistor.

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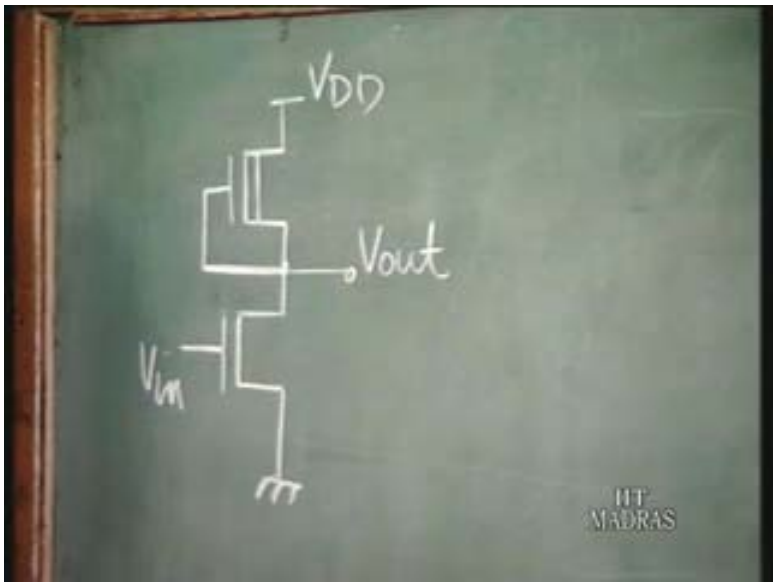

So the structure of this is something like this. This is a depletion mode MOSFET, the symbol is something like this. We put an additional line here which signifies it is a depletion mode MOSFET and for this MOSFET, the gate and the source is shorted for the load transistor. So here it is $v_{in.}$ and here you have $v_{out.}$. So this gate and source is shorted. Now we shall again try to do what we have been doing graphically that is

obtain the input output characteristics that is graphically we should try to obtain the input output characteristics. So here we come back again to the characteristics. So now we have to draw the load line. Now what is going to be the load line?

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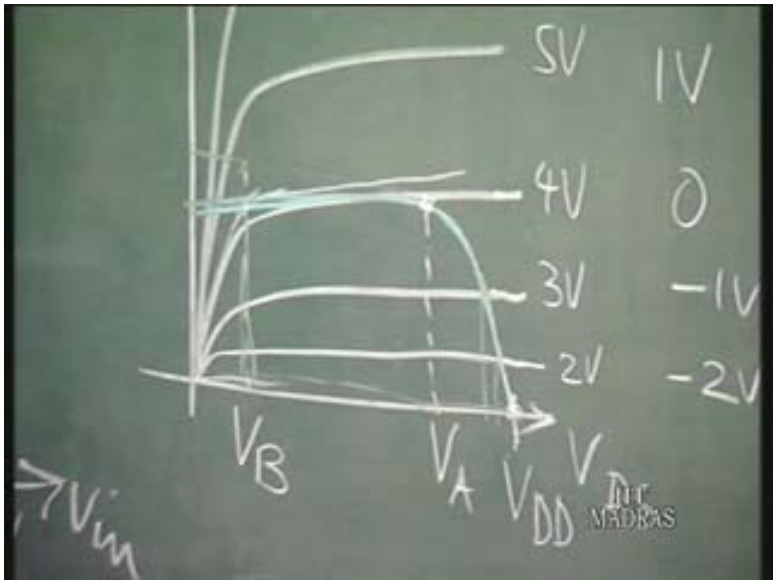

So suppose this is the characteristics of the driver transistor that is the n channel enhancement mode transistor that is a driver transistor. Then we have to draw the characteristic of the load device as the load line. As usual we have to draw it taking V_{DD} as the origin and taking the negative of the axis, just inverting the characteristics. So for this particular load device, gate to source voltage is always zero, the gate and sources are shorted. So we have to pick up the characteristic of the load device for V_{GS} is equal to zero. So see for V_{GS} is equal to zero, the characteristic is something like this.

So the load characteristics is going to be load line as you call it, is going to be something like this. That is the characteristics of V_{GS} is equal to zero, something like this. So of course this is an ideal characteristics but usually it is not so flat, it may be slightly like this, slightly increase in current is there due to various reasons. one of the reasons is of course the channel length modulation when in saturation, the other reason which we have not yet discussed is that in the MOSFET actually it is a 4 terminal device although we have always drawn three terminals, one is the bulk contact usually that bulk contact is put to ground and if you put the bulk contact to ground and in normal MOSFET as such here as you see the source is also grounded.

So there is no potential between the source and the bulk but here since the source voltage itself is going to rise as the voltage changes, there is a bulk to source potential which actually changes the threshold voltage of the MOSFET this is called body effect. The threshold voltage of the MOSFET is not a constant as such or the pinch off voltage in this case but actually it becomes a function of the output voltage because of that it is

not actually very flat but there is a slight increase in current, there is some increase in current as the output voltage we can say of the inverter changes. So anyway let us look at this characteristics.

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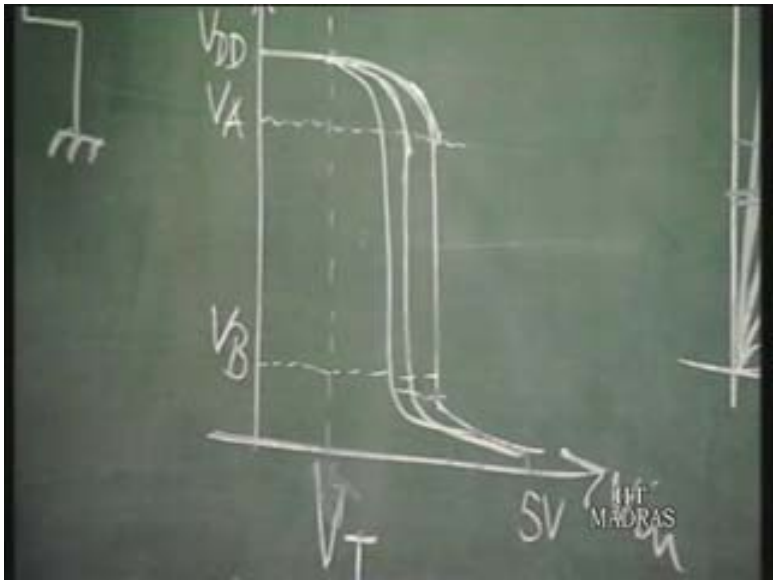

Now if you want to find out the input output characteristics of this inverter, v_{in}, v_{out}; What do we see? When the input voltage is zero what is the condition of this transistor? This transistor is cutoff, it is off basically. When this transistor is off, the output voltage is going to go to v output. Again if you look at this output characteristics, when the input voltage is zero the point of intersection between the characteristics and the load line is equal to v_{DD}., at v_{DD}.. So the output voltage is going to be at v_{DD}.. Output voltage is going to remain at v_{DD}. till v_{in} is equal to v_T.. So this is v_T. and then what happens?

As you go on increasing the input voltage, the output voltage is going to fall but you see the fall is not very sharp. There is a small change in output voltage, if you go on increasing the input voltage. so it is more or less like this, very small drop in the output voltage and then suddenly say for example when the input voltage is slightly less than 4 volts in this graph as you see it here, the output voltage is very close to v_{DD}. and then when its goes just above 4 volts you see, if you take the other characteristics just above four volts, the output voltage has fallen all the way from very close to v_{DD}. to very close to zero. So the gain is very high. so you see there is a sharp fall, it almost falls likes this very steeply and then of course if you go on increasing the gate voltage it remains very close to zero, so this maybe 5 volts. So this is a nature of the characteristics output characteristics.

So the important thing to note here is that if we recall our discussion in last class we had said that for a very high gain we want the load resistance to be very high, R_L. must

be very high. So R_L very high means the load line should be almost parallel to the x axis then only you get very high gain. At the same time for gm to be high, the characteristics, the current should be operating at a higher current.
So what you have now is a more ideal load line in the sense that not only you have a region of very high effective load resistance because this is almost flat load line and also this is elevated. If you just take a resistance and you have such a high resistance, you know it will be something like this close to the x axis but you have an elevated this region of very high load resistance is actually at a much higher current. So that you get the effect of high gm, trans conductance.

So this is a more ideal type of load compared to the other categories. With the result you have a very high gain region and in fact we shall also be able to see that you can adjust this region of the characteristics where you want this region of high gain by choosing the trans conductance parameters of the individual devices properly. So this is about the input output characteristics of the depletion mode load transistor.

Basically again if you just go back to this characteristics, you have a region from here to here when the input voltage is increasing you have a region up to here let me call this $v_{A.}$ say output voltage is $v_{A.}$ when the depletion mode load transistor is in the linear region of operation and the driver transistor is in saturation. Then you have a region when both the transistors are in saturation and in this region, so initially say the driver transistor is off up to here. In this region the load transistor is in the linear region, the driver transistor in the saturation so this output voltage corresponds to $v_{A.}$ on that curve.

This is $v_{A.}$ and then both the transistors in saturation which corresponds to the very steep region of this characteristics and again say suppose somewhere here we may call it $v_{B.}$, what happens is the driver transistor goes to the linear region and the load transistor is in the saturation region. It may be somewhere here so you have the $v_{A.}$ $v_{B.}$. So in fact I have drawn so many curves, I will just retain one of them. So let us just make a very simple analysis and see what is this value of $v_{in.}$ when both the transistors are in saturation, this value; how do you find that out? So basically in that region of operation we have to equate that the current of the load transistor with that of the current flowing in the driver transistor. Now if you look at the expressions.
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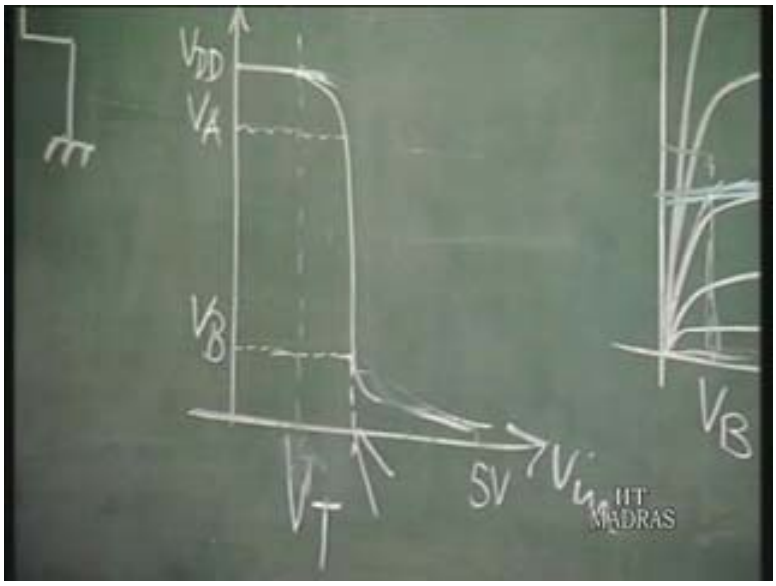

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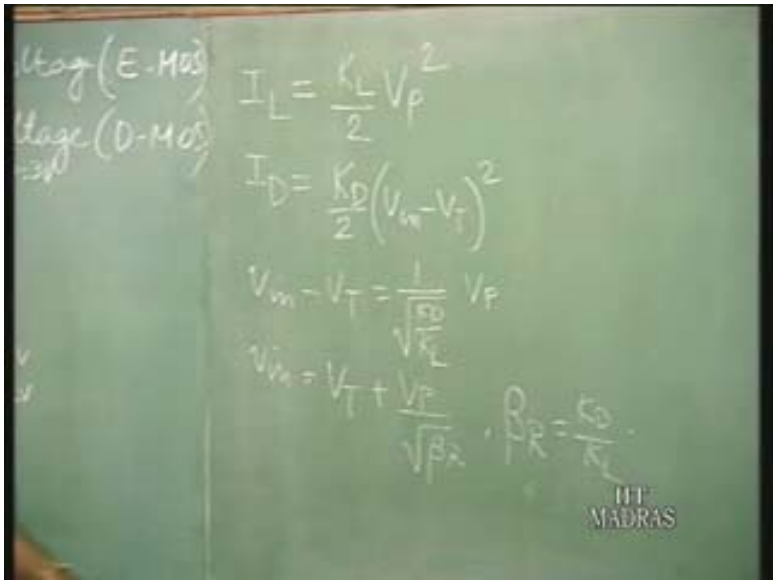

The load transistor current I_L so you know the expression for the saturation voltage so what is it k by 2 into v_{GS} minus v_T whole square. So it is k_L by 2 v_{GS} minus v_T. For the load transistor v_{GS} is always zero so v_{GS} minus v_T is equal to v_p, v_{GS} minus v_T square is vp square. So k_L v_p square and for the driver transistor you have k_D by 2 vin minus v_T whole square. So you just equate that what you get? you will get vin minus v_T is equal to 1 by root k_D by k_L into v_p or vin is equal to v_T plus vp by square root of what is known as the beta ratio where $beta_r$ is equal to k_D by k_L. So v_{in} is equal to v_T plus v_p by root $beta_r$ where $beta_r$ is k_D by k_L. So that is the value of v_{in} at which you have the steep region of the characteristics. Now what about v_A and v_B?

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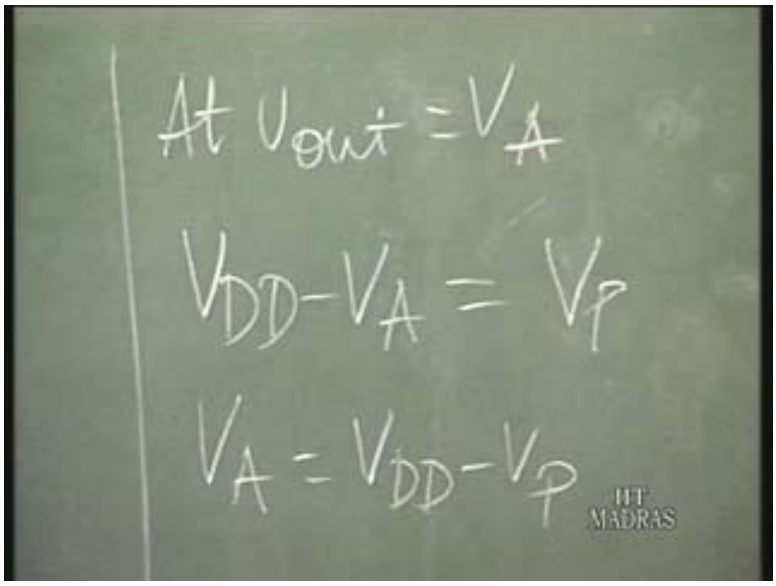

What is v_{A}? v_{A} is the voltage at which the load device goes to saturation that is for the load device that the v_{DS} is equal to v_{GS} minus v_{T}. That is the point at which the device goes from the linear region to the saturation region, v_{DS} is equal to v_{GS} minus v_{T}. So what is it actually? So v output is equal to v_{A} at that time. I think we should write it like this. So at v output is equal to v_{A}, load device goes to saturation.

So for the load device v_{DS} is equal to v_{GS} minus v_{T}. What is the drain to source voltage of the load device? V_{DD} minus v_{A} and the v_{GS} is always zero and v_{T} is actually minus v_{p}. So v_{A} is equal to V_{DD} minus vp. This is equal to v_{A}, we already found that the other voltage is v_{B} which you have to find out.

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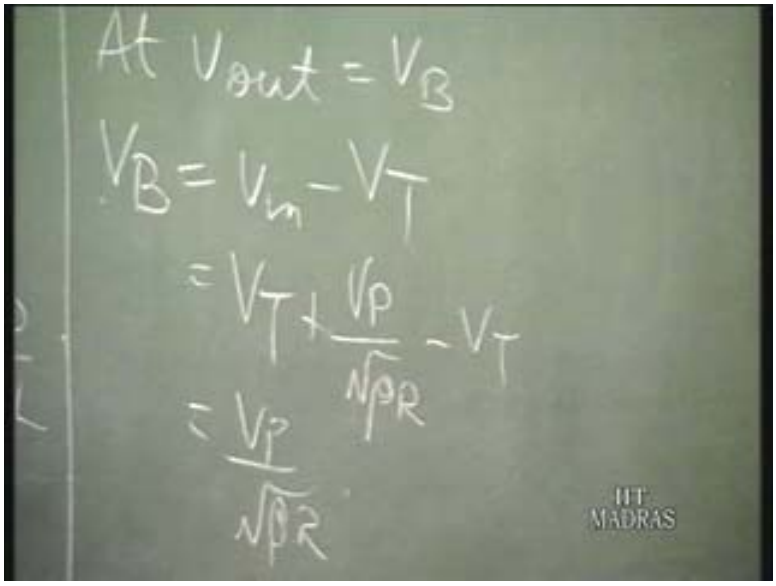

$V_{B.}$ is the voltage if we go back to this characteristics, $v_{B.}$ is the voltage at which the driver transistor goes to saturation. So at $v_{out.}$ is equal to $v_{B.}$, the driver transistor is going to saturation. So for the driver transistor $v_{DS.}$ is equal to $v_{GS.}$ minus $v_{T.}$. What is $v_{DS.}$ for the driver transistor? $V_{B.}$, that is the drain to source voltage. $V_{B.}$ is equal to $v_{GS.}$ is $v_{in.}$ minus $v_{T.}$. What is $v_{in.}$ at that point at $v_{B.}$?

At this point $v_{in.}$ is the same as the vin at which both the transistors are in saturation. It is the same vin here and which we have already found out to be equal to $v_{T.}$ plus $v_{p.}$ by root $beta_{r.}$. So this one is $v_{T.}$ plus $v_{p.}$ by root $beta_{r.}$ minus $v_{T.}$, so this is $v_{p.}$ by root $beta_{r.}$. We have found out the critical points in this curve actually so this is $v_{T.}$ here, this is $v_{T.}$ plus $v_{p.}$ by root $beta_{r.}$.

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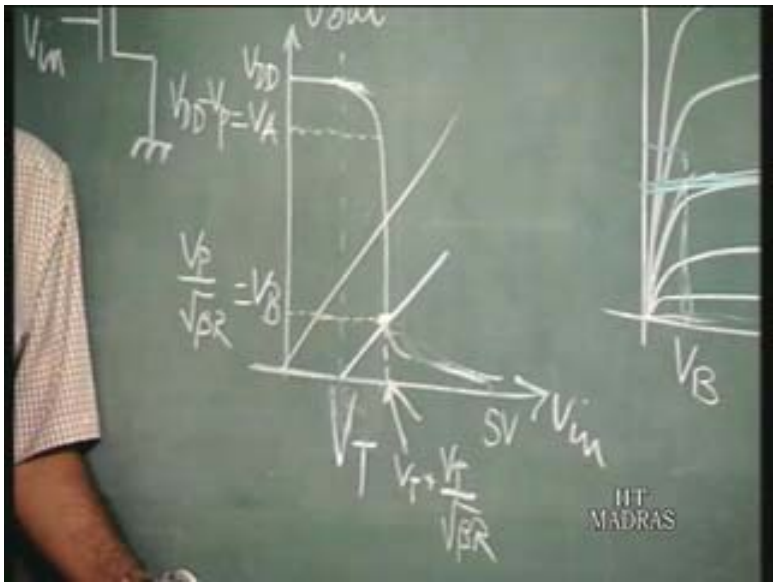

This $v_{B.}$ is equal to $v_{p.}$ by root $beta_{r.}$ and this $v_{A.}$ is equal to $v_{DD.}$ minus $v_{p.}$. Basically if you look at this, this is $v_{T.}$, this is $v_{p.}$ by root $beta_{r.}$ and this is also $v_{p.}$ by root $beta_{r.}$. So basically from $v_{T.}$ if you draw a line with unity slope, the point where it cuts here that is the point. This much is $v_{p.}$ by root $beta_{r.}$, this much is also $v_{p.}$ by root $beta_{r.}$. So that is the point, here it is $v_{DD.}$ minus $v_{p.}$.

So if you want to say that basically the idea is that suppose if you are operating from a 5 volt power supply, it is advantages to have the logic threshold at $v_{DD.}$ by 2, logic threshold I hope you remember. That is if you take a unity slope line here, the point where it intersects the curve that is the logic threshold. That is the unity slope means $v_{in.}$

is equal to vout that is the logic threshold. If the input voltage is greater than logic threshold, output will be less than logic threshold and vice versa that is how you define logic threshold. So it is advantageous to have logic threshold somewhere at the center of the logic swing. So it is advantageous to have it at v_{DD} by 2. So this value if you go back here, v_{in} is equal to v_T plus v_p by root beta_r, this should be about v_{DD} by 2.

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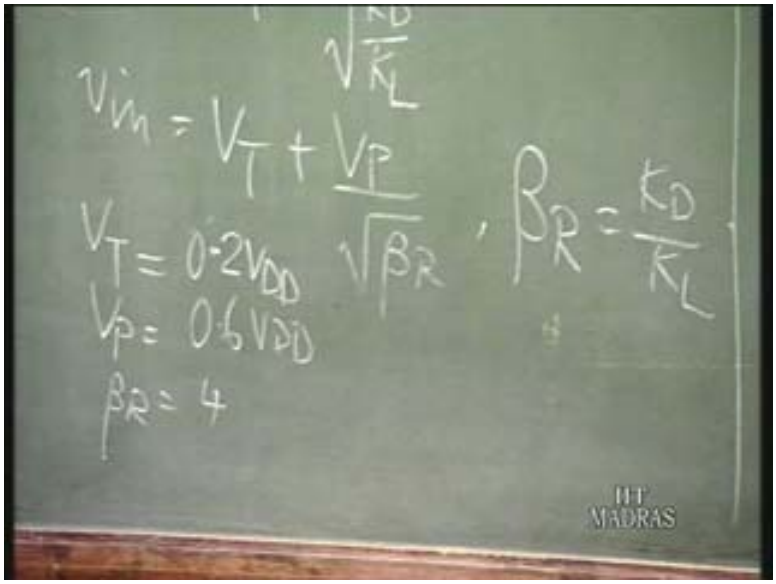

So usually what is done is v_T is taken as 0.2 v_{DD} that is the usual designs and vp is taken as 0.6 v_{DD} and beta r say is taken as 4. When you have say 0.2 v_{DD} plus, this is 0.6 divided by root of 4 is 2 so 0.3 so v_{in} will be equal to v_{DD} by 2. So these are the values one can actually take, in which case this of course is going to be 2 volts. This is v_{DD} minus v_p, v_p is 3 volts actually. So this point v_A is going to be 2 volts, v_B is going to be equal to 1.5 volts.

The reason, in fact you can take a number of combinations to get v_{DD} by 2. Here beta_r is taken as 4, you can have beta_r at a higher value in which case the region of this

unity, this large gain region in the characteristics that portion can be increased but you see what is $beta_r$? Beta$_r$ is equal to k_D by k_L. Now the k_D by k_L, beta$_r$ is equal to k_D by k_L and you know that we have already said that k_D by k_L you are just by controlling the w by l ratios of the transistor. So you have the w_D by l_D say and w_L by l_L that is for the 2 transistors.

So if it is 4, what you usually do? It can be shown that the total area which one actually requires for the device area is equal to w_D into l_D plus w_L into l_L. You must also try to minimize the area, it can be shown. you can do a simple analysis to show that in order to minimize this what one has to do is make this w_D by l_D that is equal to two and w_L by l_L is equal to half, in that particular combination you will have the area to be minimum. That is if you have beta$_r$ is equal to 16 say, then if k_D is 4 and k_L is one fourth then it gives minimum area.

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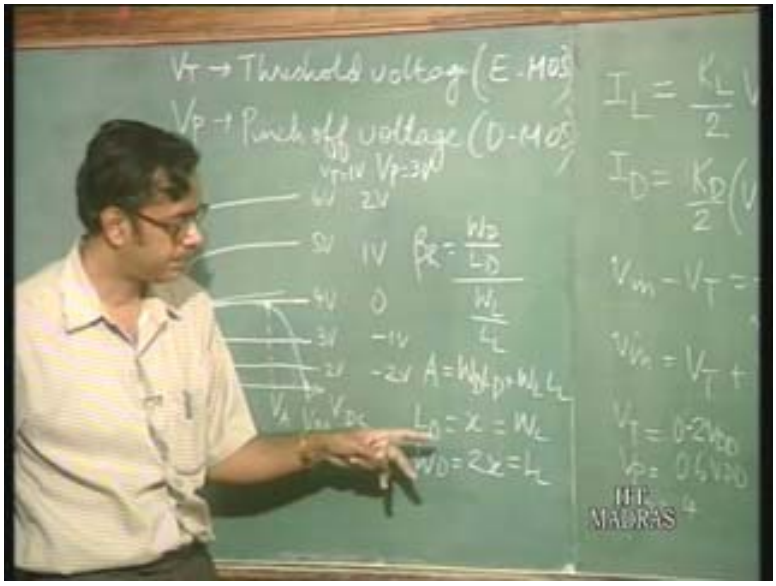

You could have had k_D 8 and k_L half that would also be 16, give you 16 but that requires much larger area. So if you have beta r as four, two and half will give the minimum area. So basically what you have is w_D by l_D, so if x is the minimum dimension in the device, in your technology, you would have ld is equal to x, w_D is equal to twice x and here you want this to be half. So w_L will be x and l_L will be twice x. if you make beta r is equal to sixteen, what is going to happen? This would remain x

but this would become 4 x, w_D and l_L will become 4 x then it will give you 16. So you require more area, it is taking up more area. So that is a tradeoff.

As you can see that if you want this characteristics to be like this, large gain region to be there for most of the output transition, the transition from high to low then you would have to have a larger beta r and that would take up and in fact if you have a larger $beta_r$, it goes all the way like this but that would require more area so that is a tradeoff. So we have seen the inverter characteristics for a depletion mode load and obviously this characteristics is much better than the earlier ones which we have discussed in the sense that if you compare for example with a saturated load, it is better because the output is going to go all the way to V_{DD} which is not true in the case of saturated load because the characteristics, the load transistor is always conducting, it does not cutoff.

If you compare with the linear mode load, it is also better because you require just one power supply, you don't require two power supplies. Also the output characteristics, the nature of the characteristics is much better and there is a sharp transition from high to low. The gain is much better because the characteristics is flat region of the characteristics here, the effective load resistance is very high and you have a very high gain which is much better than all the other characteristics because on the other characteristics the load line was something like this, that was the resistance for the other one it used to be something like this or like this. So this is much better.

So this is an inverter with the depletion mode load as we said that this configuration was very popular for a long period of time and lot of early microprocessors were fabricated using this technology like 8085. So this is an inverter just to say how to make other logic gates. That is if you want to make a NOR gate out of this, how do you do it? You must have 2 nMOS transistors in parallel, so this is the load transistor. This is a NOR gate, A B so this output will be the NOR function of A and B.

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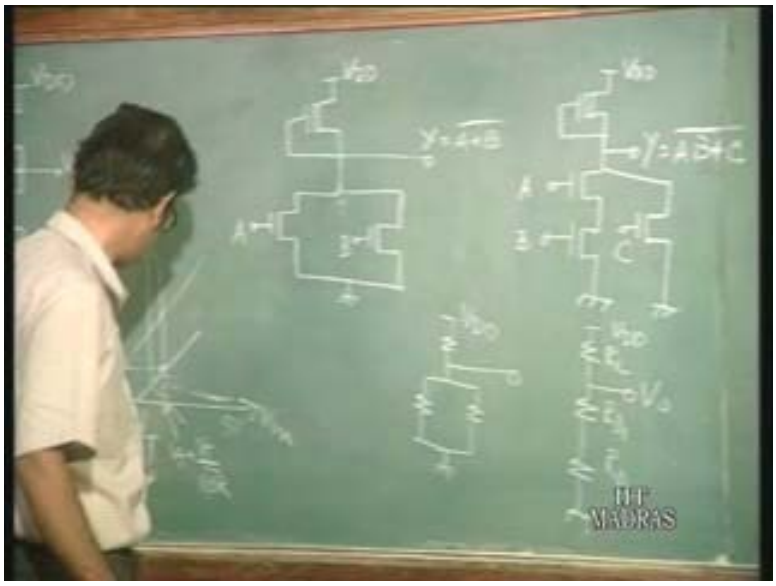

If you have to have a NAND gate which is going to be something like this A B, I just explain little bit. When any input is high in this case in the NOR configuration, the lower transistor is on. So if the lower transistor is on then what happens is the conductivity; basically you can look at it this way that you have the upper transistor, basically the model which is used to understand this is looking at them as resistors, the transistors. So you have a resistance here and you have 2 resistances like this in the NOR case, this is V_{DD}. This is the load device, these are the driver to driver transistors.

If the input voltage to one of these driver transistors is high basically what it means is that this resistance is going to become low and if you have a load, if this resistance becomes much lower than the load resistance, the output voltage will be pulled towards ground. If both this devices are off that means they are very high resistances, so the output voltage is going to be high towards V_{DD}. So if you look at this structure here, so when any input it goes high, the corresponding resistance of the transistor is going to be low which means that the output if you just consider them as a potential divider network, the output is going to be low if both the transistors are off, the output is high. So the basically this acts as a NOR gate.

Similarly if you look at this structure, you have the equivalent resistive network. This is going to be something like this, so this is V_{DD}, this is the resistance of the load R_L you can say, this is R_{d1} and R_{d2}.
So the output is going to be low, see they are in series so the output can be low only when both the R_{d1}, R_{d2} is low. That is when both the transistors are on then only the output can go low that is when both the inputs are high then only the output goes low. Otherwise if one is on and the other is off, the effective resistance of the driver part or the lower part of the network that is going to be high compared to R_L and the output is going to be high. This is a NAND configuration whereas the previous configuration, when the two driver transistors are in parallel is a NOR configuration.

In fact you can have other types of circuits also, so I mean in fact different logic circuits for example here if you put another transistor like this and call this input c, so what is the logic you get? A B or C, I mean A B or C invert. So this is can be explained by similar resistive network. This is the depletion mode load but this configuration also has its problems. In fact one can think of improvements of this. The problem one sees is that this load device is always on.

So what is the problem if the load device is always on? For example if the driver transistor is on, you have static power dissipation that is this is always conducting. So if the input is high, there is a current flowing which if it could be avoided of course it is better. The other disadvantage is when you are switching say if you think of a capacitive load here and if you apply say low to high pulse here, the output should go from high to low. How does it go from high to low?

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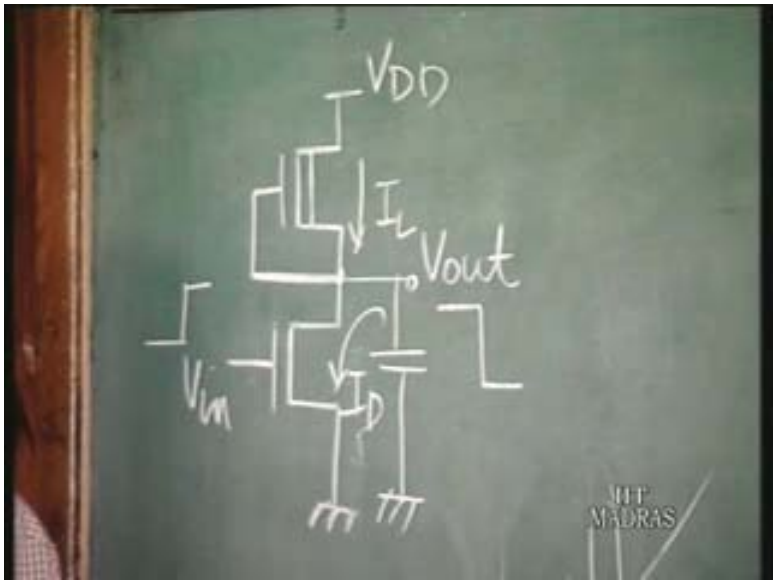

This transistor is turning on, so there is going to be a current flowing here which discharges the capacitance but since this load device is also on, there will also be a load current here, I_L. So the current which is actually discharging this capacitance is equal to I_D minus I_L. If this is the current of the driver transistor I_D, so the current which is actually discharging is I_D minus I_L and this load current is actually slowing down the process because the current which is discharging the capacitance is reduced. So this is a problem. So if you could have a situation when the load transistor also switches off completely that would be better. So that led to the CMOS concept or complementary MOSFET but where you have p channel MOSFET as well the load.

So the configuration is like this, this is the n channel device, this is a p channel device as i said the symbol which I will be using. There are many symbols in text books, I will be using is like this, the simplest symbol one can think of actually. It's a bubble here

signifies the pMOS and the 2 inputs or the two gates are shorted so this is the input here and here you have the output.

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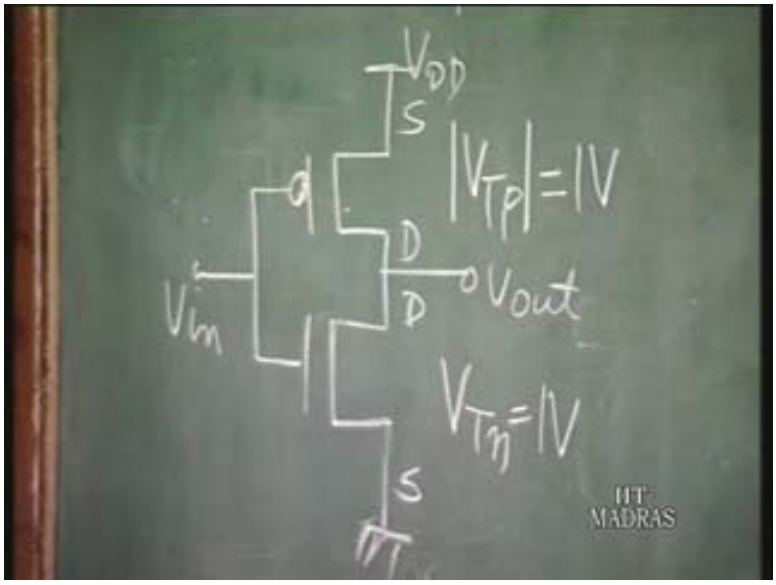

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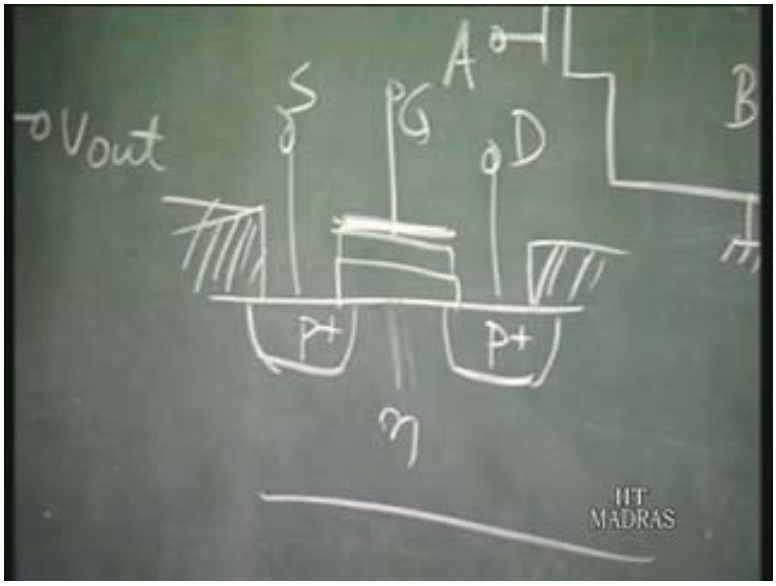

First what is a pMOS? The pMOS is again a MOSFET where the source and drain regions are made of p plus material. The substrate is n type, so this is also an enhancement mode device. So it is exactly like an nMOS, only thing is that the p regions are replaced with the n regions and the n regions with p regions and since the charges, the nature of charges, the sign of the charges are being changed, the voltages required to operate this device are just the opposite. That is the wherever you have

applied a positive voltage, here you have to apply a negative voltage. That is in order to create the channel you must have holes in the channel rather than electrons.

So you must apply a negative gate to source voltage then when the gate voltage becomes negative then only you can induce positive charges in the channel. Again you apply a positive charges, firstly the electrons are repelled from the surface creating a depletion layer and if the negative charges becomes more higher, if you apply a higher negative gate voltage, you attract holes to the surface creating the channel.

So again we can use similar relations as we have used for the n channel enhancement mode MOSFET, only the science of all the voltages are different. Say here this is the source and this is the drain, this is the gate. The drain voltage should be negative with respect to the source because the source of holes is here, the holes flow from the source to the drain. So for the holes to flow the drain voltage has to be negative, the drain to source voltage is negative whereas in the n channel MOSFET, the drain to source voltage is positive. In fact see the MOSFET as such the device is symmetric, the source and drain is symmetric.

So which terminal would you call as the source and which terminal would you call a drain? In a p channel MOSFET, see the source is the source of charges and the drain is where this charge is flow to. So in a p channel MOSFET it is the holes which are flowing. So the terminal which is more negative is the drain and the terminal which is more positive is the source, in a p channel MOSFET. In a n channel MOSFET, the terminal which is more positive is the drain and the terminal which is the more negative is the source because the electrons will flow from lower potential to a higher potential.

So it is going to flow to the drain, when the drain is more positive with respect to the source. So that is how the convention for source and drain. For example if you look at this circuit here, this is an n channel MOSFET. So this is obviously the source and this is the drain because this terminal is more positive with respect to this because this is ground which is the lowest potential in the circuit and so the drain is obviously going to be at a higher potential. So here if you look at the p channel MOSFET, this is the highest potential in the circuit so this obviously becomes the source of the p channel MOSFET and this is the drain because here the drain potential is going to be always less than the source. So you have the p channel MOSFET and the n channel MOSFET. Now what happens let us see.

If you look at the extreme cases let us say the threshold voltage of this n channel device we call it v_{tn} now is say one volt and v_{tp} again we put a mod modulus sign because it is negative as one volt, modulus of v_{tp} is 1 volt. So what happens? Now if v_{in} say zero volts what happens? This device n channel device, the gate to source voltage is less than the threshold voltage, so the n channel device is off. For the p channel device the

gate to source voltage is equal to minus V_{DD}, the source is at plus V_{DD}, the gate voltage is at zero. So the gate to source voltage is at minus V_{DD} and the V_{DD} is say 5 volts, so the gate to source voltage is minus 5 volts. So which obviously means that this p channel device is going to conduct because the gate to source voltage is more negative than the threshold voltage. It has to be more negative to conduct p channel MOSFET.

So this is conducting fully when this is off. So what is going to be the output voltage? Again if you think of it as a resistances, the upper resistance is low. The lower resistance is very high so the output is going to be high. So when the input voltage is zero volts, output voltage should be 5 volts and one of the transistors is off. So basically it means that there is not going to be any current flowing as such in the steady state because in this branch in this circuit from this supply to the ground, this transistor is off. There is no path for current to flow.

Then if V_{in} becomes equal to 5 volts say or equal to V_{DD}, the n channel device is on because 5 volts is greater than 1 volt. This n channel device V_{GS} is greater than V_T so current flows. What about the p channel device? Off, because this is five volt five so it is zero volts and you require the gate to source voltage to be more negative than the threshold voltage for the conduction to take place for the p channel but it is just zero volt so that is off. So the lower transistor is on, the upper transistor is off so what is the output voltage? The output voltage is low.

So this behaves as an inverter and you see in both the cases which we have discussed, one of the transistor is off. So there is no power consumption as such because there is no current flowing. It's just like one of the transistors behaves as an open circuit, a very high resistance. So there is zero static power dissipation in both the study states so that is what makes the CMOS such an ideal inverter. This particular side CMOS inverter circuit behave as an ideal inverter. So in fact if you look at the input output characteristics so this way, the input is less than V_{tn}.

So this is output this is input so this is up to V_{tn}, the output will be V_{DD} which we have already seen then the output falls and here when the input is equal to V_{DD} minus V_{TP}, the output will be equal to zero volts that is when this output transistor is no longer I mean the output transistor is that is when input goes above V_{DD} minus V_{TP}, the gate to source of the p channel device becomes less negative compared to the negative threshold voltage. It cuts off, so the output voltage goes to zero. So this is more ideal inverter characteristics.

In fact the CMOS is very popular logic circuit nowadays and that in fact if you consider in terms of volume may be about 80 to 90% of all the logic circuits fabricated today

would be CMOS. The major reasons for that it seems so popular is the extremely low power dissipation and which makes it ideal for very large scale integration.

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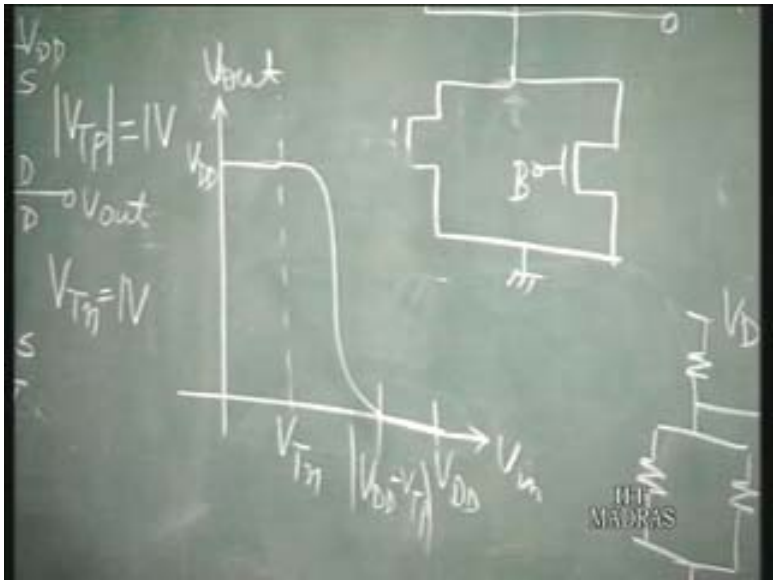

The problem initially was from the technology point of view, it was difficult to fabricate n channel MOSFETs and p channel MOSFETs on the same wafer because the requirement of the wafer was different but once this is being sorted out, this becomes very popular and so in the next class we shall discuss the circuit in more detail and see other logic circuits and further extensions of the basic inverter circuit.