Digital Integrated Circuits
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Lecture – 24
nMOS logic circuits

In today's class we shall begin our discussion on MOS logic circuits. So we shall see how the MOS logic circuits developed from the initial stages to the present logic configuration. Now if you take an MOS transistor just what we had discussed in last class.

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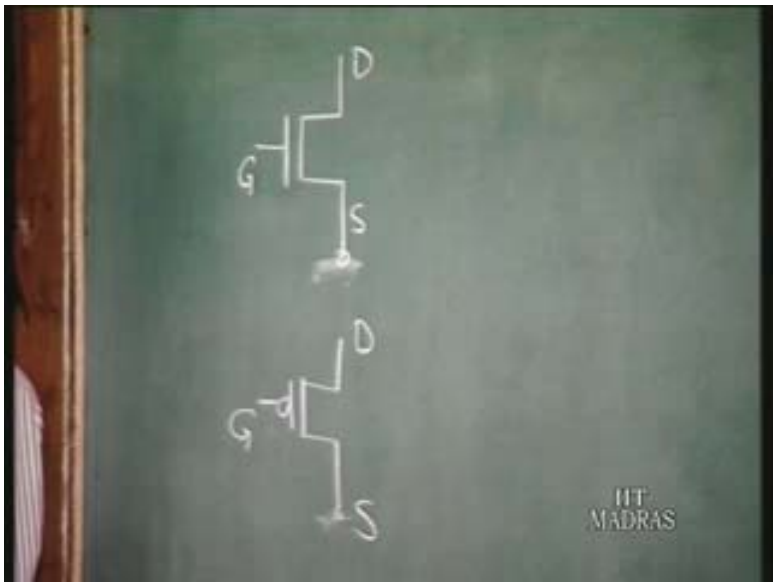

So this is the symbol say we often n channel MOSFET transistor with we shall use. So this is the source terminal, this is the gate and this is the drain. For a p channel MOS transistor what we are going to do is we are going to have a bubble here which indicates that it is a p channel MOSFET. So you have a drain, you have a gate and you have a source. Anyway we shall come to the p channel MOSFET later on. For the time being we shall be using only circuits which contain n channel MOS transistors.

We have already seen that the n channel MOS transistor, the current voltage relation is given by the drain current say which is flowing here $I_{D.}$ is equal to zero, when v the gate to source voltage is less than what is called the threshold voltage $V_{T.}$ which is a very important parameter of the MOSFET is equal to k by two twice $V_{GS.}$ minus $V_{T.}$ into $V_{DS.}$ minus $V_{DS.}$ square for $V_{GS.}$ greater than $V_{T.}$ and $V_{DS.}$ less than $V_{GS.}$ minus $V_{T.}$.

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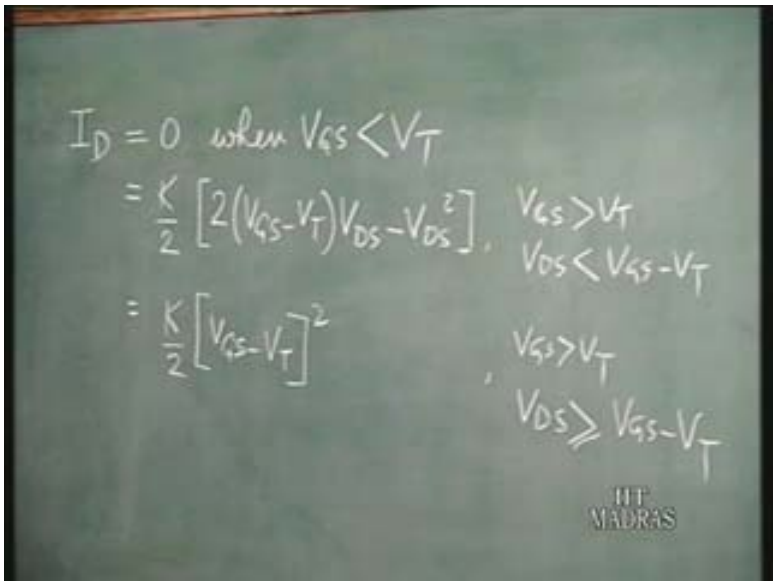

This region of the characteristics is called the linear region of the characteristics and when V_{DS} becomes equal to V_{GS} minus V_T, so what happens is you have 2 V_{GS} minus V_T square, minus V_{GS} minus V_T square so this becomes V_{GS} minus V_T squared. So you have k by two V_{GS} minus V_T whole square for again V_{GS} greater than V_T and V_{DS} greater than equal to V_{GS} minus V_T. The characteristic curve for this MOSFET is something like this.

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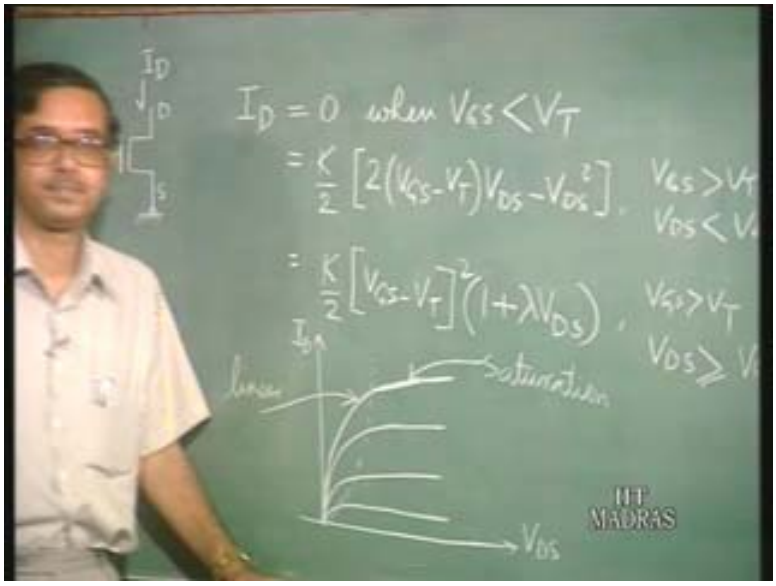

This is the drain current, when you are plotting versus the drain source voltage, we have the curves for different gate to source voltage.

This part of the characteristics to the left of this line, this is the linear region that is when V_{DS} is less than V_{GS} minus V_T this equation (Refer Slide Time: 4:44). So you see that in this case the current increases with drain to source voltage alright so it is called the linear, it is almost a linear it's not exactly linear but it's almost a linear characteristics that is why it is called a linear region of the characteristics and this part of the characteristics when the current is almost a constant and is independent of the drain to source voltage is called the saturation region of the characteristics.

So you must be careful when talking of the saturation region of the characteristics with relation to a bipolar transistor where this region is not the saturation region, this is the active region in the bipolar transistor. So this is the saturation region of the characteristics. There is one more thing that in the saturation region, the current is not exactly a constant. There is a slight increase in the current which is due to channel length modulation that is the effective channel length is reduced because of the penetration of the drain depletion layer. So usually you have one more term in this, one plus lambda V_{DS} means that with drain to source voltage, the current increases slightly and this lambda is a quantity which a small quantity much less than one. So with the drain to source voltage there is a small increase in the drain current.

Now just to have a continuous curve that is when you move from the linear to the saturation region that is there should not be a discontinuity in the drain current because that will give rise to lot of problems in simulation. That is say along this line, this left side is linear, right side is saturation but at this point if you calculate the current using the linear relationship or the saturation relationship, the current should be the same. So at when V_{DS} is equal to V_{GS} minus V_T, the current should be the same irrespective of whether you are using the relation for the linear region or the saturation region otherwise you have a discontinuity in the curve.

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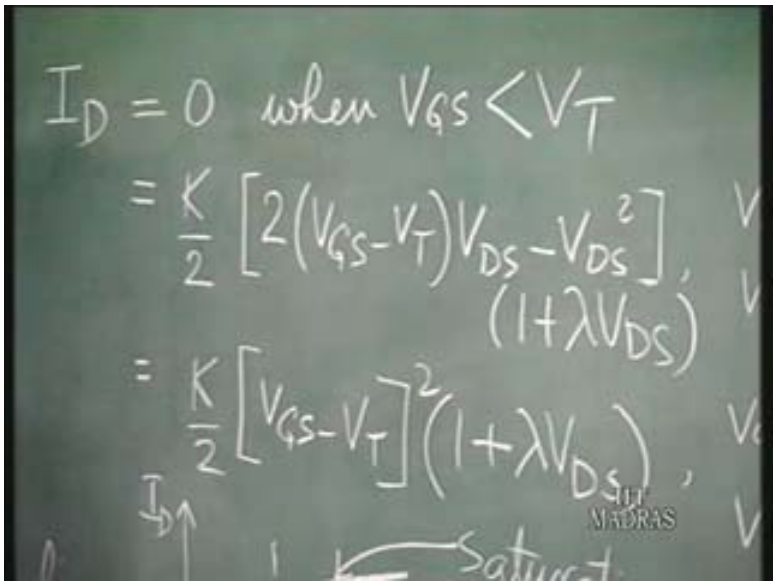

That is why, so if you have a one plus lambda V_{DS} here, you also have to include a one plus lambda V_{DS} in the linear region expression otherwise it will give rise to discontinuity. That is why you also have a one plus lambda V_{DS} although it does not come from physical considerations but from the circuit simulation point of view, to avoid any discontinuity between these two regions but the point is this lambda V_{DS} term is proportional to V_{DS} so in the linear region V_{DS} is quiet small.

So this lambda V_{DS} term is going to be quiet small and so the contribution of this term is going to be quiet small. Only when you go into the saturation region, this term really has some effect. So from that point of view it is not going to be very inaccurate. So this is the equations which are generally used for simple simulations. Of course there are other more complicated models also which are more exact models but for the sake of some hand calculations and trying to understand how the circuits work, we shall use these particular equations to model the MOS transistor when we take up for discussion.

Now again when we take up the MOS digital circuits, we shall have to start with the inverter which is the basic building block on any digital circuit. So how do you make a MOS inverter?

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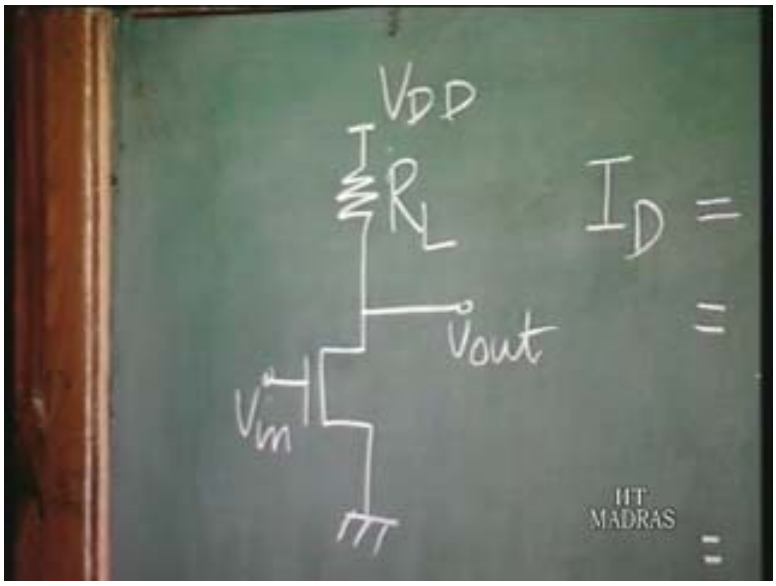

The most obvious and the simplest circuit which one can think of is having the MOSFET here. This source is grounded and we have a resistance here, the load resistance, supply voltage and you have an input voltage here and this is the output voltage. This is the circuit of a MOS inverter circuit. Now how do you obtain the input output characteristics? Again as we have done in the case of a bipolar transistor we go to the output characteristics of the MOSFET which is given here and then what we have to do is we have to draw the load line.

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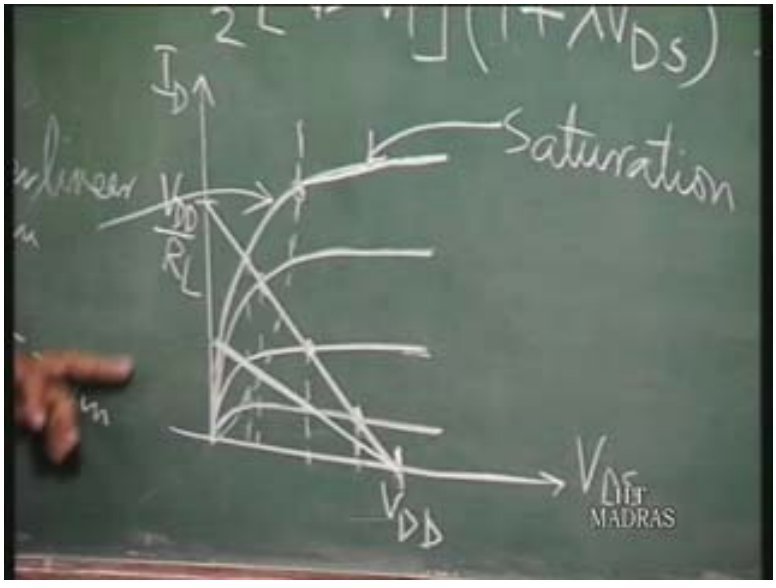

What is the load line? The load line is the current voltage characteristics of the load taking V_{DD} as the origin that is the supply voltage as the origin and drawing it in the

inverted fashion. So something like this. This is the load line. Here this intersects so at V_{DD} by R_L where l is the load that is this load line equation is given by I_D R_L plus V_{DS} is equal to V_{DD}. So when V_{DS} is equal to zero, id is equal to V_{DD} by R_L. So it comes here and when id is equal to zero, V_{DS} is equal to V_{DD}. It is the equation of a straight line. This is the load line and as you know these are the characteristics of the MOSFET for different gate voltages and gate voltages is the same as the input voltage here. So what happens when you increase the input voltage?

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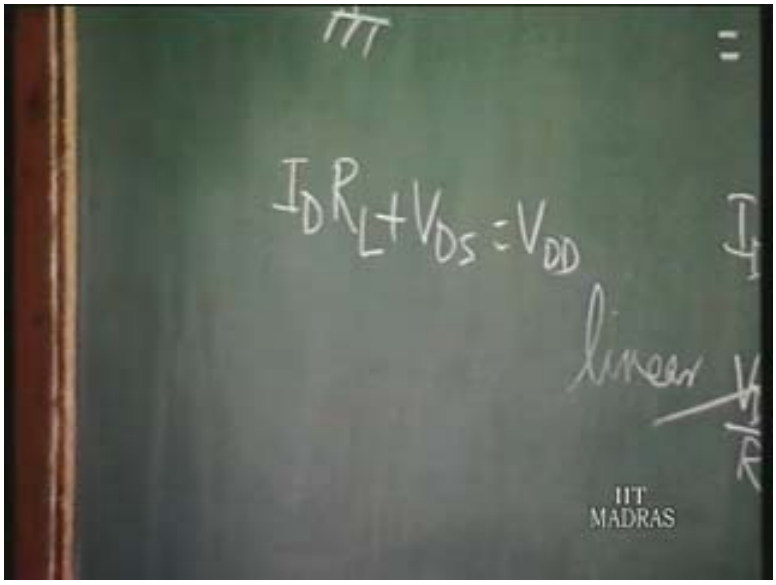

The operating point is given by the intersection of the load line with the characteristic curve. So when the input voltage is given by this value here corresponding to this curve, the point of intersection is here which means that for the MOSFET the drain to source voltage is this much and the drop across the load resistance is this much. So together they make a V_{DD}. Now when you go the next curve that is you have increased the input voltage, the point of intersection is here which means that again the drain to source voltage has reduced whereas the drop across the load resistance has increased and so on.

As you go on increasing the input voltage what happens is the drain to source voltage keeps on reducing and the drain to source voltage is the same as the output voltage of this circuit. As the drain to source voltage reduces output voltage falls that is when the input voltage increases, the output voltage falls which is what you expect in an inverter. So if you just plot the exact input output characteristics, so v_{in} v_{out}. Now when v_{in} is zero volts what happens? Which is the characteristic curve here? If you look at this equations here, I_D is equal to zero when v_{GS} is less than v_T.

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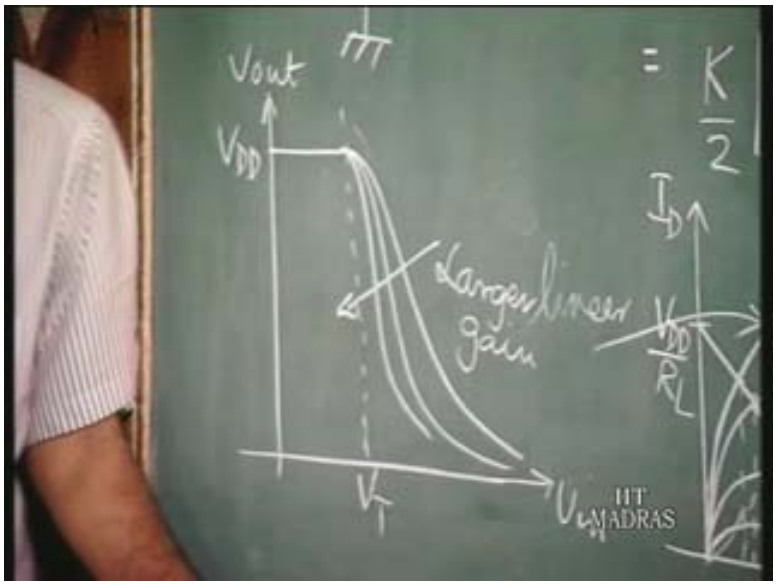

If $v_{T.}$ say 1 volt so when $v_{in.}$ is less than 1 volt, $I_{D.}$ is zero that is the drain current curve over the x corresponds to the x axis here. So the point of intersection is at $v_{DD.}$. So up to $v_{in.}$ is equal to $v_{T.}$, the output voltage is going to be equal to $v_{DD.}$. So you have this up to input $v_{T.}$ output voltage is equal to $v_{DD.}$ and then what happens? As you go on increasing the input voltage, above $v_{T.}$ the output voltage keeps falling. So the input output characteristic will be something like this. So the input output characteristic will falls likes this. In this part of the characteristics, the circuit here actually behaves as an amplifier. That is and the gain of the circuit is of course the gain is negative that is when the input increases the output falls.

If the gain of the circuit is made higher, it would mean that the output, the fall would be sharper that is if the gain is increased it will be something like this. So this way it is for larger gain. Now so if you want to have a better characteristics, we have to increase the gain. Now what is the gain equal to? Gain we shall say is equal to d $v_{out.}$ by d $v_{in.}$ and $v_{out.}$ is equal to $v_{DD.}$ minus $I_{D.}$ $R_{L.}$.

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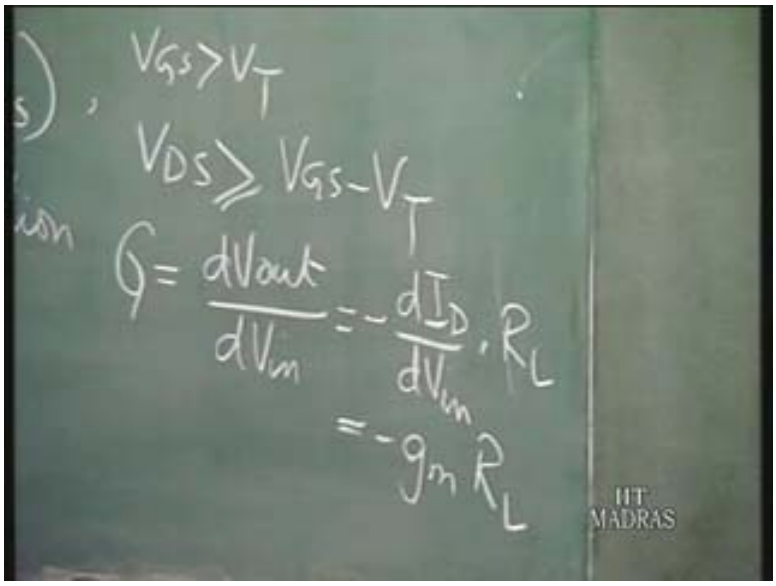

So what you get is minus d I_D by d v_{in} into R_L and what is this d I_D by d v_{in}? gm, so it is equal to minus gm into R_L. If you want to have a higher gain one way would be to increase the load resistance. So if you increase the load resistance what happens to this load line? The load line is going to be something like this that is if the load resistance is higher, the load line is going to be something like this. That is this lower curve here, this slope is going to be higher. This is because this point is v_{DD} by R_L.

It is clear from here that if the load resistance is increased then the current flowing through the device is going to be less. Isn't it? Because at the operating point the current would be less. Now it is quite obvious also if you see from this relationship. If you look at this characteristic equation is quiet obvious that it is obvious that the gm of the MOSFET is higher in the saturation region. The currents are higher that is the difference, basically gm means del I_D del v_g. How much does the current change with v_g? So if you look here in the linear region, if you look at the different curves with vg they are more closely packed whereas here they are more widely separated.

So the device has a higher gm that is del I_D del v_g for in the saturation region that is clear and if you look at this expression for the saturation region, what is del id del vg? It is proportional to, if you just differentiate this with respect to vgs you get k v_{GS} minus v_T. gm is equal to k v_{GS} minus v_T which means that gm depends on v_{GS} so larger the gate to source voltage larger is gm, the transconductance. It's also quiet obvious that in fact if you have the same difference, if you plot the output characteristics with equal increments of v_g, the curves will be more and more separated, if you go for higher and higher gate voltages because the gm increases with vg. At lower gate voltages the gm is less.

So now if you look at this equation there is a problem that if you want to increase the gain you have to increase the R_L but if you increase R_L, you will be operating a lower current levels which means that you have lower gm. So that is a problem which of

course with this circuit we cannot avoid. So anyway you get a characteristic like this. So this was the simplest of the inverter circuits one can think of but again as we know that in an integrated circuit, fabricating a resistance is a problem especially if you want to go for high values of load resistance, it is not advisable.

So the next it is better if you can use an active device as a load or an active device here in a MOS circuit MOS based circuit would be a MOSFET. So obviously the people went for a MOS transistor as the load device. So the first circuit which was used was the load, what is called saturated load. That is the circuit configuration is something like this. So this is our MOS transistor and that for the load you have another MOS transistor with the gate to drain shorted, so this is V_{DD}.

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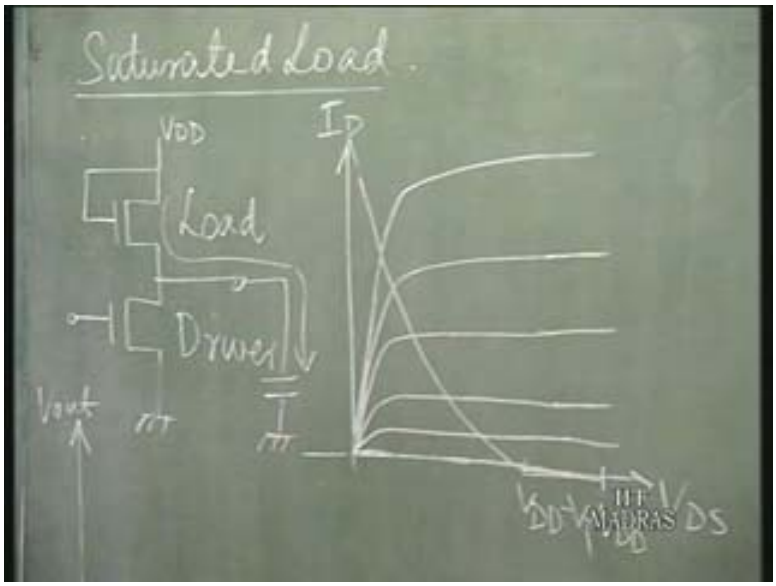

This acts as the load device, the gate to drain is shorted. So what does it mean if the gate to drain is shorted? It means V_{DS} is equal to V_{GS}, the drain to source voltage is equal to gate to source voltage and we have already seen that the transistor goes in to the saturation region when the drain to source voltage is greater than V_{GS} minus V_T and if the drain to source voltage is equal to gate to source voltage then obviously drain to source voltage will always be greater than gate to source V_{GS} minus V_T which means that this particular transistor would always be in saturation. So if this is the load device now what is going to be the output characteristics?

Again we follow the same procedure. We draw the output characteristics of the MOS transistor and then we have to draw the load line. For the load line again we have to draw the characteristic of this device again with V_{DD} as the origin here, starting from V_{DD} as the origin and just inverted like this. Now what is this characteristics of this device, how does it look like? Since this is a saturated transistor, we have to take the expression for the saturated case which is this one that is k by two V_{GS} minus V_T square

and so v_{GS}, see v_{GS} is actually equal to v_{DS} for that. So that is the voltage across the device basically behaves as a two terminal device because you are shorting the gate and the drain.

So it is this equation, it's a square law type of relationship but one important point here is that its k by 2 v_{GS} minus v_T whole square so what happens when v_{GS} is less than v_T? Current is zero, this current is going to flow only when v_{GS} is greater than v_T for this device. So when v_{GS} is less than v_T then the current is zero.

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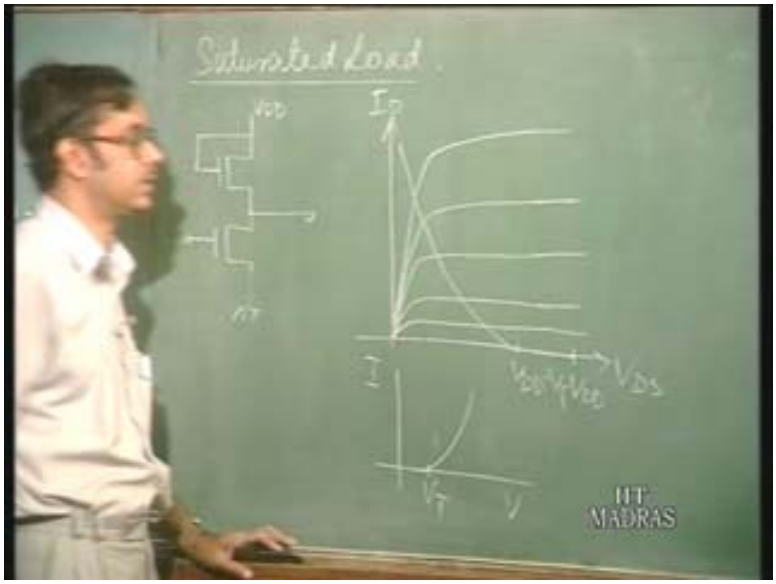

So if you look at the characteristic for that, I just want to draw it separately. This zero up to v_T, so if you want to plot the IV characteristics of the load device, it is up to v_T is zero and then it follows the square law type of relationships. So now if you want to use this characteristic as the load line in this curve here, you have to draw like this up to v_{DD} minus v_T which is like this and then goes like this. So this is the load line. If you have this as the load line what is going to be the input output characteristics? We will draw it here. This is v_{in} and this is v_{out}. Again the same question, when v_{in} is equal to zero what is v_{out}?

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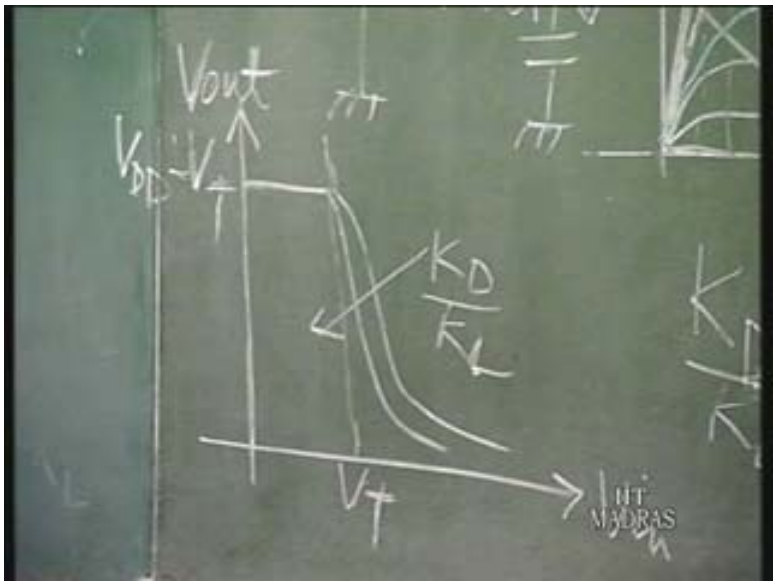

When v_{in} is equal to zero the characteristic equation for the MOS transistor, anyway see in this case when you have two transistors here, the name given to this transistor we choose the lower transistor is called the driver transistor and this is called the load transistor. I mean just to differentiate which transistor we are talking of. So this is the characteristic of the driver transistor when v_{GS} is equal to zero or v_{in} is equal to zero for the circuit, this is here. Now so where does the two characteristic that is the load line and this characteristic intersect? It intersects all along this. So what is going to be the output voltage, whether it is going to be v_{DD} or v_{DD} minus v_T or somewhere in between, that is the question.

Now what happens is when you want to discuss that i think what we should bring out is that usually we have not brought any capacitance into picture as such because we are just drawing static characteristics where usually these devices will have a capacitive load which maybe the input capacitance of the next device. Now what happens is when the input voltage goes from high to low say, so that this particular device the driver device is cutoff that is basically the input voltage is less than v_T.

So that the driver transistor is off. What is going to happen is the capacitance will be charged by the load device. the load device is on, the output voltage was low so the output voltage is going to rise because the current will flow this way to charge the capacitance and as the output voltage rises, the source voltage of this load device it is increasing and the gate to source voltage is falling because the gate voltage is fixed at v_{DD}. So up to what value can the output voltage rise? It can only rise still v_{DD} minus v_T because when the output voltage goes to v_{DD} minus v_T,

The gate to source voltage of the load transistor becomes equal to v_T and then the load which is being provided by the load device to charge the capacitance goes to zero. So

the voltage across the capacitance cannot rise any further. So the output voltage of this type of configuration is going to be equal to V_{DD} minus V_{T}. It can never go beyond or above V_{DD} minus V_{T} because if it has to go above V_{DD} minus V_{T}, the current has to be provided by the load device which it cannot do when the source voltage goes beyond V_{DD} minus V_{T}. So the output voltage is actually V_{DD} minus V_{T}. So this is the output voltage V_{DD} minus V_{T} and then of course the situation is quiet similar to the inverter with a resistance load. It is not really a straight line but it is quiet similar you know, the output voltage will keep falling as you go on increasing the gate voltage or the input voltage. We have a situation like this, so this is V_{T} so after V_{T} the output voltage keeps falling.

Now again if you want to in increase the slope or the gain of this inverter what you have to do is you have to have a characteristic something like this. That is if you have a characteristic like this, see for the same gate voltage here say if you take the same gate voltage that is the input voltage is somewhere here so it starts falling from vin is equal to V_{T} but for the same input voltage here, the output is fallen to a lower value for the same input voltage. For this if the load line was this, if the load line is like this it is still but the higher value (Refer Slide Time: 30:59)

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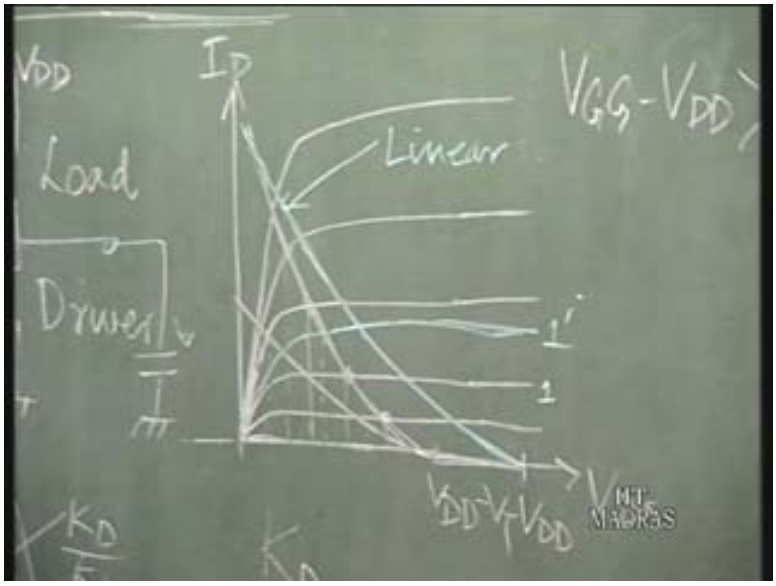

So obviously for this curve, the gain is more. Now what does this mean? For this curve what is the difference between these two curves? These are curve of the load device. What can you say about the transconductance parameter of the load device? This one, the trans conductance parameter is less.

Suppose if you consider that this is the load device and for the driver if you have a device with a larger transconductance that is all the curves is going to move up for the same V_{in} the curve is going to move up. That is say for example if you consider this

curve one and another curve one prime say, they are for the same gate input voltage but with two difference trans conductances of the driver transistor. So this obviously has a higher transconductance. So if you have a higher transconductance for the driver transistor, gain is more and if you have a higher transconductance for the load transistor, the gain is less.

So the gain actually depends on what is called the $k_{D.}$ by $k_{L.}$ ratio where $k_{D.}$ is the trans conductance of the driver transistor and $k_{L.}$ is the trans conductance of the load transistor. This $k_{D.}$ by $k_{L.}$ ratio, so if you increase the $k_{D.}$ by $k_{L.}$ ratio then the gain is going to go up.

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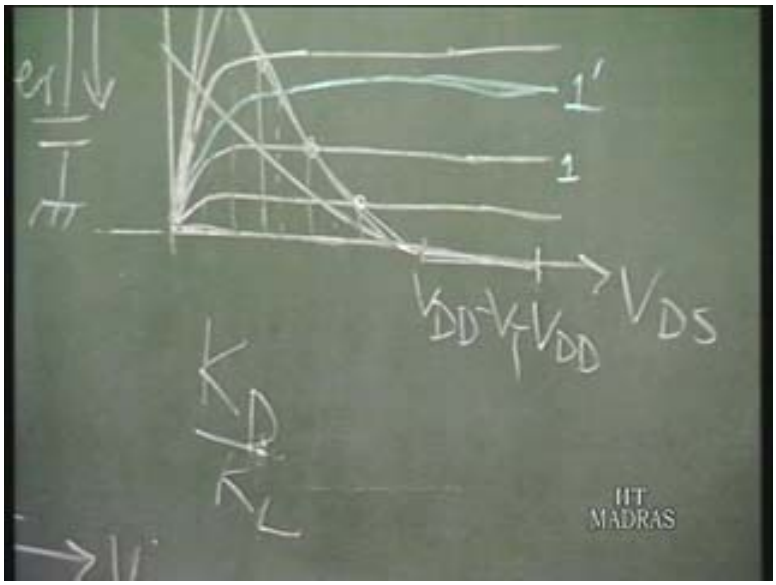

So we shall come to that how it depends on that, i think we shall discuss that for maybe other logic circuits but basically it is understood that if we increase $k_{D.}$ by kl ratio, the gain goes up. So if you have increasing $k_{D.}$ by $k_{L.}$ ratio, the gain goes up. So in fact if you have similar devices, if you consider them to be similar devices that is they are fabricated simultaneously. Then what does this $k_{D.}$ and $k_{L.}$ depend on? They depend on the width to length ratio of the individual devices.

So you can control the gain by changing the sizes of the devices. That is how it is usually done, to change the gain you control the sizes of the individual devices what is called the w by l ratios of the individual devices. So we shall come to how exactly it depends maybe for some other circuits because this circuit, it did not last in the sense that it was replaced by better circuits. This is the output characteristic of this particular circuit obviously this has the disadvantage in the sense that the output voltage does not go up to $v_{DD.}$.

You are losing output voltage, the logic swing is less than the other circuits by $V_{T.}$ and this has repercussion in the sense that the logic swing less means the noise margin is less, also the speed of the device is going to be less in the sense that since it is not going all the way to $V_{DD.}$ say for example when the output voltage charges to $V_{DD.}$, if you have a circuit for the output voltage charges to $V_{DD.}$. So output voltage goes up like this and if the output voltage charges to $V_{DD.}$ minus $V_{T.}$. Now it will go up like this.

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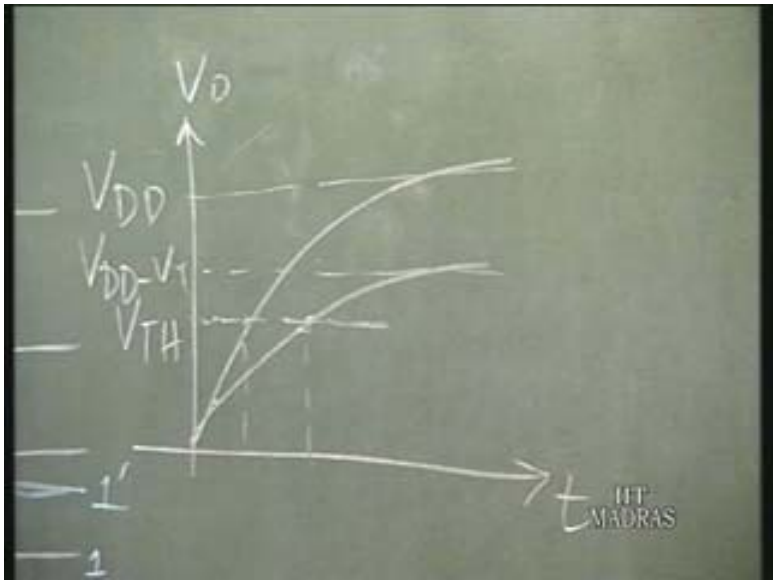

So if you say that the logic threshold is somewhere here where above which we are going to say it is logic one. So obviously if it is charging towards $V_{DD.}$ minus $V_{T.}$, so this is the time how it charges output voltage. So the one which is charging towards $V_{DD.}$ minus $V_{T.}$ is going to take more time. Its quiet obvious. If this is the value of logic thresholds which consider as the threshold between 0 and 1. So these are some of the problems so one has to see how to remove this problem.

So the next circuit which was contemplated or used maybe was the one with, not a saturated load but with a linear load. That is you use the load device in such a way, configure the load device in such a way that it is not in the saturation region but in the linear region of operation. So how do you do it? Actually load operating in the linear region.

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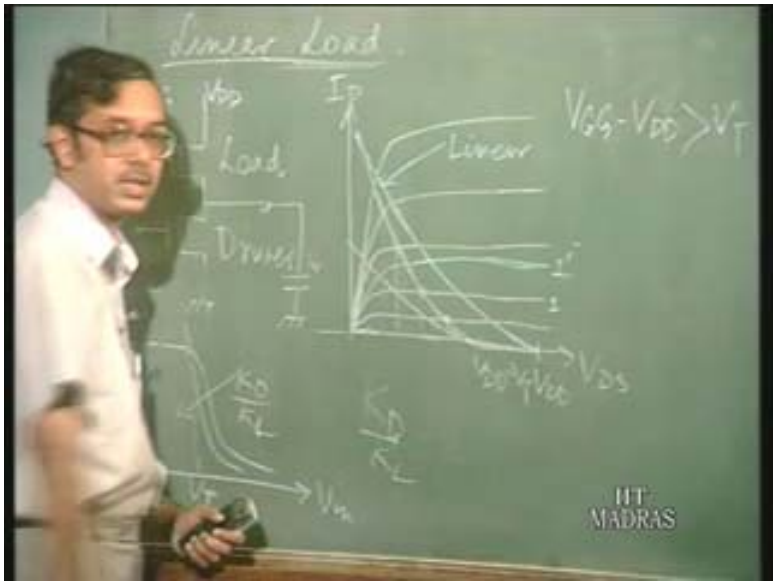

So what you do is you have this gate voltage you have a separate power supply for the gate voltage v_{GG} and if v_{GG} is greater than v_{DD} by v_T that is v_{GG} minus v_{DD} is greater than v_T. That is what you are going to have is that see this transistor, the gate to source voltage is always going to be greater than the drain to source voltage by more than v_T. So v_{DS} is always going to be less than v_{GS} minus v_T, the gate to source voltage is greater than the drain to source voltage by more than v_T because v_{GG} is greater than v_{DD} by more than v_T.

So v_{DS} will always be less than v_{GS} minus v_T which means that the transistor is always going to be in the linear region of operation and this transistor is always going to be on because this is greater than v_{DD} minus greater than v_{DD} by v_T and the maximum value which you can have here at the source point is v_{DD} and so since v_{GG} is greater than v_{DD} by more than v_T, so v_{GG} minus this source voltage which can be maximum v_{DD}. The gate to source voltage of this device is always going to be greater than v_T. So this transistor is always going to be on.

So if you look at the load line for this, if I may draw it here again on the same characteristics for the linear load, it is going to be something like this. So this is the linear. So which would mean that from the performance point of view, from the input output characteristics point of view, the output voltage would go all the way up to v_{DD}. When v_{in} is zero, the point of intersection is here up to v_{in} is equal to v_T. So if you look at the input output characteristics so this is v_{in}, this is v_{out}. It is going to be similar

to the one with the resistive load, goes all the way like this. So up to $v_{T.}$ it is $v_{DD.}$ and after that it keeps falling.

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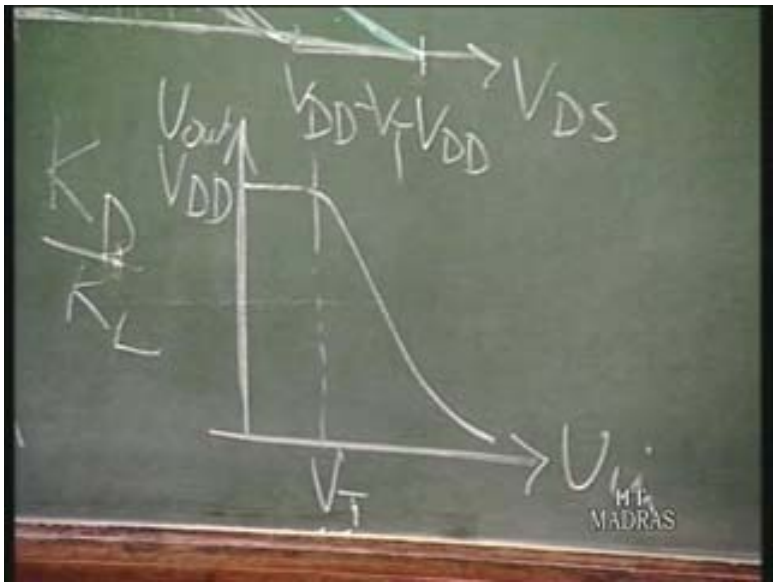

So it is similar to $v_{DD.}$, it is in fact better than the saturated load but there is a problem. the problem is that you must have two power supplies, one for the drain and one for the gate which is not very good thing to have because you will unnecessarily increase the cost of the system because we have to have two power supplies, you have to have more interconnections because again you have to takeout two power supplies and that creates a lot of problems. So from that point of view, it is not good thing having two power supplies so we should again try to eliminate. So how to do it?

So the next type of inverter which came was with a different type of device altogether which is called I mean this particular device is called the depletion, it is called a depletion mode load. Now all the transistor characteristics or the devices which we have been discussing now come under the category of enhancement mode devices. That is the threshold voltage of such a device is positive, greater than zero and at $v_{in.}$ or $v_{G.}$ equal to zero, the device is off. It does not conduct that is $I_{D.}$ is equal to zero when $v_{GS.}$ is less than $v_{T.}$ when $v_{T.}$ is positive so it is a normally off device. The difference with a depletion mode load is that it is a normally on device that when $v_{GS.}$ is equal to zero, the transistor conducts and in fact you have to apply a negative voltage to switch it off.

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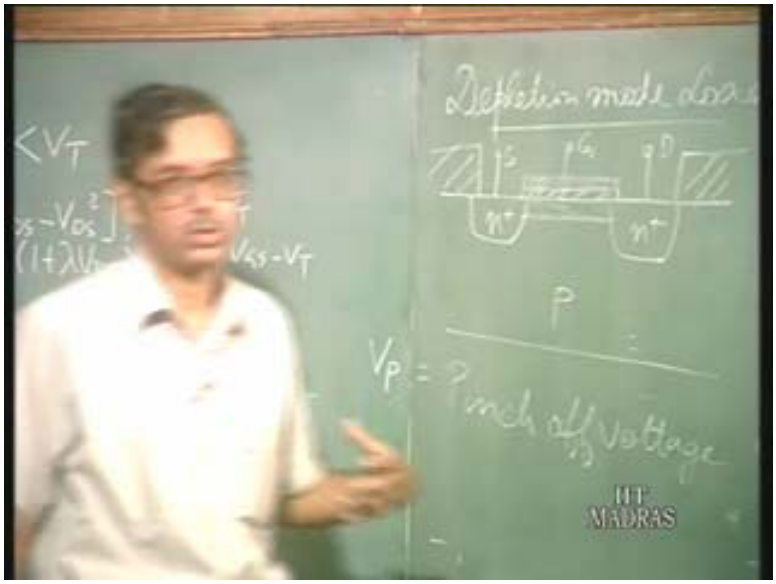

The construction of the device or the cross sectional view of the device is something like this. In a normal n channel MOSFET, you have the structure like this. This we have seen already so this is the oxide, this is the metal. So you have MOS structure, this is the end source so this is the source, this is the gate, this is the drain (Refer Slide Time: 44:13). So you have to apply a positive gate voltage to create the channel that is the channel consisting of electrons.

Now here in a depletion mode transistor what you do is, you already create a channel that is you use ion implantation to create an n channel here. That is this region is already doped n type at the surface. When the gate voltage is zero say when you apply a drain voltage there is a current flowing, this behavior as a resistance. Now what you have to do is, if you go on increasing the gate voltage above zero, you have larger concentration of electrons. if you are positive here you introduce and the current goes on increasing just like in the case of a enhance type device but what you do is when you apply negative gate voltage, when the gate voltage is negative here you should induce positive charges in the semiconductor. What happens really is the electrons from the surface, they get repelled from the surface.

So if you apply a negative voltage here, it's like a capacitance so you should have positive charges in the other plate. That is the electrons get repelled from the surface here and you create what is called a depletion layer and the depletion layer thickness will go on increasing, as you make the gate more and more negative. So at a particular negative gate voltage called the pinch off voltage, the channel will be pinched off when the depletion layer covers the entire channel and the current goes to zero. so you have instead just likely you have a threshold voltage, for a n channel device enhancement type device here you have what is called a pinch off voltage that is given by the symbol $v_{p.}$, $v_{p.}$ is the pinch off voltage.

Basically what happens is if you go on increasing the negative voltage, the depletion region increases and it goes like this. Suppose if you have a gate voltage of zero volts, what is happening is and you are applying a positive drain voltage. As you as you are increasing the positive drain voltage at the drain end of the channel, so this is becoming more and more positive. So what about the gate to channel voltage. It is becoming more and more negative, the gate is becoming more and more negative with respect to the channel.

So again what happens is if you go on increasing the drain voltage up to a particular value that is basically the gate to channel voltage at the drain end when it becomes equal to the pinch off voltage, the channel is pinched off. The depletion region keeps widening at the drain end and the channel gets pinched off and that is why you have a saturation of current just like you have in the enhancement type devices. In order to model this depletion type device, we use the same set of relations. we have the same set of relation because it's almost identical expect for the fact that instead of threshold voltage here you have a pinch off voltage and this pinch off voltage is going to be negative.

That is if you look at this equation here that id is equal to be zero, when $v_{GS.}$ is less than the pinch off voltage which is negative that is it is more negative than the pinch off voltage then the current is zero and when the gate to source voltage is less negative compared to the pinch off voltage, you have a channel. It is the similar type of relations only that I mean you can think of it in such a way that the threshold voltage is not positive but just negative number and then it behaves in a similar fashion. So that is what is a depletion type device and this depletion type device we shall see depletion mode load device gives a much better characteristics compared to all the load devices which we have to talked of so far.

In fact for a long time a lot of circuits were fabricated using the depletion mode load till I mean the CMOS actually took over, in fact the early microprocessors like 8085 they were fabricated using the nMOS logic with a depletion mode load. So we shall take that up next class.