Digital Integrated Circuits
Dr. Amitava Dasgupta
Department of Electrical Engineering
Indian Institute of Technology, Madras
Lecture – 23

Heterojunction Bipolar Transistor based ECL; ECL gate array; cont., ECL – TTL interfacing; MOSFET characteristics

We shall continue our discussion on ECL gates. We have seen in last class how one can actually model the propagation delay in its real gates that is by using summation of the different time constants in the circuit as well as the transit time and one can actually optimize the device by reducing the different resistances and capacitances. We have also seen that a self-aligned structure is going to give higher speeds that is lesser delay because of the fact that the parasitic resistances and capacitances are reduced.

We have also seen that for a particular logic swing there exists an optimum value of the current source which gives the minimum delay. If you want to operate the gate for a minimum delay we have to operate it at the particular value of the current. The logic swing is the product of the current source as well as the load resistance. You can have different combinations of current source and load resistance to give the same logic swing but one has to optimize the value of the current source in order to operate at the lowest delay point.

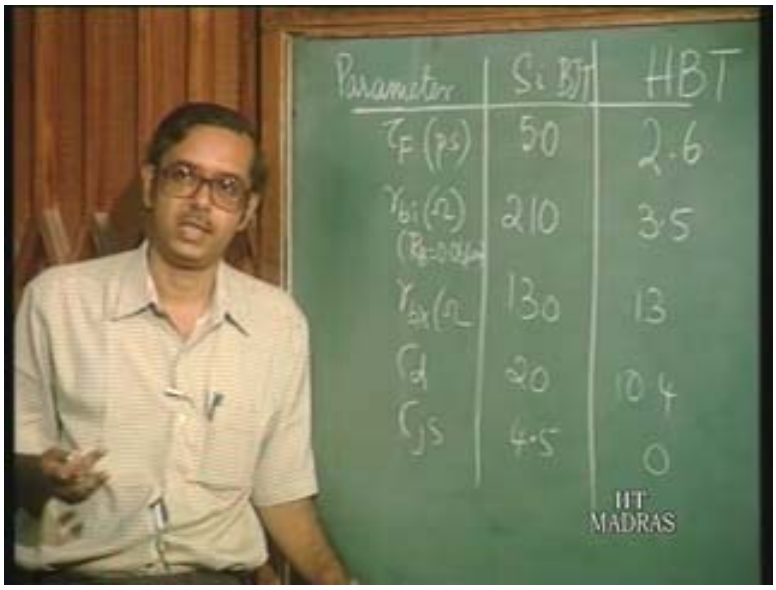
We have seen the different technologies, we have seen polyemitter bipolar transistors how they are superior to the normal conventional bipolar transistor and they are used for high speed ECL gates as far as silicon technology is concerned but silicon technology has limitations. So you can go to higher and higher speeds but there is a limitation beyond which you cannot go. How do you break that barrier? The direction people are working now is to use hetero junction bipolar transistors which has the possibility of higher speeds compared to the silicon bipolar transistors.

We have already discussed what is the hetero junction bipolar transistor and how it is different from a normal homo junction transistor in the previous class when we discussed i squared l gates. We shall just look at some of the parameters and compare the values of HBTs with that of a corresponding silicon bipolar transistor and see in which way the HBT performance is going to be superior compared to that of a silicon bipolar transistor, when it is used for an ECL gate.

Now we know that an HBT consist of a wider band gap emitter and we also seen that another important characteristic of an HBT is that the base doping concentration is made very high compared to the emitter and collector doping concentrations with the result that the base resistance is very low because of the high doping concentration. Also these hetero junction bipolar transistors are usually made of compound semiconductor materials that is gallium arsenide based or indium phosphide based or even nowadays you can have silicon germanium HBTs where the base is made of silicon germanium and silicon germanium the mobilities are higher than silicon.

In all these materials, the electron mobilities are higher than that in silicon with the result what you expect is that the forward transit time of the device which is inversely proportional to the mobility that is going to be less in compound semiconductor devices compared to that in silicon. Just for the sake of comparison some of these parameters, just list out; this is some published results. So for one micron devices we have a parameter, we have silicon BJT, HBT.

(Refer Slide Time: 00:09:33)



Tau$_{f.}$ say typical values, tau$_{f.}$ that is the forward transit time say in picoseconds, it is 5 whereas in this case it is 2.6. This implies that this is due to the higher mobility in HBT's. Then the intrinsic base resistance in ohms for silicon say it is 210, this is 3.5. This is for a particular base width, this is 0.06 micron base width, $R_{B.}$ = 0.06 micron. So this is you see the point is the large difference in the intrinsic base resistance. For a HBT it is just 3.5 ohms whereas for a silicon BJT it is 210 ohms that is because of the very heavy doping in the base of a HBT which reduces the resistance.

Then r_{bx} also that is the extrinsic base resistance in ohms, this is 130, this is about 13. This is corresponding to a particular technology but anyway what is important is the numbers. One can just have a look at the numbers and one can see their difference.

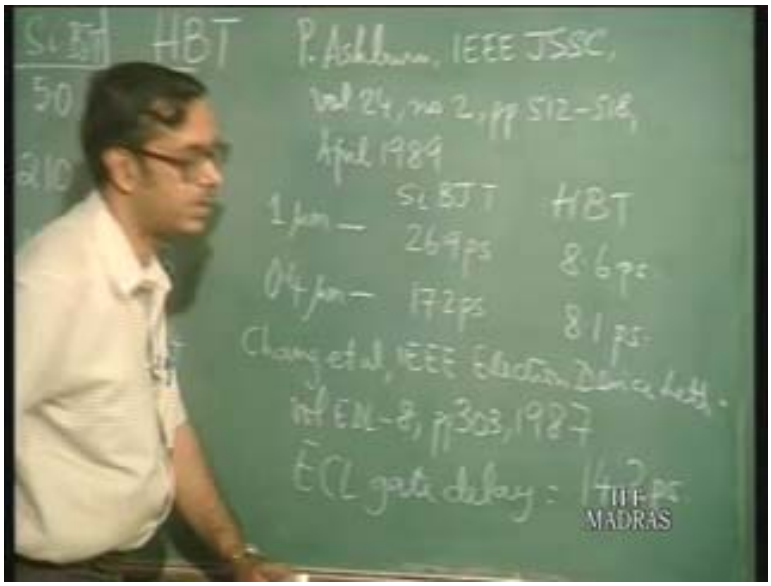
I won't list out all the parameters but some of the parameters where there is a definite difference, even diffusion capacitance. so for an silicon BJT it is 20 whereas this is 10.4, this is around half that in the case of silicon BJT because of the fact that here the base doping concentration is much higher.

The base stored charge in the base is going to be less and also the emitter side, when the base emitter junction is forward bias, the emitter because is lightly doped. most of the stored charge is expected to be on the emitter side but because of the wider band gap in the emitter the charge stored n_i that is intrinsic carrier concentration is less so the charge stored also would be much less. So this is the diffusion capacitance another interesting thing is the substrate capacitance c_{js}. So this one is around 4.5 but this is 0. Here for an HBT, the substrate capacitance is zero. Why? Because in HBT's, the substrate on which the device is fabricated is a semi insulating gallium arsenide substrate.

The substrate is actually a semi insulating gallium arsenide substrate. gallium arsenide because of its very wide band gap, one can have almost semi insulating means almost an insulating substrates that is one can have very high resistivity substrates on which the device is fabricated and if you have very high resistivity substrates almost insulating substrates, the capacitance is going to be almost zero because you can imagine that the depletion region is going to be infinitely wide, it is going to be very large and with the result the capacitances are going to be very small. So this is another advantage of HBT's that the devices are fabricated on semi insulating substrates. so the substrate capacitance is almost zero.

These are some of the reasons why an HBT is expected to give a superior performance compared to silicon bipolar junction transistors. In fact some simulations have been carried out and just I give the reference, I think also Peter Ashburn, another IEEE journal of solid state circuits volume 24, number 2, pages 512- 518, April 1989. He has found that for the minimum one micron technology that is the minimum dimension of one micron, the difference silicon BJT based ECL is going to give a delay of 26.9 nine picoseconds whereas HBT based technology is going to give a delay of the minimum is around 8.6 picoseconds.

(Refer Slide Time: 00:14:09)



For a 0.4 micron technology, this can go down to 17.2 picoseconds. This doesn't make so much of the difference but anyway still much better, around 8.1 picoseconds. So this is some simulations and we see that this is some of the expected results. So you see that this is the order of delays, one can expect from ECL gates around less than 10 picoseconds. In fact there is a paper, again I give the reference chang and others IEEE electron device letters, volume EDL – 8, page 303, 1987.

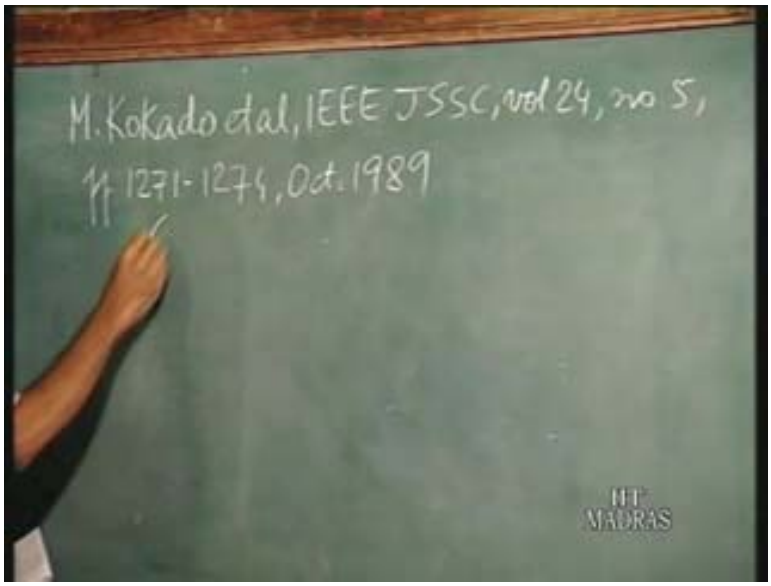
So way back in 1987 in fact where HBT based algas gas HBT based ECL gates were fabricated and delays experimental. This was actually fabricated were this is simulation, this was actually fabricated device and delays of ECL gate delay of 14.2 picosecond was achieved. This is some of the interesting results so this will give you an idea of the order of the delays one can expect from ECL gate. In fact entity corporation of Japan have also claimed that they have fabricated ECL gates with delays as low as 5.5 picoseconds. So that is also HBT based. Heterojunction bipolar transistor based so that is the order of delays, one is talking of nowadays in terms of ECL gates and of course ECL gates as you know is fastest logic family and so the drive is towards lower and lower delays and higher and higher speeds.

So the next thing I would like to talk is, what about large scale integration? The problem with ECL gates is we have seen in general is the power dissipation. So ECL gates are not really conducive to make large scale integration that is very large chips that is very highly complex chips but there are some companies which have come out with gate arrays, ECL gate arrays. I hope you know what is a gate array. Gate array is a chip where all the devices and the individual gates are prefabricated and the only thing which is left is the interconnections. It allows the customer to design his own interconnections to get whatever function he wants to realize.

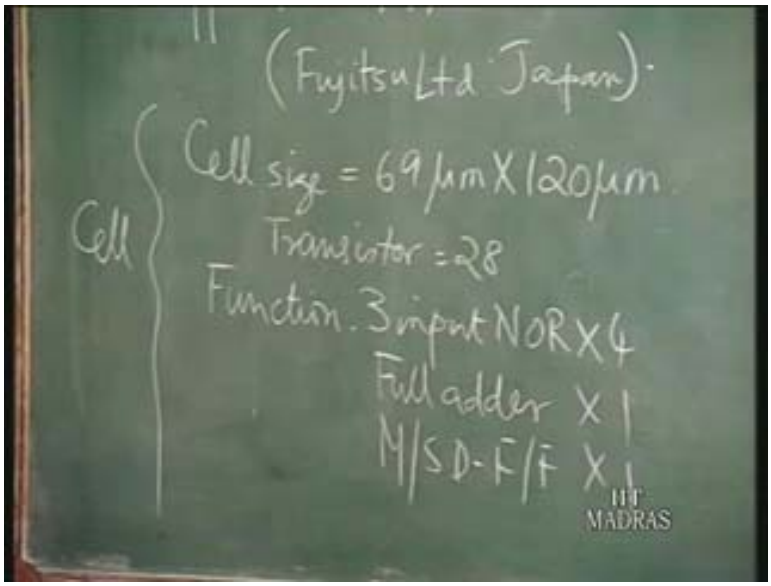
So basically all the gates and whatever flip flops etc are prefabricated, only the metallization is what has to be done. So I just give you at least one of the existing gate arrays which are available, also to give you an idea of the level of integration that has been achieved in the ECL gates. The reference I will give you IEEE journal of solid state circuits, volume 24, number 5.

So this actually is a paper from the Fujitsu Company, Fujitsu of Japan which you may have heard the name of this company. So it explains that this is the gate array available from this company used by a customer. In this particular gate array which is described in this paper in ECL gate array, silicon based ECL gate array, in the gate array you have a number of cells. Its each cell, cell size is 69 micron into 120 micron.

(Refer Slide Time: 00:17:21)

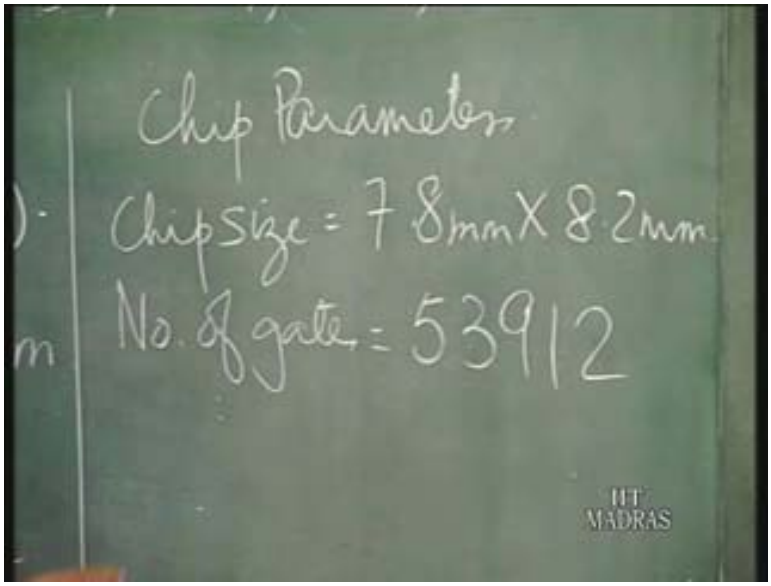


(Refer Slide Time: 00:18:59)



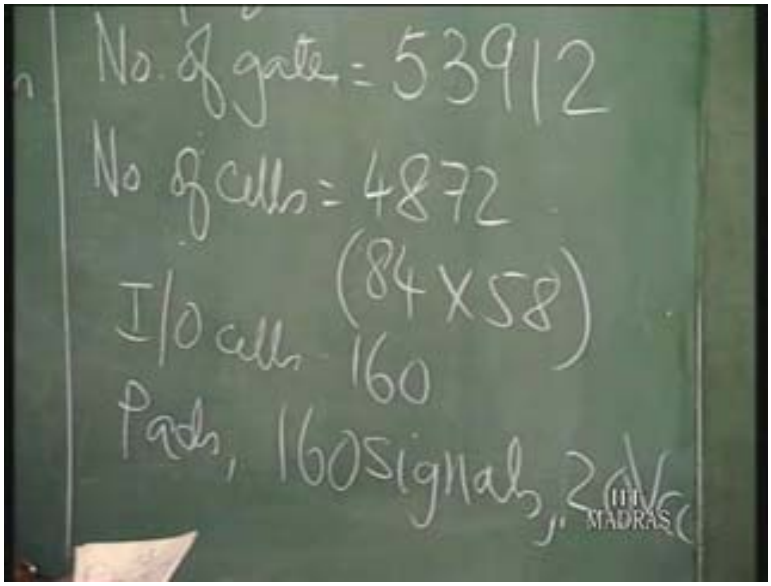
Each cell consist of 28 transistors. So this is a regarding each cell, so this is each cell. 28 transistors and the function which are there in each cell is 3 input NOR into 4. There are the basically 4, 3 input NOR gates, one full adder and one master slave d flip flop. So this is what is contained in each cell. So 4, 3 input NOR gates, one full adder and one master slave d flip flop and total of 28 transistors in an area of 69 micron into 120 micron. Chip parameter: chip size 7.8 mm into 8.2 mm.

(Refer Slide Time: 00:19:54)

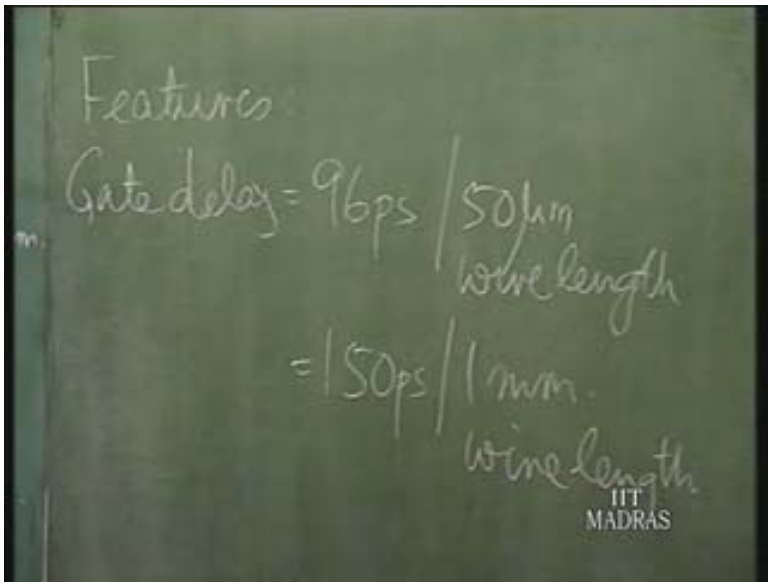


Number of gates, this is an equivalent number of gates because exact number of gates is very difficult to find out, 53912 and the number of cells is 4872 in an array of 84 into 58. So 84 into 58 array of such cells are there, we have seen what is there in one cell. So there are 84 rows and 58 columns of such cells, total number of cells being 4872. So this is the total number of cells which are there in that chip and in addition you have some I/O cells that is for interfacing 160 and there are number of pads 160 per signal and 20 for power supply v_{cc}. so 180 pin Ic.

(Refer Slide Time: 00:20:55)



(Refer Slide Time: 00:21:53)

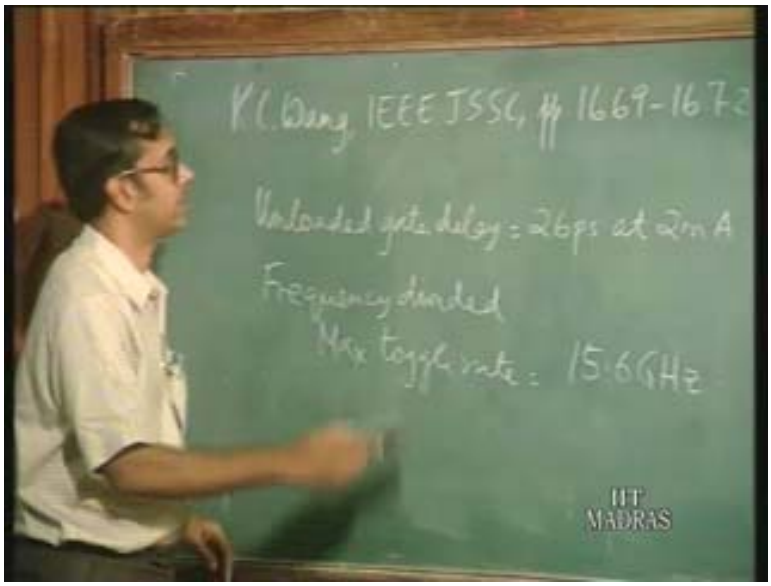


This is about what is there in the cell but what is also important to us is what is the performance, the features is gate delay 96 picosecond. For 50 micron wire length and 150 picosecond for 1 mm wire length. See that is the delay is dependent on the length of the wire which we are using at the output. When you make an interconnection from one chip to the other, you have to connect it with a wire or interconnection basically. Now that interconnection will also have a capacitance of its own which affects the delay.

So if you have a 50 micron wire length that is from one gate output say to an input on the other gate is 50 micron wire then the delay would be around 96 picoseconds. If it is one mm that it would go up to 150 picoseconds so that is the sort of delays which is there in the chip. So it is just to give you an idea alright of the present state, although its quiet old now but anyway this is the sort of gate array which are available and the delays. This is in fact already about 10 years old so one expects that things have improved since then.

HBT based ECL gates has also been announced and they have superior performance in terms of delays. I just give one example, just to give you an idea again. So the reference is K. C. Wang, this page is 1669-1672, November 1991. So basically they have 500 gate arrays and in that there are 144 logic cells and the important thing is the delays, the unloaded gate delay is equal to 26 picosecond at 2 milli amperes per gate current flow and they have fabricated frequency dividers with a maximum toggle rate of 15.6 gigahertz. These are some of the results which shows you the level of or the speeds one has achieved with ECL gates. So we can see as a comparison, the HBTs are obviously much faster compared to the silicon BJT based counter parts.

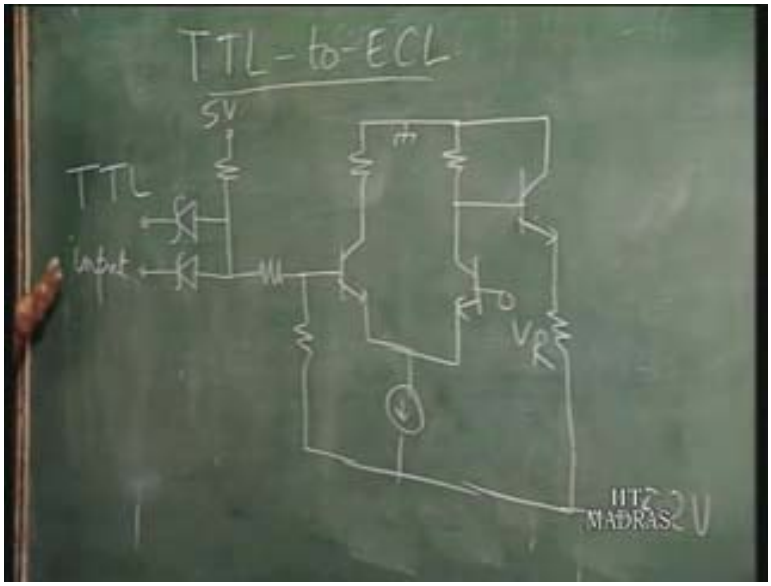
(Refer Slide Time: 00:25:39)



So with that we almost come to the end of this section on ECL gates. This is just one more thing I would like to add before we conclude on ECL gates. Again as we did in the case of i squared l, you see that the voltage levels in ECL gates are somewhat different from the TTL voltage levels and the TTL voltage level is often taken as a standard. So one may have to have interfaces which convert the TTL levels through ECL levels. That is you have a TTL level output which you want to feed to an ECL gate or on the other hand if from an ECL gate you want to take an output and which must be an equivalent to a TTL level.

So I will just discuss this level translation that is TTL to ECL level translation and ECL to TTL level translation just some circuits how it is done before we conclude. So TTL to ECL. So the input you have TTL levels so you want to drive an ECL gate. How do you do that? So basically you have a TTL level input here say, so this is just like the input of LSTTL gate, you have 5 volts here and then what you do is from here you have a sort of potential divider network and this goes to an ECL type of input here.

(Refer Slide Time: 00:28:43)

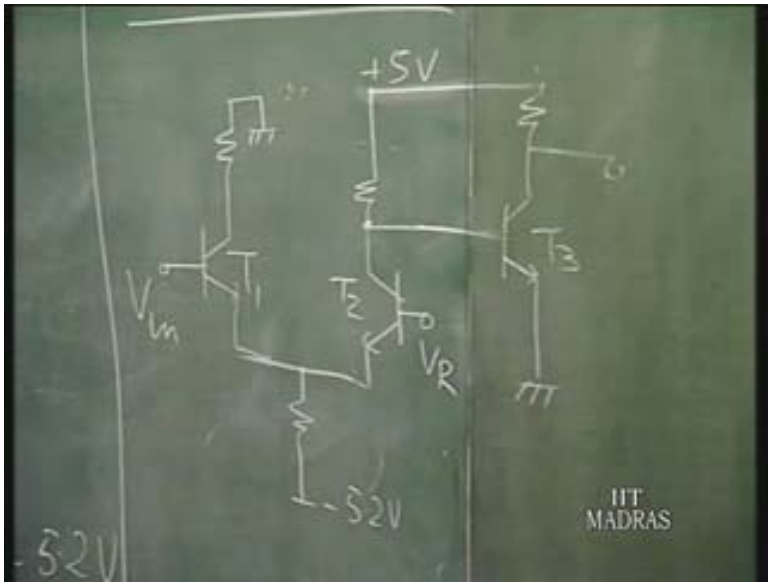


This is an ECL type of input, so this is the reference voltage, this is the input here, this is ground so this is just like an ECL gate. So this $v_{R.}$ say whatever is the $v_{R.}$ of the ECL gate and then you have the emitter follower at the output. This is minus $v_{ee.}$ that is minus say 5.2 volts which is the standard for ECL say. What you have here is this is 5 volts so $v_{R.}$ will be a negative voltage, this is just like an ECL gate. So what you have to do is here if the input, this is the TTL input. So TTL input means the logic high, it will be close to 5 volts or say usually 3.6 is taken as the TTL input voltage, the high voltage and logic low will be 0.2 volts or so.

When this voltage is high, here the voltage is going to be almost close to 5 volts and you have basically a potential divider network here and if this voltage here at the base of this transistor is higher than the reference voltage then the transistor $T_{1.}$ here is going to be on and $T_{2.}$ is going to be off and here you have the corresponding ECL level voltage and if this TTL input goes low, this point here is going to be correspondingly lower that is the base of $T_{1.}$ because here the voltage is going to be less. So basically you have to choose the potential divider network in such a way that the voltage at the base of $T_{1.}$ is less than the reference voltage.

This end it is minus 5.2 so this becomes more negative compared to $T_{2.}$ when this input is low and so this $T_{1.}$ cuts off, $T_{2.}$ is on and you have the logic high at the output and the output which you have corresponds to an ECL level. The input you have TTL level, the output you have ECL level. Similarly you want to do the other thing that is ECL to TTL translation, so what is going to be circuit?

(Refer Slide Time: 00:32:48)



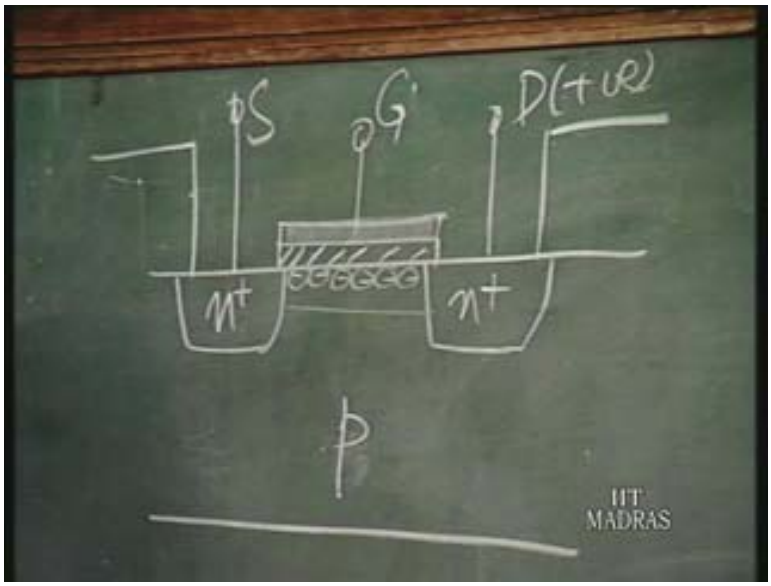
What you have is you have an ECL type of input here, this is ground. This is minus 5.2 volts which is the ECL input, so you have the input here. This is the ECL input which you are giving here. Here this voltage is plus 5 volt and this will go to the base. Now let us see what is happening here. Here you have the reference voltage, now if v_{in} the input voltage is high T_1 is conducting and T_2 is off. Here you at the input side this is just like an ECL gate. If the input is high, T_1 is conducting T_2 is off. So here you see that this right hand branch of the ECL gate here it is connected to plus 5 volts. So if T_1 is conducting T_2 is off, you have a circuit like this which means that the base of this transistor T_3 it is connected to v_{cc} through a resistance and this T_3 is going to conduct and output is going to be low.

On the other hand if v_{in} is low that means $T_1$is off, T_2 is conducting and there is going to be drop across this resistance and this drop is going to be equal to the current which is flowing into the resistance value. So you can adjust that this resistance value on the current, the product so that this drop is large enough and the input voltage at the base of T_3 becomes less than; so if this drop is say around 5 volts or so. So this voltage at the base of T_3 is going to be zero volts which is going to cutoff that transistor T_3, the output is going to be high and so the voltage which you get here corresponds to TTL levels.

So at the input you have ECL levels that is the voltage, the ECL levels means the logic the voltages which we have already discussed in the input output characteristics. So here you have the ECL levels and the output you are going to have the TTL levels. This type of circuitry can be used to convert ECL levels to TTL levels and here from TTL levels to ECL levels. With that I think we can conclude our discussion on ECL gates.

So we have seen what is the circuit configuration of an ECL gate and the basic properties of ECL gates as well as how people have worked to improve the properties especially the delays because ECL gate is supposed to be the fastest logic family and so it is the fastest logic family and so it is very important to achieve higher and higher speeds. The maximum speeds which can be achieved. Then we conclude this section of ECL gates, in fact we have gone through the different bipolar logic families that is the TTL i squared l and the ECL and now we should move on to the other type of logic families or the logic circuits based on MOSFET's. That is a different device altogether. We shall see first what is a MOSFET, you are all aware but I will just draw the cross sectional view of an n channel MOSFET.

(Refer Slide Time: 00:38:28)

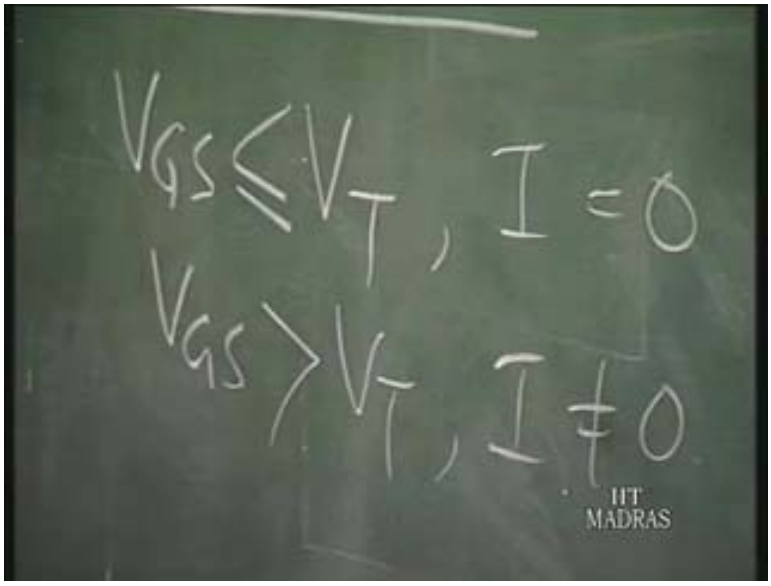


You have the MOSFET here so an n channel MOSFET, we will have a p type substrate n plus n plus, these are the source and drain contacts, this is the gate region. So this hatched region is actually silicon dioxides so this is an oxide. On the top of that you have metal. So that is why it gets its name metal oxide semiconductor is MOS and FET is field effect transistor. So this type of device you can have n channel device or p channel device. In an n channel device the substrate is p type, what happens is when you apply a positive voltage on the gate because of the capacitance here, the negative charges are to be induced in the semiconductor. What happens initially is the holes which are the majority carriers in the p type semiconductor are repelled from the surface initially and this creates a depletion region in the sense the holes are repelled and the acceptor ions which are negatively charged are uncovered.

So you have a depletion region in the surface and then as you go on increasing the positive voltage on the gate, the electrons which are the minority carriers in the semiconductor are attracted to the surface and a channel is formed and this electrons which are attracted to the surface cannot penetrate the oxide and there is a large number of electrons on the surface and this electrons creates a channel of the surface and when you apply a positive voltage on the drain compared to the source, the electrons can flow from the source to the drain and you have a current.

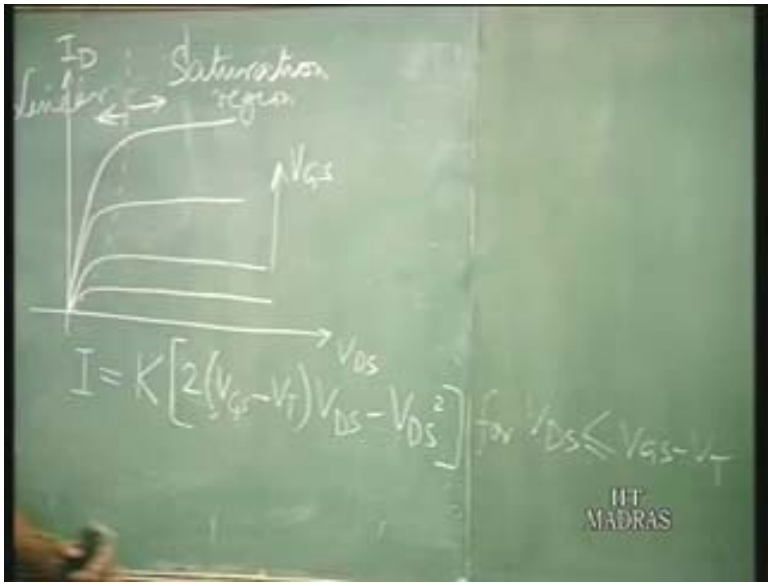
One important parameter for the MOSFET is the threshold voltage v_{T} .which is the minimum gate voltage, required gate to source voltage required for conduction. That is when v_{GS} is less than v_{T} the current will be equal to zero this is what we assume and in fact v_{GS} less than equal to v_{T} and then v_{GS} is greater than v_{T} then I is not equal to zero so you have a drain current flowing. So this v_{T} is a important parameter of a MOSFET.

(Refer Slide Time: 00:39:12)



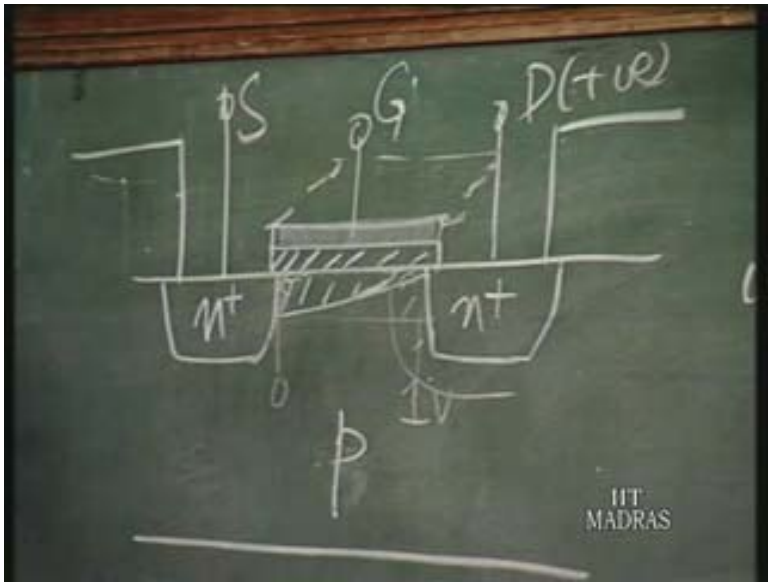
Also for a MOSFET the characteristics if you plot the drain current versus the drain to source voltage characteristics is something like this. This is for different gate voltages so increasing gate voltages. In the MOSFET all the voltages are measured with respect to the source when we say drain voltage it is actually the drain to source voltage that is how much is the drain voltage positive with respect to the source.

(Refer Slide Time: 00:44:37)



Gate voltage is actually the gate to source voltage. So if you see that for a particular gate voltage what happens is initially the current increases with increase in drain to source voltage and then the current saturates. Each of these characteristics is for a particular gate voltage. This part of the characteristics on this side is called a linear region. So this side is the linear region and this side is called the saturation region. What actually happens is when you keep on increasing the drain voltage there is a drop in the channel from the source to the drain end. Say for example if you apply a 1 volt at the drain, the voltage at this end of the channel is going to be 1 volt whereas this end is 0 volt.

(Refer Slide Time: 00:46:40)

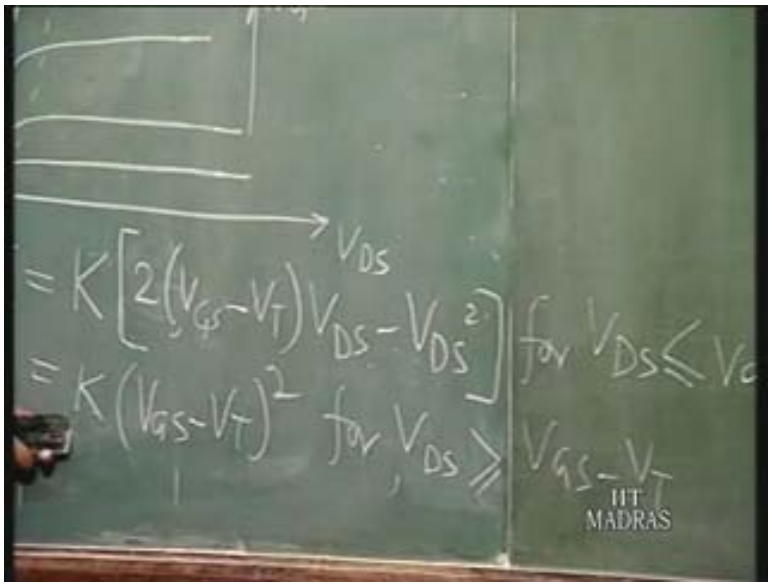


So this drop in the channel actually reduces the gate to channel voltage. The channel is always going to be sort of wider at the source end and less at the drain end because the gate to channel voltage is going to be less at the drain end and if you go on increasing the drain voltage, ultimately the gate to channel voltage here at the drain end will become equal to the threshold voltage.

After that what happens is you have a situation like this, the channel is just what is said to be pinched off at the drain end. Any further increase in drain voltage basically what happens is this pinch off point moves towards the source and the remaining voltage is dropped in a depletion region here. So the voltage drop across the channel is fixed to v_{GS} minus v_T and that is why the current becomes almost constant here, after it reaches saturation but there is a small increase in current it is not actually constant. There is a small increase in current because what happens is the effective channel length is reduced.

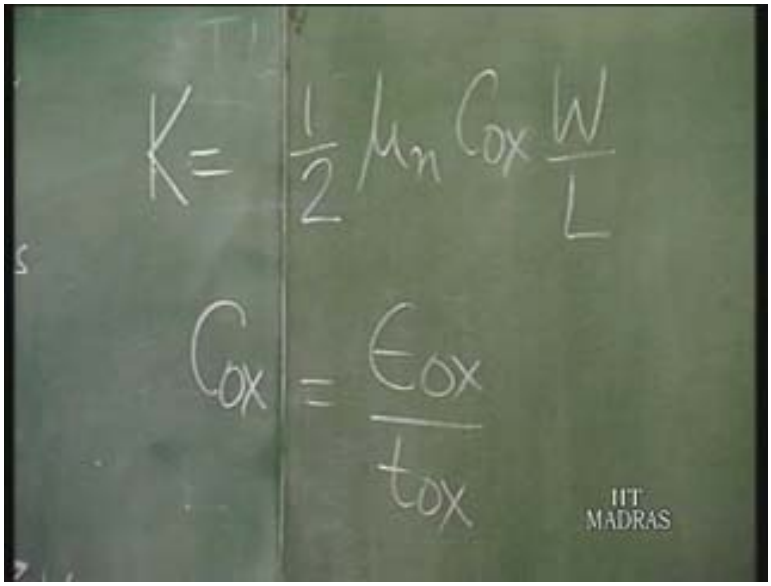
So this is the characteristics of the MOSFET. there are different models of this MOSFET current voltage characteristic but we shall take a simple model for our analysis whatever we do in this course which is called the square law model and the current is given by according to this model k [twice (v_{GS} minus v_T) v_{DS} minus v_{DS} square] where this is capital v_{GS} where v_{GS} is the gate to source voltage and v_{DS} is the drain to source voltage. This is for v_{DS} less than equal to v_{GS} minus v_T. When v_{DS} becomes equal to v_{GS} minus v_T or more than that what happens is this term if you see that when v_{DS} is equal to v_{GS} minus v_T, this becomes equal to v_{GS} minus v_T whole square.

(Refer Slide Time: 00:45:22)



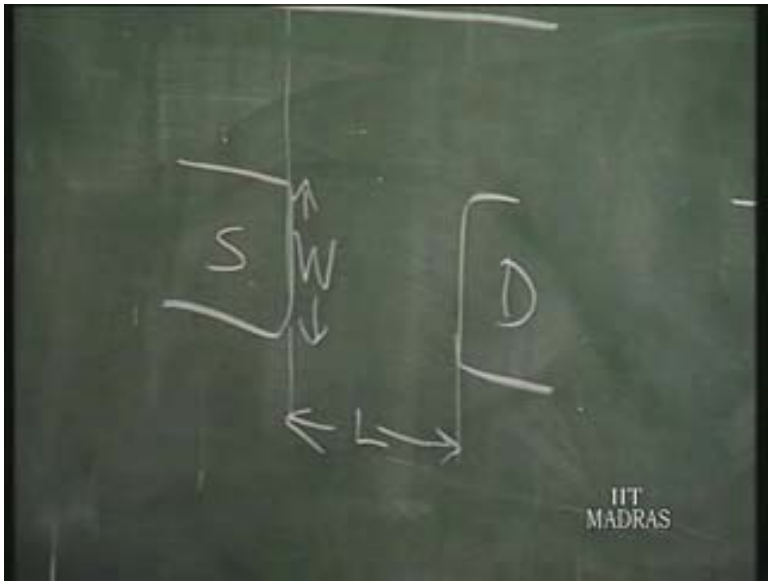
So this is equal to k v_{GS} minus v_T whole square for v_{DS} greater than equal to v_{GS} minus v_T and this k which is called the trans conductance parameter is given by k is equal to half mu_n c_{ox} W by L, mu_n is the electron mobility, this is for an n channel device, it is the electrons which flow from the source to the drain. so this is equal to mu_n, c_{ox} is the oxide capacitance that is the gate oxide capacitance and c_{ox} is given by epsilon ox by t_{ox} where epsilon is the dielectric constant of the silicon dioxide which separates the gate metal from the semiconductor and this is the thickness of the oxide. So that is c_{ox} and w by l, w is the width of the MOSFET channel and l is the length of the MOSFET channel. So if you look at this MOSFET here, the length is the distance between the source and the drain and w is the width that is the other dimension.

(Refer Slide Time: 00:46:05)



In fact if you have a top view of this device, this is say source, this is drain. This is going to be the length that is the distance between the source and drain and this is going to be the width.

(Refer Slide Time: 00:47:03)



So it is quite obvious that as the width increases, the current is going to be more and as the length increases, the current is going to be reduced because basically the channel behaves as the resistance and the resistance of the channel we know that if the channel resistivity is rho that the resistivity resistance is going to be rho l by a. So the larger the length the resistance is more which means the current is going to be less.

So the current is proportional to w by l ratio that is where an important parameter of a MOSFET w by l ratio. It is proportional to, this width to length ratio of the MOSFET the k is proportional to w by l. So the current is proportional to the mobility so the current is going to go up with mobility. Obviously it also increases with the oxide capacitance that is if you basically reduce the thickness of the oxide region, the $c_{ox.}$ will go up that is oxide capacitance is increased. That is also understandable because the current which flows depends on the charge in the channel. If we have more electrons, we have more current and the charge in the capacitance q is equal to cv.

So for the same gate to source voltage or the gate voltage which we have applied, if you have a larger capacitance you have more charge and if you have more charge you have more current. So it is proportional to the oxide capacitance and it is also proportional to w by l ratio. This is the simple model of the MOSFET which we should generally take up in our discussions when we analyze the different circuits. I will go into more details if it is necessary to have more complicated models but for the time being we will stick to this particular model which is a simple model and is sufficient to understand most of the effects in a MOS based logic circuit.

Of course I must point out that this is not very accurate. If you want to have more accurate results, we must take a more complicated models but that is more time consuming in the sense that any simulation etc is going to be more and more time consuming. With that we close today.