Digital Integrated Circuits
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Lecture – 20
ECL 100k series; Stacked ECL gates; D-F/F

Last class we had analyzed the circuit for the ECL 10 K series which is the commercially available ECL gate. So just like in the TTL gate you have the advanced gates, here also in the ECL you have an advanced series called the ECL 100 K series where some modifications have been made with respect to circuit but the major advancement is in the form of technology. We will come to that first let us take up the circuit aspect. So in the black board here we have the circuit for the ECL gate of the 100 K series.

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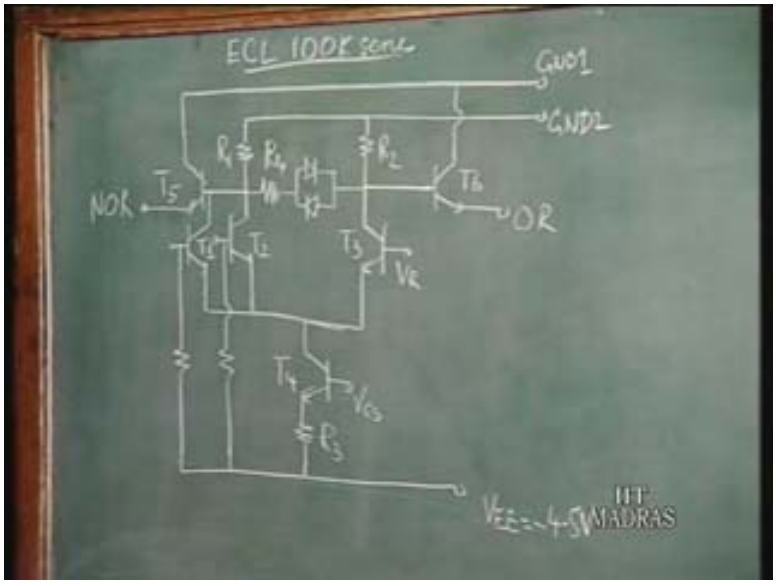

Now as you can see that the modifications on the circuit, there is a small part here which consists of 2 diodes connected and with the resistance here. Now in the purpose of this is basically for temperature compensation that is the circuit outputs should not depend on temperature. Just I will explain it. That is we know that in a PN junction, the voltage drop changes with temperature. It reduces in fact by about 1.5 milli volts per degree centigrade. So if you assume that what happens is if the temperature raises, so this is instead of a resistance only as a current source, here you have a proper current source, this is a current needed type. So what happens is if you assume here that the voltage V_{CS} is fixed. Now as the temperature goes up this base emitter drop is going to change say by 1.5 milli volt per degree centigrade. So which means that the current flowing here is going to change, the emitter current of the transistor is going to change and you have a corresponding increase in collector current which means that the value of the current source is going to change.

Now if you assume that the left hand branch is conducting say that is for example if T_2 is on. What it means is that there is going to be a larger current flowing through the left hand branch through this resistance R_1 and if we adjust the current and the resistance in such a way that here the drop is around say of the same order that is 1.5 milli volt per degree centigrade, the drop here increase by 1.5 milli volt per degree centigrade. This would compensate for the drop change in the V_{BE} of this transistor. So this V_{BE} is going to reduce, so the output voltage here remains the same. The drop here goes up whereas this goes down by the same order. So this output voltage remains the same. Now what happens at the other output? See if this voltage changes say by 1.5 milli volt per degree centigrade with increase in temperature, there is going to be a current flowing in this path and this current is also going to increase.

In fact this diode here in this path also has same temperature dependence of V_{BE}, of the drop across the diodes. So basically there is going to be a drop corresponding to say three milli volts per degree centigrade and what is going to happen is, if you assume R_2 is equal to R_4 because of this increased current flow there is going to be a larger drop here across this R_2 by the same 1.5 milli volt per degree centigrade that is the 3 milli volt per degree centigrade is going to be divided between R_2 and R_4. So at this point also we have an increased drop corresponding to 1.5 milli volt per degree centigrade which compensates for the reduction in V_{BE} of this transistor by the same margin, by the same amount so with the result the output remains fixed irrespective of temperature. So with this circuitry basically the output voltage variation with temperature is reduced. So that is the purpose of this, so we have an additional circuitry also I have not drawn it. This voltage generation circuits for V_R and V_{CS} are properly temperature compensated so that these voltages are fixed with respective to temperature. So these are the modifications in the circuitry in this series.

So the other point, other modification which you see here is that instead of a 5.2 volt power supply, minus 5.2 volt this is minus 4.5 volts, so the power supply voltage has been reduced primarily to reduce the power dissipation. So these are the modifications from the circuit point of view. The other major modification is as I said from the technology point of view these transistors as in the advanced TTL series also these transistors are different transistors in the sense that mostly they employ oxide isolation instead of junction isolation which reduces the parasitic capacitances from the device and also the device dimensions are reduced. Whereas the original transistors where about 6 micron minimum feature size, this is about three micron minimum feature size and you know that with the reduction in size all the capacitances are going to go down which will result in lower delays and higher speed of operation. so this is the ECL 100 K series which has got superior performance compared to the ECL 10 K series and the data is power dissipation of this K is 40 milli volt per gate and the propagation delay is 0.75 nanoseconds and which corresponds to a power delay product of thirty picojoule which is less than the 10 K series.

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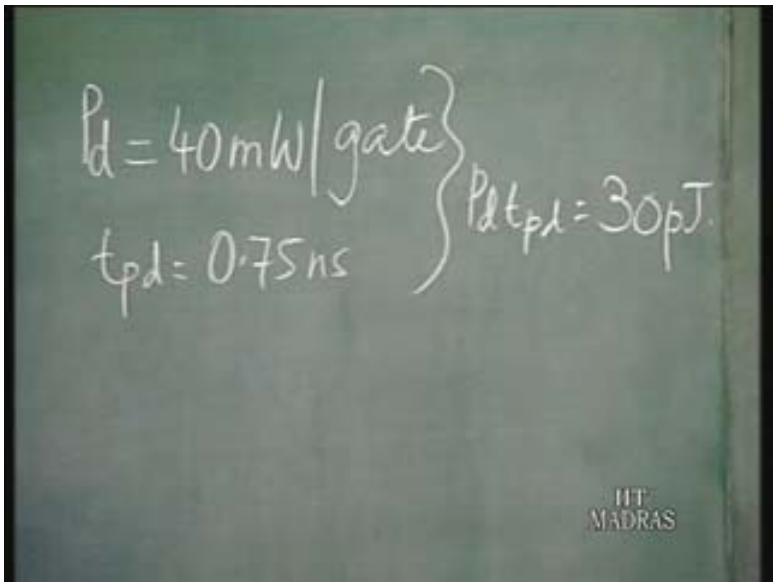

So you see that this is real sub nanosecond gate which has been achieved and this is available commercially. So now what we have seen is the ECL gate, the speed performance is quite good that is the propagation delays are quite low but the major problem with respect to ECL gate is its power dissipation. That is it has got very large power dissipation that is the problem with ECL gates and there has been a lot of effort to reduce this power dissipation. So we shall now take up those aspects, how to reduce the power dissipation in an ECL gate. One of the ways to reduce the power dissipation of an ECL gate is to improve the functionality of an ECL gate, functionality we mean that if we can achieve more logic function, more complicated logic function using the same power dissipation.

How can we do it? We achieve more complicated logic using the same power dissipation. That is for example whatever with the same power as in a OR NOR gate, if you can achieve more complicated logic then you would say one power. So let us see how we can do it. The way we can do it is by using a stacked ECL gate.
So you are already aware of the stacked I squared L gate, so this is the similar concept as such. So let us see how this works. This is our well known NOR gate structure, suppose we have structure like this and then we have another emitter couple structure like this and this is V_R and basically this is level shift down by 1 V_{on} and here also this level shifting is required.

So this is another input so let us say you have the inputs A B C here. Let us say you have the input S here and this is V_R and this basically would mean it is V_R minus V_{on} where V_{on} is the drop across the diode and of course here also the purpose of this diode resistance combination is to reduce the voltage by one diode drop. So you have this combination, so this is for level shifting purpose. So again you can have the emitter follower as you have normal ECL gate and

here also and have another emitter follower. Suppose I call this $F_{1.}$ and I call this $F_{2.}$ and here it is ground, there it is minus $V_{EE.}$.

So this is the circuit of a stacked ECL gate. Now let us see what is the logic function you get at $F_{1.}$ and $F_{2.}$. We can just write a truth table S say and here we say A or B or C and $F_{1.}$ and $F_{2.}$ are the outputs. That is S, so you have the four possible combinations. Now if you look at this emitter couple structure, the lower part of this stack then this side the voltages are just level shifted down by one diode drop. Now if S is high compared to $V_{R.}$ then the current flows in this transistor $T_{1.}$ and $T_{2.}$ is off. So current flows in $T_{1.}$ and $T_{2.}$ is off. Now so the current is flowing in this path. Now you have the emitter couple structure here and the current of this is flowing through this path. Now if A or B or C is high, current will flow in this left branch through resistance $R_{1.}$ and this output F will be low and $F_{2.}$ is going to be high and if A or B or C are low then actually current flows through this transistor which may call $T_{3.}$ and $F_{2.}$ is going to be low and $F_{1.}$ is going to be high.

On the other hand if S is low what happens? This part $T_{1.}$ is off, $T_{2.}$ is on and if $T_{2.}$ is on, the current actually flows through $R_{2.}$ and this is off so there is no current flowing here. So if current flows to $R_{2.}$, $F_{2.}$ is going to be low and $F_{1.}$ is going to be high. So what is the logic here let us see, 0 0 means S is 0 that is S is low that means the $T_{2.}$ is on, so the current flows through $R_{2.}$. So $F_{2.}$ is going to be low, $F_{1.}$ is going to be high because there is no current flowing through $R_{1.}$.

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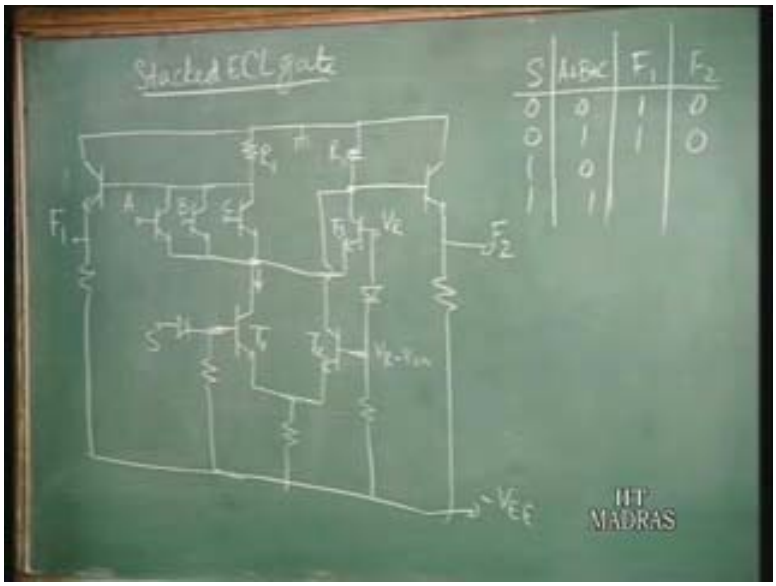

$F_{1.}$ is going to be high, $F_{2.}$ is going to be low. Now again S is 0, basically irrespective of what is A or B or C, $T_{2.}$ is conducting which means that you have the same condition here. Now if S is high that means what is happening is this left hand branch of the lower part of the stack is conducting and $T_{2.}$ is off. Now in this condition if A or B or C is 0 that means none of these transistors, all this is 0 that means $T_{3.}$ is conducting that means current flows through $R_{2.}$ so $F_{2.}$

is low and $F_{1.}$ is high and now if S is high as well as A or B or C is high that means current flows through $R_{1.}$, no current to R_{2} so $F_{1.}$ is low $F_{2.}$ is high. So what is the logic function? So $F_{1.}$ is A or B or C NAND, AND of A or B or C.

So you see basic idea is in this configuration the power dissipation is the same as that of a just the ECL OR NOR gate because you have the same power here, that the current which is flowing is the same as that of an OR NOR gate. This is standard ECL or NOR gate power dissipation is the same but you have got out of these is larger functionality. That is you can make more complicated circuits using the same power as that of an OR NOR gate. If you would have to realize this using OR NOR gate, you would have to have more than gate which would mean that you consume more power.

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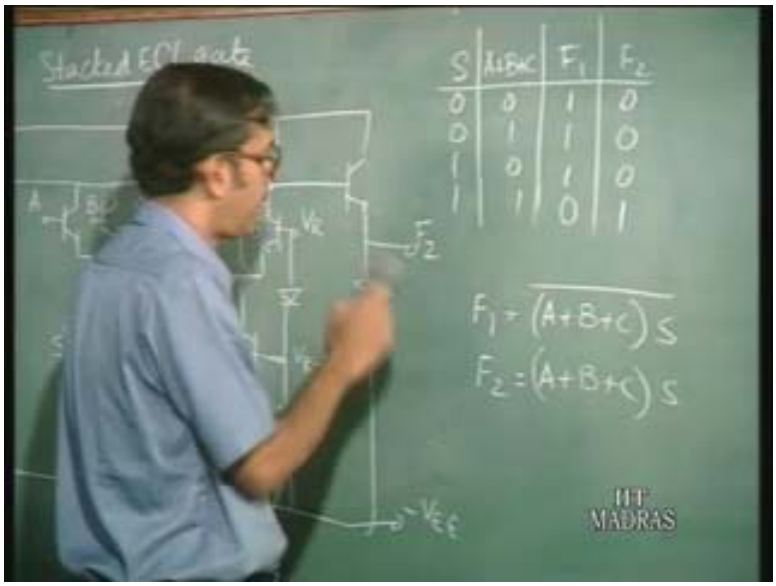

So effectively you are reducing the power consumption by using stacked structures, so this is the whole idea. Now we shall see more interesting circuits. So you can have different combinations of stacked ECL gates by connecting them in different ways and you can get more complicated functions realized. Another interesting circuit which we shall take up now is that of a D flip flop.
This circuit you have clock and clock bar inputs and then you have the similar structure as you have seen for a stack gate. This is one resistance, you have another structure and you have two more transistors in your stack. One of this inputs goes here and the other one goes here. This part is basically for level shifting as you can see, the voltages are shift down by one diode drop, one PN junction drop. These two transistors are for that purpose to the lowest part of the stack, the voltage levels have to be shifted down. So write here the input, here this is $V_{R.}$. Now output must go to level shifted, these are the level shifted transistors. So this is basically the emitter follower transistors, so one goes to the base here, the other output goes to the base here and so this one should come here and this one should come to the base of this transistor and this is going to be Q bar, this is going to be Q. So this is the circuit of a D flip flop basically as

you can see, the power consumption is going to be almost the same as that of a simple OR NOR gate because you have one basic gates structure, the same power except of course you have some emitter followers, level shifting circuit which also will draw some current but they are quite small currents. So this is a power supply.

Now you know what is the D flip flop? D flip flop it has one input D and the other input is clock and you have Q and Q bar output.
When the clock is high then whatever is the D input is transferred to the Q output and when the clock is low then whatever was the previous Q output is retained. The output does not change when the clock is low, the output changes only when the clock is high and when the clock is high, the D input is passed on as the Q output.

So this is the simple level triggered the flip flop, this is not an edge trigger or a master slave. We shall see how we can make a master slave but this is the simple level triggered D flip flop that is when the level clock level is high it is going to pass on whatever is the D input to the output. Now here of course this is the slight modification in that we require both the clock and the clock bar inputs. You can have circuit switch have required just the clock input but I have taken this because normally you can easily get the clock bar outputs. Especially in ECL gates where any output which you get, you also get the complement of the output, you have OR NOR combinations. So clock and clock bar will be available, so you have those two outputs. Now these inputs clock and clock bar are level shifted down by one diode drop and they are fed to the base of these two transistors and so one of them is high and the other is low. Whichever one is high so if the clock is high that means this left hand branch is going to conduct, this left hand transistor for this T_1 is going to conduct and T_2 is going to be off. So basically what it means is that this left hand part of the circuit is going to be operational for the right hand circuit as such is not operational because there is no current flowing there.

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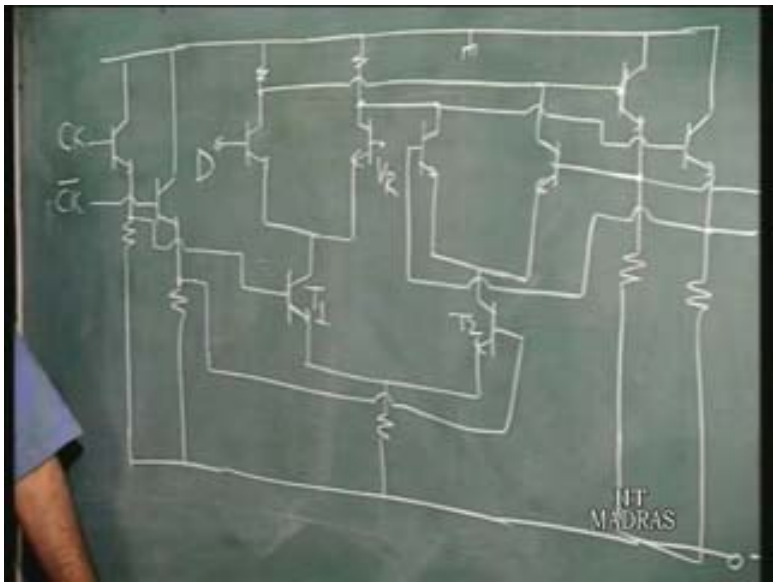

So if you look at this now, this is just like an ECL gate. If D is high if D is high then this output again D and VR these are the two inputs just like any ECL gate, if d is high then say we call this T_3 and T_4, T_3 is on T_4 is off. If T_3 is on then there is a collector current for T_3 which means that this output at the collector of T_3 that is low, this voltage is low whereas the other voltage is high.
So basically you have level shifting here or emitter followers structure here, so this is Q bar and the other one is Q. The other thing which you notice is that this Q bar output which is here is connected to the base of this transistor which let me call this T_6 and Q output is connected to the base of T_5. Suppose the clock input changes, that the clock becomes low. Now let us see. So initially if D is high, Q is high and Q bar is low, I think I made the mistake here (Refer Slide Time: 26:42). Please make this change, this one will come here. Now if D was high, initially Q is high so this is high and this is low but actually these transistors are not conducting because there is no emitter current because T_2 is off but suddenly if the clock becomes low what happens is, this input is high and this is low. So T_5 is on and T_6 is off so basically the current which was flowing in T_3, it still continues to flow through T_5 and since there was no current flowing in T_4, T_6 is not going to draw any current. So again Q bar will be low, Q is going to be high and you retain the original condition.

Similarly if D was low the current would be flowing in this branch, current would be flowing through R_2 and there is no current flowing through R_1. So what happens is Q bar would be low so if D was low Q bar is going to be high, this is connected to this point and Q is going to be low and basically the whole idea is that when the clock is high, T_1 is conducting you get the output corresponding to this ECL gate that is when D is high, Q is high and Q bar is low. At the same point what you are doing is, the same outputs Q and Q bar is fed as inputs to this part of the circuit and one of the inputs is high and the other is low and so what happens is if suddenly the clock goes low then the control is transferred to this part of the circuit, the right hand side part and here the inputs are such that the currents continue to flow in the same resistance. If the current was flowing through R_1, the current will continue to flow in R_1 and so the output really does not change. If current was initially flowing through R_2 when the clock was changed from high to low, current will still continue to flow through R_2 and so the output does not change.

Again when the clock goes high the control is transferred to this part of the circuit, the right left hand part of the circuit and so the output will depend on the D input. Depending on what is the value of the D input, the output is going to change. So this is the D flip flop circuit and it gives an output as expected for a D flip flop. Now in most practical applications, you would want the output to change at one instance of time rather than for the entire period when the clock is high. So what do you have is you have an edge triggered or a master slave type of D flip flop. In this case it is more practical to have a master slave type of flip flop. the master slave flip flop what do you do is you have another D flip flop and here if you have the clock, here the clock is inverted and fed as the clock of the second flip flop. So what happens is when the clock is high, the output changes with respect to the D input but the second flip flop is disabled. So the output, the actual output of this does not change.

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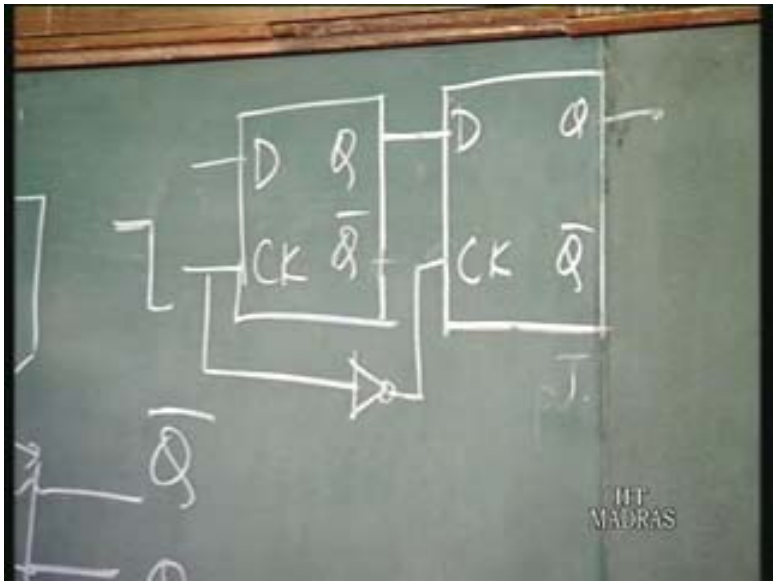

Only at that instance of time when this clock goes from positive to negative, at that instance of time what happens is the first flip flop gets disabled and the second flip flop gets enabled. so whatever is the output here of the first flip flop gets passed on to the output of the second flip flop at that instance of time. After that since the first flip flop itself is disabled, so this if you call this Q one, Q one is not going to change any more with the result the Q two is also not going to change Because the D input for the second flip flop is no longer going to change. So only at this instant of time, when the master clock, the original clock changes from high to low whatever is the value of the D input of the first flip flop gets transferred to the final output. So that is master slave D flip flop.

Here if you have a clock, the output changes only at one instant that is at the falling edge of the clock pulse. It does not change at any other instant. So for many practical circuit it is advisable to have a master slave configuration because you one change per clock pulse. How do you do it? Obviously you must have another such circuitry, another such D flip flop made and how do you make, what changes you make in the second D flip flop? You have to just change the clock inputs. So just like you have fed the clock input here at $T_{1.}$ and the clock bar to $T_{2.}$ We have to just change that we have to keep the clock bar to $T_{1.}$ and the clock to $T_{2.}$ so that will

take care of that and the D input of the second flip flop is going to come from the Q output of the first flip flop. So if you have that, you have a master slave D flip flop. The advantage for this type of gate is that they have much improved functionality that is you have achieve an entire D flip flop with the power consumption corresponding to a single gate. So that is the advantage you have derived using stacked gates. So this gives us some idea of how one can use stack gates to reduce the power dissipation in ECL gates.

In fact there are being other some similar circuit configuration which have been suggested to improve the functionality. We shall take up one of them. Now I mean in fact we shall take up two of them. In the first one which we shall take up is called the EFL, it stands for emitter function logic and this is sort of derivative of the ECL and again the idea behind this is to improve the functionality, So that the power is used more effectively. So what is an EFL, we shall take that up first. So ECL gate you know is basic structure is something like this. We have a current source, this is ground, this is the input, this is V_R . and this output here say is going to many such gates, So these are the fan out basically. So you have one more say, now is the EFL gates always we use the non inverting output. The inverting output is not used that is this output which normally the NOR output not used. So one thing which can be done is that this resistance has no purpose as such. This particular resistance because you are not taking the output from this collector. So you can remove this resistance, so this can be basically shorted with in all the circuit. So this resistances is removed that is one thing which we can do straight away because all the outputs will be taken from the non inverting output. The other thing is here we have that seen that we are removed the emitter follower which we were using in the normal VCL gate, we shall see that later on. We shall see that even with that the circuit performs well, there is no problem. I should take the topic later. With this configuration now what is done is suppose I take this part of the circuit.

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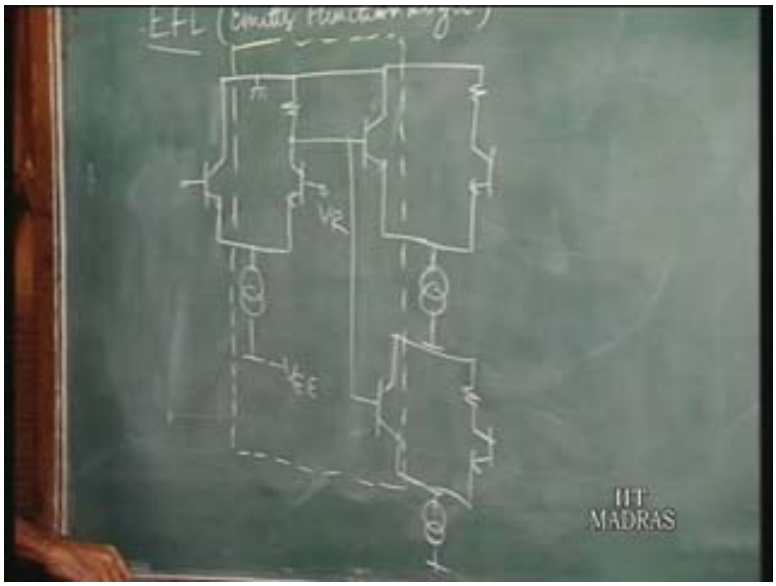

I can redraw it as I have a resistance, I have one current source here, minus V_{EE}, now from this point you have the outputs. so this is gone to the ground, the collector is gone to ground and if you look at the fan outs, for all of them the collectors are gone to ground, the base is common, only the emitters are different, the base is shorted. All the bases are shorted; the collectors are gone to ground so what I can use is a multi emitter transistor because as I said the collectors and bases are all shorted.

I can redraw this part of the original circuit by this circuit. So this we shall see now. Here what do you have is that is if I have a logic a here and here of course this is VR that is the reference voltage. Now if A is high that means what happens is the base emitter voltage of this transistor become lower than the cut in voltage Von then what happens this transistor is off then the output is high. If A goes low, current can flow here and current flows through this resistance, now output is low. So basically if you write Y here, it is equal to A, we have not achieved anything as such. Now suppose this also has a multi emitter transistor and I put another input here B then what happens? What is the logic there? Y is high; the output is high when none of this emitters are conducting.

There is no current flowing through this resistance, if none of the emitters are conducting. So it must be that A must be high and B must be also high then only none of the emitters are conducting and current flowing is zero. so this is Y = A B, A and B must be high, if one of them is high then the current can flow through the other emitter and then if the current flows through an emitter there is a going to be a collector current and the output is going to be low . So Y is high only when A and B is high. So you can have other input also, you can make AND gates but anyway that is not very important. The important configuration is something like this you have two inputs like this. Then suppose I have structure like this, it's a current source V_{EE}, here again there is a level shifting done here. So this is VR, from here you have a diode drop to here and say let me call this A one, let me call this A two and this is called capital A. What is the output which is what is important in this circuit? So when is Y high? Again Y is going to be high when both the emitters are not conducting.

When emitter one and emitter two is not conducting, only in that case the collector current of this transistor is zero And there is no drop across this resistance and the output is going to be high. If you call this emitter one when is emitter one not conducting? When either a_1 is high or if a_1 is low you see, the current has to flow through this But if this transistor is off then also there cannot be a current flowing in this emitter. So you say that when a_1 is high or when A is low, when A is low then this transistor is off And for emitter two, a two is high or A is high. if A is high then current is flowing in this transistor and the other one is off, So this emitter 2 is not going to conduct. So I just I want to repeat, if say if we call this emitter one and emitter two; emitter one is not going to conduct if a_1 is high which means just switches of this emitter because that emitter is not going to get forward bias by sufficiently Or even if a one is low if A is low then there is no current flowing here, there is no path for the current to flow. so if either a one is high or A is low and for emitter two to be not conducting either a two must be high or A has to be high.

If A is high $T_{1.}$ will be on and $_{T2.}$ will be off so emitter two cannot conduct. So this one is the output logic output which we get. In fact this can also be written as, this is the same as a one into A plus $a_{2.}$ into A bar. So this is the logic function so we can write it in this way. What you get it you have one input here capital A Then you have two output here, this two OR gate and so this is A bar or a one and this is a two, A or $a_{2.}$ AND gate so this is one.

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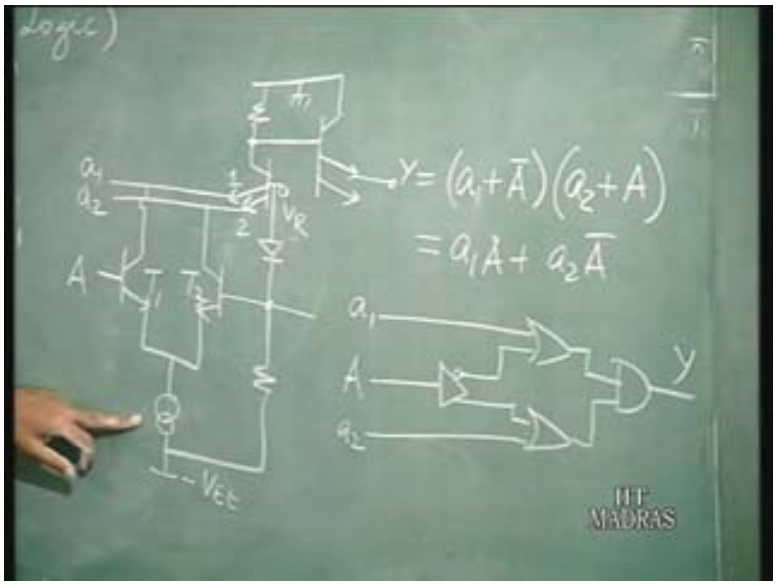

So this is what is achieved in this circuit and of course as you can very well see the power dissipation corresponds to that of a single gate because there is one current source. So this is the logic. Now of course you can make it even more complicated by just modifying the circuitry that is you have say you put this here. Then what happens, what is the change in this circuit here? Instead of an inverter this becomes a NOR gate, you have a NOR and OR. So the logic which we have is, this is the NOR gate. You have the two inputs A and B. I will draw it like this. You neither have one NOR output and one OR output and again you have the one and a two, F. The power consumption is the same as that of single OR NOR gate but you see that you have very complicated circuit here and so you have improved the functionality that is what is more important.

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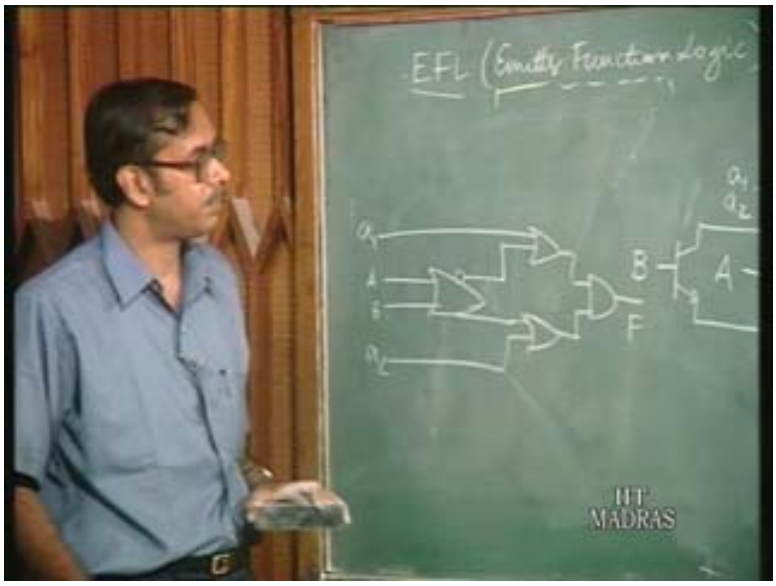

So this is the circuit. Now well you can make lots of other things like gates. Now suppose you want to make let us takes some example. Suppose you want to make an exclusive OR gate, how do you do it? We can come back here. Now if we make this a one which will go back here, If a one is equal to B and a two is equal to B bar, in fact what you get is an exclusive NOR gate That is you get a B plus A bar B bar that is an exclusive NOR gate and if a one is B bar and a two is B, you get an exclusive OR gate.

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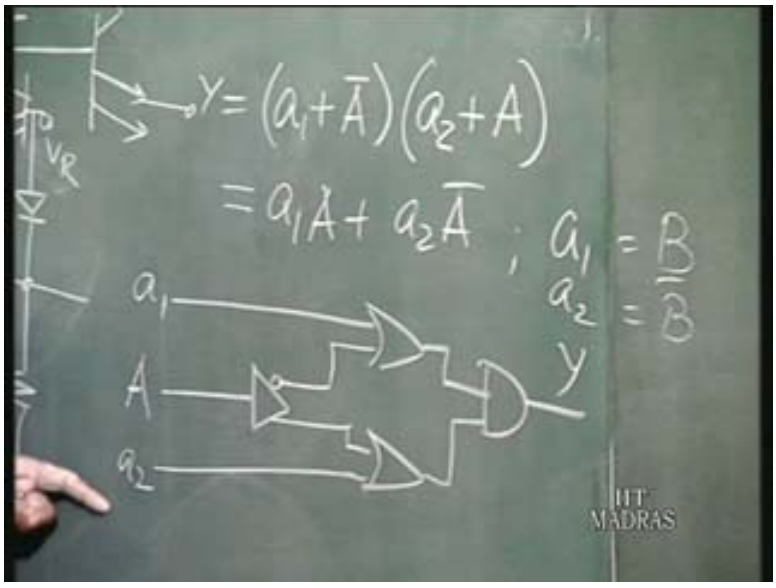

So by changing the inputs you can get different types of gates also in this case. Now you can also have D flip flop. This is the original function which you have, if you look at this function. I think we shall take it up in the next class that is we shall see the more complicated circuitry, the D flip flop for example how do you realize using EFL and we shall also see one

thing which we have left out that is the voltage requirements that is we have removed the emitter followers. So whether the circuit will actually work because the voltage levels are different. So what is the voltage levels required to make the circuit work? so these are the things we shall see but of course we can see that the functionality is improved tremendously in this circuit that is you can make a lot of complicated circuitry using the same power consumption as in a single gate and that is why this is called emitter function logic AND it's a important variation of the ECL gate for low power dissipation.