Digital Integrated Circuits
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Lecture – 19
Quantitative analysis of ECL 10k series gates

Last class we started our discussion on ECL gates and we have seen how the circuit functions. So we shall carry on with the discussion. So today's class what we shall do is we shall take up the circuit of commercially available ECL gate. So I have it on the black board here. So this is the circuit diagram of commercially available ECL gate, this is the ECL 10 k series and we shall analyze this circuit and we shall see how the input output characteristics are, for this particular circuit.

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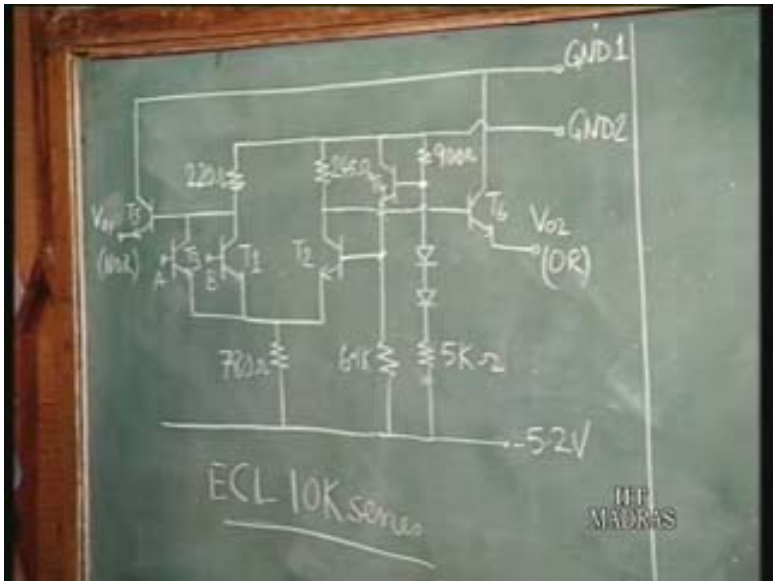

So let us just look at the circuit and see how does it compared with the circuit which we have already discussed. This circuit as you see here, this part of the circuit, this is the emitter coupled configuration. You have the transistors $T_{2.}$ on one side and at the base of that you have the reference voltage. So this is basically $V_{R.}$, the voltage here is the reference voltage and this $T_{1.}$ and $T_{3.}$ are the transistors for the inputs, where the inputs are applied and from the collector of these transistors you are supposed to have the emitter followers. So you have the emitter follower transistors, I just missed out something here (Refer Slide Time: 02:53). We have some resistances here at the inputs. So these resistances are 50 kilo ohms. So the collector of these transistors, these are the emitter follower's transistors. Here it's $T_{5.}$ this side and $T_{6.}$ on the other side. You see that the resistances are missing, the output is taken at the emitter but the resistance is missing here. Now if you are taking this output directly you can externally connect a resistance of whatever value you want to choose because also that contributes to the

delay also, what is the value but if you are feeding this output to the input of another ECL gate, what you have here is at the input A you have a resistance.
So this particular resistance would act as the resistance for this emitter follower. So this particular, if you are feeding output of similar gate to the input of this gate here, you have this transistor the emitter of which will come here, so this resistance acts as the emitter follower. Why you have a resistance here at the input? One reason is that if you have a resistance, the base is basically connected to the lower potential here. So if any input is left floating, it will be basically a low voltage. It will be a logic 0 at the input. You are basically not leaving the input floating which can give raise to lot of problems. If you are not connecting an input here, the logic at that particular input is going to be a logic 0 because that is basically connected to the lower potential through a resistance and if you are having a OR or NOR logic, you know that if any input is logic 0, it actually does not contribute to the output. The output is going to be governed by the other inputs. If you have a three input NOR gate or OR gate, if one logic is zero then the output depends on the other two inputs, zero does not contribute. On the other hand whereas in a NAND or AND configuration, if you have any input as one, the output does not depend on that input but it depends on the other inputs.

Any zero is going to force the output to one in a NAND whereas in a NOR, any one is going to force the output to zero. So that is why you have a resistance at the input which is basically means that any input which is not used, unused input has a logic zero. This part of the circuit which I am marking out here, this part of the circuit is for generating the reference voltage. You don't have a separate voltage input for reference voltage but this is generated internally in the chip from the power supply. So this part of the circuit generates the reference voltage. So we shall discuss that. The other interesting thing about the circuit is that you have two ground connections. Normally you have the two terminals for the power supply but here you have two ground connections. The reason for that is like this that if you look at this part of the circuit for example this $T_{1.}$ and $T_{2.}$, what is happening is when the input changes, the current may switch between from one branch to the other but the total current remains more or less fixed.

It is just the total current which is being switched from one branch to the other and also of course for this reference voltage generation circuit, the current is almost fixed. So if you look at the circuit connected to this ground, ground two in this case, this one, the current flowing is almost fixed. Whereas here ground one is actually connected to the external transistors $T_{5.}$ and $T_{6.}$ which is connected to the output and output you may have for example large capacitive loads and so what happens is when the output voltage switches from one state to the other and you know in an ECL gate, it is supposed to be a very fast logic. So DVDT or the rate of change of a voltage is going to be very fast. So you are liable to have large currents spikes across this transistor which is going through this transistor and again which may give raise to variations in the power supply, as we have already discussed.

So this ground one is sort of considered to be the noisy ground and ground two is considered to be the clean ground. So basically what is done is the two grounds are separated. So that the effect of any variations in power supply voltage is not felt in this part of the circuit which is actually carrying out the logic. So you have 2 separate grounds and they may be connected

finally at the system level but at this stage we are separated out and to protect this part of the circuit from any noise as such which may give raise to clichés in the logic. So that is the other thing, ground 1 and ground 2.

So with this background we can start our analysis of this circuit and see how the input output voltage characteristics looks like. So first let us see what is the value of V_R, what is the reference voltage? That is what we must find out. V_R or the reference voltage in this circuit is the base voltage of T four minus the V_{BE} of T_4. V_{BE} of T_4 or any on transistor here let us call it V_{on} and so V_{B4} - V_{on}. V_{on} is the base emitter drop of a transistor when it is in the on state. This let us say Von is 0.75 volts in this case. So we have to find out V_{B4}, what is the value of V_{B4}? It is very easy to calculate. The total drop across the power supply is 5.2 volts out of which 1.5 volt is dropped across the diodes, the remaining voltage is dropped across the two resistances and the constant current flowing through that. So you can find out the current, once you find out the current you can find out the drop across this nine hundred ohms and this is ground so minus of that.

So V_{B4} is equal to 5.2 minus 1.5 is the drop across the two resistances divided by the sum of the two resistances is five K plus 0.9 k. so this gives the current in milli amperes and the drop across the 0.9 k is going to be this. This is the drop across that resistance, minus of that is the voltage at the V_{B4}. So this if you calculate it gives minus 0.57 volts. So V_R equal to minus 0.57 minus 0.75 equal to minus 1.32 volts. So that is the value of V_R. Now that is once you have calculated we can go ahead.

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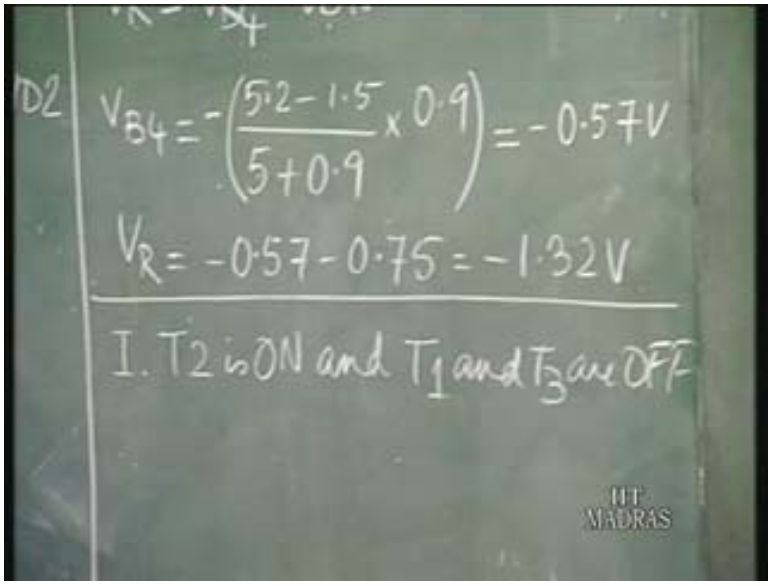

Now we shall look at the two different states that is one is when the left branch is conducting and the other is when the right hand branch is conducting and the other is when the right hand branch is conducting. So let us say case one, T_2 is on and T_1 and T_3 are off that is the right

hand branch is conducting. $T_{1.}$ and $T_{3.}$ off means that the input voltages at the base of $T_{1.}$ and $T_{3.}$ are much less compare to $V_{R.}$, we have already seen in fact a very small difference in voltage is sufficient to transfer the entire current to the right hand side branch. So if it is less than $V_{R.}$ by even low as 75 milli volts, very little current could flow in the left hand branch and most of the current would flow in the right hand branch.
So what is the value at this point? This is we call it $V_{E.}$ that is the emitter voltage, that is the common emitter point of these transistors. When this is conducting $V_{EE.}$ is equal to $V_{R.}$ - Von. So that gives us minus 1.32 – 0.75 is equal to minus 2.07 volts. $I_{E.}$ that is the total emitter current which is the different between these two voltages divided by R, the power supply voltage is 5.2 volts. So you have 5.2 – 2.07 divided by 780 ohms and it works out to 4.02 mili amperes according to my calculations, almost 4 milli amperes. So this is the emitter current which flows here. So these two transistors are not conducting. Now if you assume that this is the collector current, so the beta is high the collector current of that transistor is equal to the emitter current. so the collector voltage $V_{C2.}$ that is the collector voltage of transistor $T_{2.}$, $V_{C2.}$ is equal to minus $I_{E.}$ $R_{2.}$, if I call this $R_{2.}$, this is $R_{1.}$ say, this is $R_{2.}$ which is 245 ohms. So if you do this calculations 4.02 milli ampere into 245 ohms so this gives minus 0.99 volts. So the same current is flowing through this. So the voltage at this collector point is this and now just for the sake of checking you know, this is the collector voltage and what is the emitter voltage? minus 2.07.

So what is $V_{CE.}$ of this transistor $T_{2.}$? So $V_{CE2.}$ is 2.07- 0.99 so its 1.08 volts. So which means that this transistor is in the active region. It is not in saturation that is it ensures that. Now we know $V_{C2.}$.

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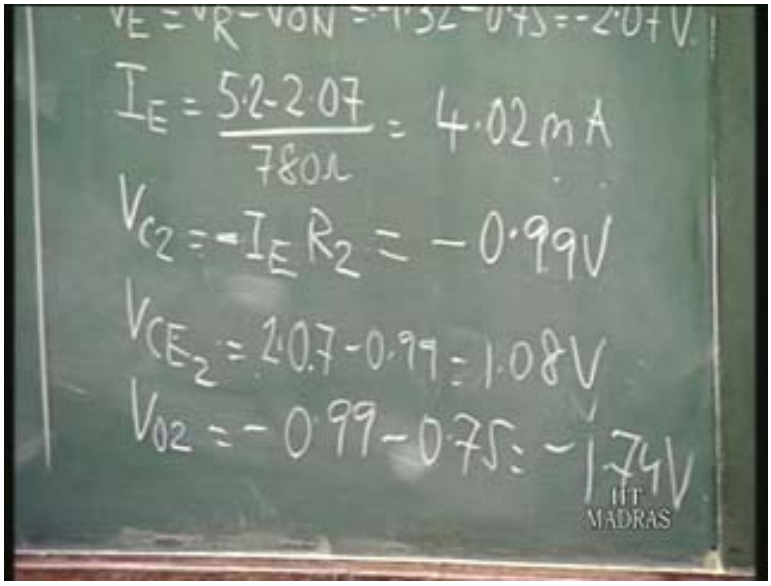

So what is V output? $V_{O2.}$ minus 0.99 minus 0.75 is equal to minus 1.74 volts. So that is the output when in this condition. That is $T_{2.}$ is on and $T_{1.}$ and $T_{3.}$ off and what is the output at

V_{o1}? V_{o1} is the output here, now this output is going to be; so there is no current flowing normally. That is basically I_{c1} is zero, there may be a current flowing which is the base current of T_5. So that is going to be the current, the emitter current of T_5 divided by beta times, beta plus one times. So basically it is going to be zero minus R_1 times the load current divided by beta. So that depends on the load current. This 0.75 is the base emitter drop of this transistor T_5, so 0.75 minus; so let us assume this is minus 0.9 volts. It is just an assumption that the value of I_L is such that this is 1.5 volts and you have V_{O1} is minus 0.9 volts.
In fact this has been designed assuming this in which case what you have is V_{O1} + V_{O2} by 2 is equal to; what is V_{O1}? minus 0.9 and V_{O2} is minus 1.74 by 2.

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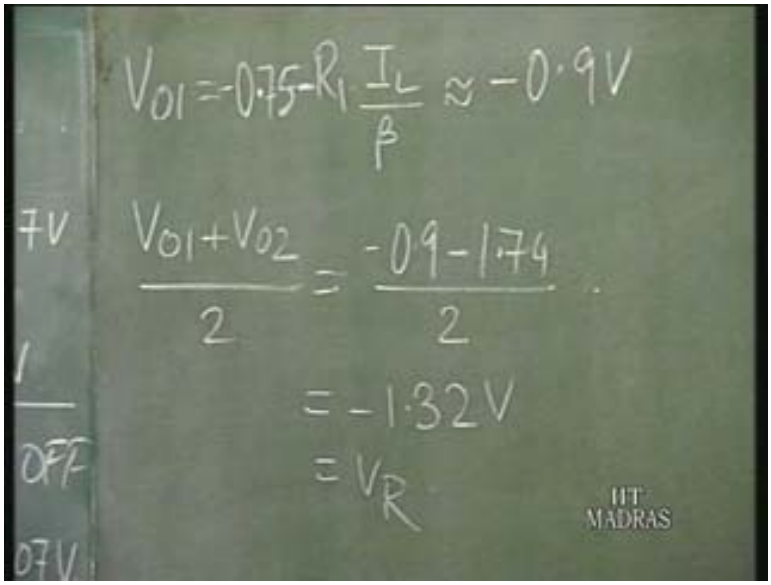

What is this equal to? (Refer Slide Time: 20:30) minus 1.32 volts which is equal to VR. That is the output voltage swing is symmetric about the reference voltage that is the output voltage of this ECL gate is also going to be the input voltage because the output is going to be fed in as input to the other gates. So the input voltage swing is symmetric about the reference voltage that is what is important here. So you get this voltage variations. So this is about the case where T_2 is on and T_1 and T_3 is off.

Now let us take the other case that is T_2 is off and T_1 or T_3 is on. What is going to happen? That is case two, T_2 is off and T_1 or T_3 is on. That is the base voltage for transistors T_1 or T_3 is greater than the reference voltage which would mean that either T_1 or T_3 is on, whereas T_2 is off. So if you have this condition I_{E1} say T_1 is on, so I_{E1} will be equal to; the T_1 is on means that the input voltage at the base of T_1 is equal to the input corresponding to logic high and you have seen that the voltage corresponding to logic high is minus 0.9 volts. So let us assume that the input voltage is minus 0.9 volts .so the voltage levels here, the logic levels are minus 0.9 and minus 1.74 volts, minus 0.9 is logic high, minus 1.74 is logic low. So if you assume that it is minus 0.9 volts so what is the current flowing? What is the V_E in this case? The emitter

voltage in this case, if this is minus 0.9 volts, the V_E is going to be minus 0.9 minus 0.75. So this is minus 5.2, so the current flowing is going to be 5.2 minus the sum of minus 0.9 and 0.9 and 0.75.

So divided by the resistance so you have 5.2 minus 0.9 plus 0.75 divided by 0.78 kilo ohms. So this comes in milli amperes which is 4.56 milli amperes. So that is the current which is flowing. Now what is the output voltage, what is the collector voltage going to be? V_{C1} is going to be 4.56 into 220 ohms.
So this gives 0.22 basically, so this is milli amperes, this is kilo ohms, so this is going to be one volts.

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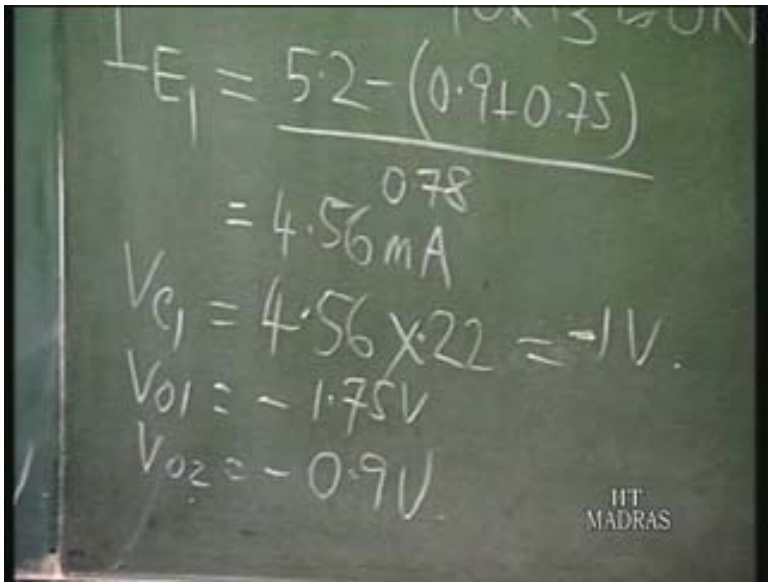

So V_{C1} is minus 1 volt, so this is the drop across the resistance, so V_{C1} is minus 1 volt and V_{O1} is minus 1.75 almost the same as previous case and V_{O2} similarly is going to be minus 0.9 volts because in this case again that is no current flowing in the other branch here. So this drop is zero, again the output is going to be this drop and again depending on the load current you get the output. So we assume that this is the voltage. So basically you see that both cases this is true. So the output voltages vary from minus 0.9 to around minus 1.75 volts. Now can we draw the input output characteristics based on this?

So this is the input scale say. I draw this, this is V_R is equal to minus 1.32 volts and then what happens? So suppose we are plotting the OR output. Now for the OR output when the input is

low, output is also low. So when the input is low, the output should also be low then it goes high. Now so when the input is low what is the output voltage? That is the equal to logic low minus 1.74 volts. So this is going to be minus 1.74 volts, this is minus 1.74 volts. So this goes like this then up to what value does it go like that? The logic changes, we have already seen that the current is going to switch from one state to the other or from one branch to the other, when the input voltage is about 75 milli volts from the reference voltage.

So when it is very close to this, then its starts changing like this, it just switches to the other level. So what is this value here? It is around minus 0.9 volts, so this is OR. So it goes from minus 1.74 to minus 0.9 volts. What about the NOR? So basically in the case of NOR output, again when the input is low, the output is going to be high. So here the output is going to be high. What is the value here we have seen? Again minus 0.9 volts and then goes like this but there is a small difference here between the two. This you can see when you go back to the circuit. See when the input voltage goes high here, what is happening? This particular transistor is off, T_2 is off, say T_1 is on. Then what happens is this circuit behaves as an amplifier, you have a collector resistance R_1 220 ohms and you have a emitter resistance 780 ohms and if you go on increasing the input voltage, what is going to happen?

What happens is if you go on increasing the input voltage, what happens to this V_E? It also keeps on increasing. So what happens to the current? Current also increases, emitter current keeps on increasing because V_E increases so the drop across the emitter resistance increase which means the emitter current keeps increasing which also means that the collector current is also increasing because collector current is the same as the emitter current. So what happens to the collector voltage? Collector voltage decreases because the drop across this collector resistance increases. So as you go on increasing the input voltage, the emitter voltage increases whereas the collector voltage decreases. So what happens to V_{CE}? The V_{CE} goes on reducing and ultimately the transistor will go to saturation when this V_C becomes about 0.2 volts. So in this case the transistor is actually going to go to saturation, if you go on increasing the input voltage because V_{CE} keeps on reducing. This is just like a common emitter amplifier with emitter resistance. So what is the value of the input voltage, when this transistor goes to saturation? Say when V_{CE1} is equal to 0.2 volts, I_C is equal to I_E. What is the value? The total voltage across the power supply is 5.2 volts, 0.2 volts is the drop across the transistor, the remaining five volts is dropped across the two resistances and the current flowing through the two resistances is the same, I_C is equal to I_E. So 5 volts divided by the sum of these two resistances is the current.

What is the sum of these two resistances? 780 ohms plus 220 ohms, 1 kilo ohm. So I_C is equal to I_E is equal to 5 volts by 1 kilo ohm which means 5 milli amperes. So what is V_E equal to? V_E is equal to 5 into 780 ohms, I think we, put 0.78 because this is in kilo milli amperes this is in kilo ohms, minus 5.2 volts that is the reference plus this drop. So that is V_E. So what is

this? This is 3.9 I think, minus 5.2 minus 1.3 volts. Am I correct? Now $V_{E.}$ is minus 1.3 volts, so $V_{in.}$ is minus 1.3 plus 0.75 so that is equal to minus 0.5 volt. So when $V_{in.}$ goes to minus 0.5 volts, the transistor actually goes to saturation and once it goes to saturation, what happens is if you go on increasing the input voltage, the $V_{CE.}$ remains fixed. It is not changing any more. So if you go on increasing this, the emitter voltage goes up because the drop across this is 0.75 which means that the collector voltage also is going to go up. So basically the characteristics which you have now is going to be something like this for the NOR output, it behaves like this, goes up like this. So this is minus 0.5 volts.

We have already seen that when the input voltage is minus 0.9 volts, for this the output voltage is minus 1.74 volts. So when this is minus 0.9, this is minus 1.74 volts. So this point we have already seen, calculated. So it goes through this point, goes down to minus 0.5 and then it goes up. So this is the NOR output. So the point is as we see the transistor actually goes to saturation, if the input voltage is very large but the point is the input voltage has to be restricted, voltage rain has to be restricted.

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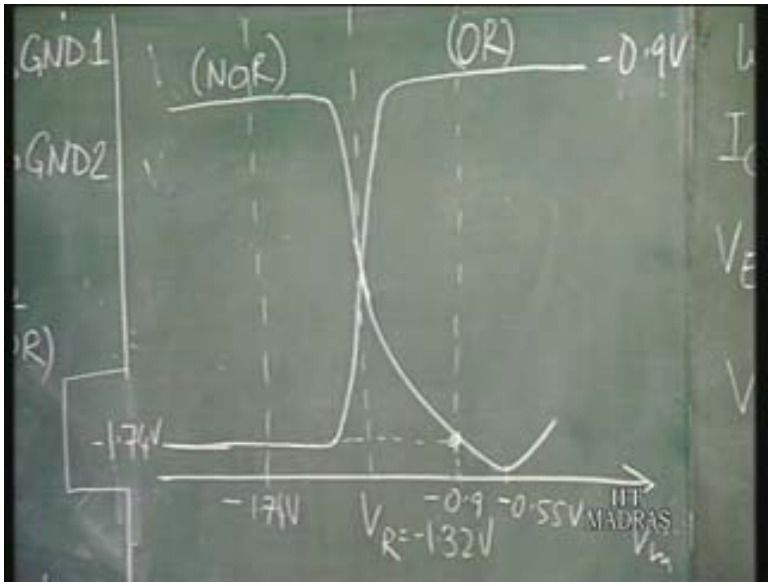

That is the input voltage range which we must have must be restricted to minus 1.74 volts on one side and minus 0.9 on the other. So if the input voltage range is restricted within this limit then we will be sure that the transistors are going to go to saturation. So that is another condition which we have already seen last class that we have to restrict the input like we have said, $V_{R.}$ plus minus half $V_{on.}$. So similarly here also we have to restrict the input voltage within a certain limit that is we have assumed here that the input voltage range is the same as the

output voltage range and if this is there then the transistors are not going to go to saturation, so they remain within this limits.

Now for this circuit what is the noise margin? Let us take it up as the next thing. From the input output characteristics, you can calculate the noise margin. The noise margin low is V_{IL} minus V_{OL}. So what is the input low in this case? So it is with respect to V_R, so basically if the input voltage is up to here, it is going to be considered the logic low beyond that it is no longer a logic low. So this is V_R this is the reference voltage, so what is the difference in voltage? Usually it is 0.75 as we had seen from a calculation but for worst case because of the other drops in the base emitter, serious resistance drops, this is usually taken to be 0.1 volts for the worst case. So if this is 0.1 volts that means this is minus 1.22.

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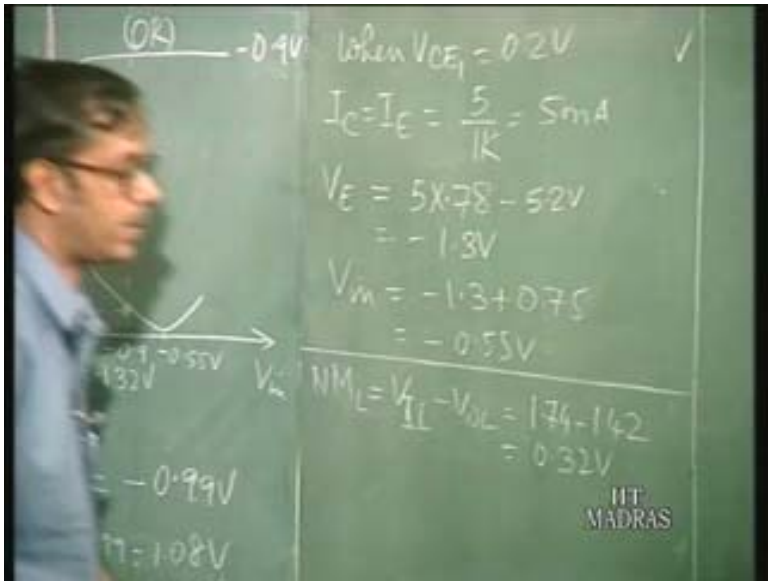

The other extreme is minus 1.42 on the other side. V output low is minus 1.74, this is minus 1.42 that other side would be minus 1.2. So this is going to be 1.74 minus 1.42 so this is 0.32 and noise margin high is equal to V_{OH} minus V_{IH} so which is equal to minus the difference of 1.22 and 0.9, this is again 0.32 volts. So basically you have equal noise margins, low and high. So 100 milli volts above V reference would be considered a logic high, that particular branch would start conducting, if the input voltage is greater than V_R by hundred milli volts.

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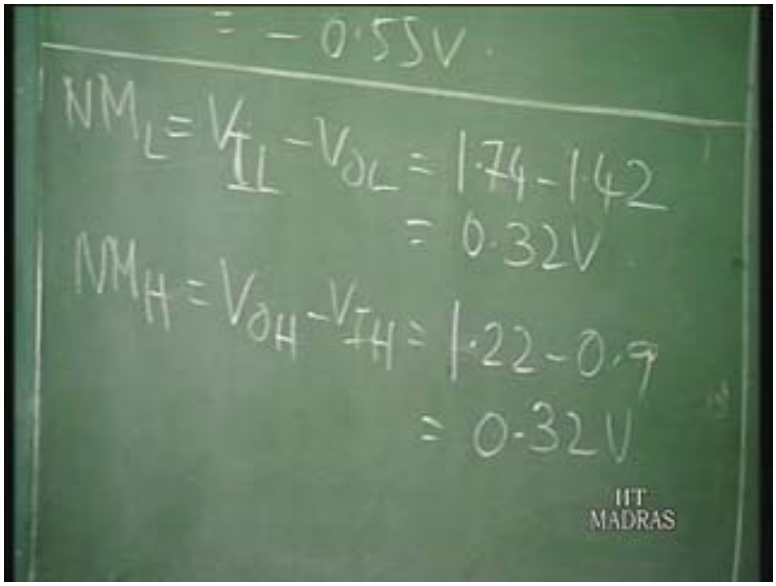

So that is minus 1.22 and the logic high output is 0.9 volts minus 0.9 volts. So the noise margins are symmetric in this case for 0.32 volts. So we have made the calculations of noise margin from here. Then the next thing which we shall take up from the circuit is power dissipation.

Power Dissipation:
We have seen that in the two states that is one state when left branch is conducting and the other state when the right hand branch is conducting. the values of the currents IE in one case current was 4.02 milli amperes and the other case it was 4.56 milli amperes. So we can take the average of the two currents, IE average of these two and that is equal to 4.29 and power consumption will be equal to this current 4.29 milli amperes into 5.2 in milli watts.

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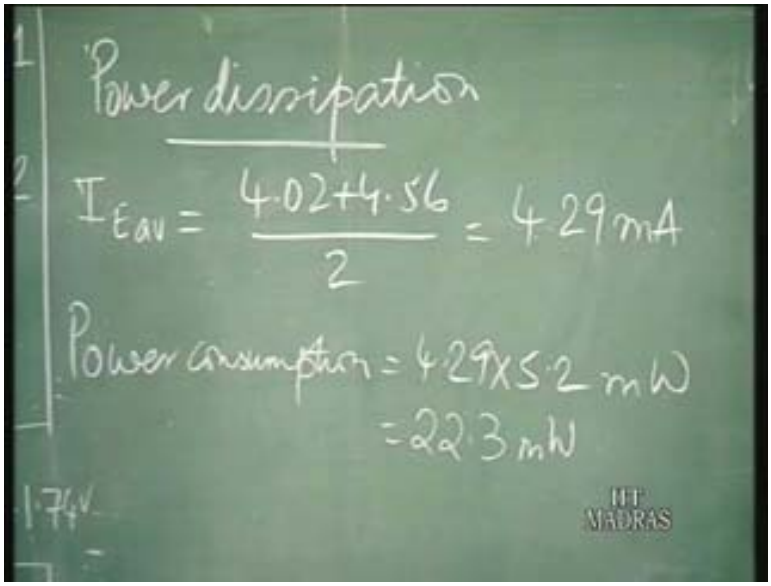

This works out to 22.3 milli watts. For the reference voltage generation circuit what is the current through T_4? I should say I_E. T_4 say the reference voltage divided by 6.1 K is going to be that current. That is the current which is flowing through this branch. So that is the difference, reference voltage and the supply so 5.2 minus 1.32 that is the drop across the resistance divided by 6.1 K that is equal to 0.64 milli amperes and bias that is the other part this one. One can easily calculate, if you know the voltage this is ground, so this is the drop across 900 ohms divided by nine hundred ohms gives the current. So we have already seen that the base of T_4, the voltage is minus 0.57 volts. So 0.57 divided by 0.9 K so this is 0.63 milli amperes. So the power consumption is 5.2 volts into 0.64 plus 0.63 is equal to 6.6 milli watt, I just mean this calculation.

Now in this circuit, this OR NOR gate is available as a quad or NOR gate in a chip. That means that in a chip you have 4 such OR NOR gates and this part of the circuit, the reference voltage generation circuit is common to the 4 gates. You don't have the 4 different reference voltage generation circuits, you have a common reference voltage circuit for the 4 gates. So now how do you calculate the power dissipation per gate? So the power dissipation first is going to be 22.3 milli watt plus 6.6 divided by four because the 6.6 milli watt you shared in the 4 gates.
So this works out to 24 milli watt per gate and so this is the power dissipation per gate which is rather high which you can see that is one of the problems of ECL gate, the power dissipation is rather high because the transistors have to be operated in the active region which means that you cannot restrict the current. I mean so you have a large current flowing so that is why the power dissipations are rather high. So you have 24 milli watts per gate. In fact for this particular circuit the delay is 2 nano seconds per gate which makes a power delay product of 48 peco Joules.

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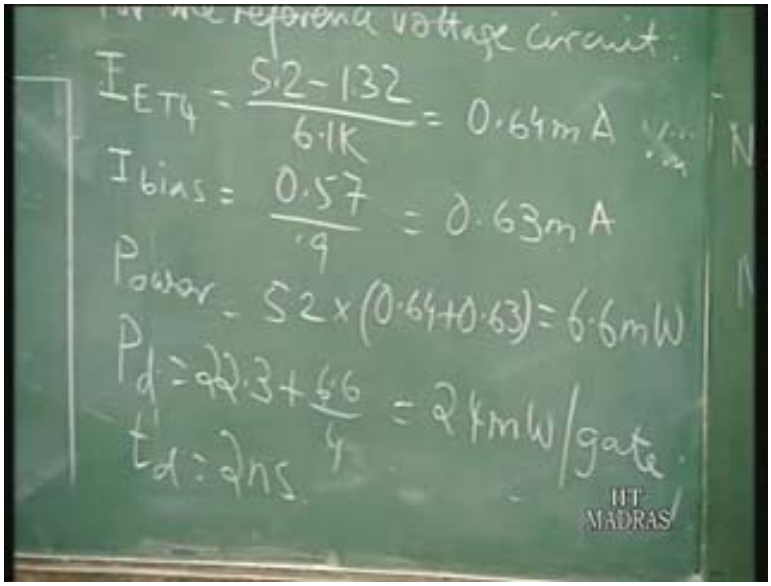

So for this gate the delay is 2 nano seconds, so the power delay product is forty eight peco joules. Of course one must remember that this is the first generation of ECL gates. So you should not compare with the second generation of TTL gates, advanced short key TTL is faster but you should not do comparison, unfair comparison because this is actually the first generation. We will come to that next generation characteristics which is superior to advanced short key TTL. So this is the characteristics of this particular gate. Just before I close today, I just have one small question. This if you look at the reference circuit it is a peculiar, we have 2 diodes here. Why do you have two diodes there, what is the purpose of having two diodes? No it is not really level shifting, it is basically for temperature compensation. See you know that the basic emitter voltage of a transistor changes, it's around 2 milli volts per degree centigrade and when you convert that to current because of the exponential nature, you know you have a lot of difference. So what happens is when the temperature goes up, you see the voltage across these diodes also changes. So from this point if you see a two diodes here and these are the two base emitter voltage is here so presents of these diodes actually compensates for any change in the voltage is across the base emitter of these transistors. So you do not have any problems as such. So this diodes are used for temperature compensation. So otherwise you could have had a simple potential divider type of network.

So I think we shall stop here today. What we have seen today is we have analyzed this particular circuit which is the 10 k series, you have looked at the input output characteristics of an ECL gate, as well as the noise margins and the power dissipation. Of course the problem is power dissipation which is quite large. In the next class what we shall take up is the next series of ECL gates and we shall also see efforts being made to improve the characteristics further.