Digital Integrated Circuits
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Lecture – 18
ECL Basic Operation

Today we shall begin our discussion on another logic family that is the ECL or the Emitter Couple Logic which is the fastest of all the logic families and therefore has an important place in the family of logics. So you have the Emitter Coupled Logic (ECL). This is also sometimes denoted by another name called Current Mode Logic or CML. So the basic structure of the emitter couple logic is like this. It is similar to the differential amplifier configuration in analog circuits. So you have a current source here and you have two transistors here, you can have more than them. Here this side grounded is the typical configuration. We shall come to that why the circuit actually operates from a negative power supply. So here you have a negative power supply and this is grounded here.

So here you have a constant voltage at the base of this transistor and these are the inputs, say input A and B. So this is the configuration of the ECL. Now it is very clear about why it is called the emitter coupled logic because as you can see the emitters of all the transistors here are coupled together and the inputs here are the basics of these transistors and for this branch, the input is a fixed voltage called the Reference Voltage or V_R. How does this logic work?

So the output of the logic can be taken from the collectors of either of this group of transistors here or from the group of transistors there. So let me call this Y_1, let me call this Y_2. You have a constant current source here I_0, so the total emitter current is constant I_0 and what happens now is if A and B, the input voltages are much less compared to V_R. Of course one must remember here that we are operating with negative power supply voltages, so this is minus V_{EE} and this is ground, so all the voltages in the circuit are negative but it is a positive logic in the sense that if we will call it logic high, if the voltage is closer to ground, I mean the more negative voltage is the logic low and the less negative voltage is a logic high.

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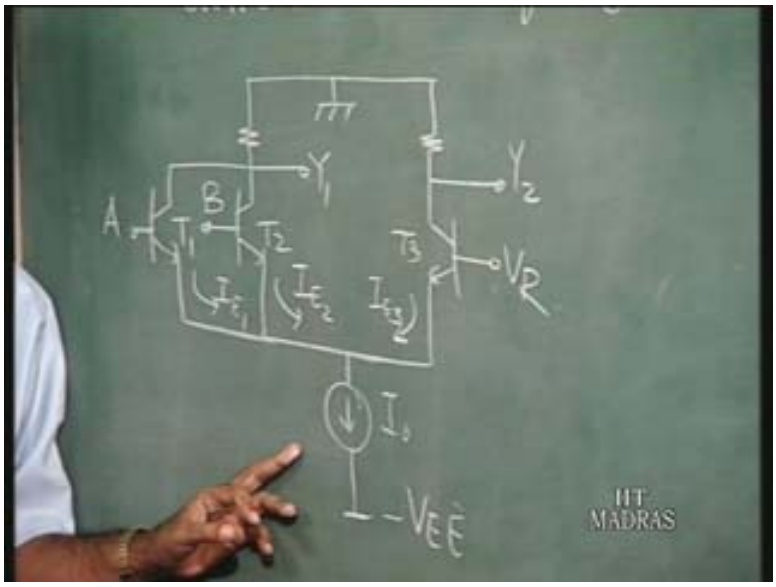

So in fact it is quite similar, if you have the ground here and a plus V_{cc} here, everything else is similar but there is a definite reason for operating the negative power supply voltages which I shall discuss later on. So when this input is less compared to V_R which means that when this input is more negative than V_R then we can say that the base emitter voltage of this transistor is much less than this one. So I will give the names I think T_1, T_2 and T_3. So if V_B that is at the input B is less than V_R, the base emitter drop of transistor T_2 is going to be less than the base emitter voltage of transistor T_3 because the emitter point is common. So if the base voltage is less obviously base emitter voltage is less.

Similarly if V_A is less than V_R, the base emitter voltage of transistor T_1 is less than the base emitter voltage of transistor T_3. So if the base emitter voltage of this and they are usually identical transistors, so if the base emitter voltage is less, it is quite natural that this is going to draw less current and the transistor with higher base emitter voltage is going to draw more current. So if V_A and V_B are both less than V_R, the majority of this current I_0 so let me call this I_{E2} and this is I_{E3} so this is I_{E1} so I_{E1} plus I_{E2} plus I_{E3} will be equal to I_0 in this circuit.

Sum of all the emitter currents is equal to the total current. Now if I_{E1} and I_{E2} are very much less than I_{E3} then the entire current flows in this branch, the right hand side branch and there is very little current flowing in the left hand side branch. So let me call this R_1 and let me call this R_2, let me keep it a constant resistance R in both the cases.

Since I_{E3} is much more than I_{E1} and I_{E2}, so the drop across this resistance in the right hand branch is going to be more compared to the drop in the left hand branch. So what is the voltage? Y_2, it is going to be more negative compared to Y_1. So Y_2 is logic low where Y_1 will

be logic high. So if both of them are low, both the inputs are low, $Y_{2.}$ is logic low and $Y_{1.}$ is logic high.
Now if any one of them goes high, say if B becomes higher than $V_{R.}$, it is going to draw more current and since the left hand side branch, the total current flowing through this resistance is $I_{E1.}$ and $I_{E2.}$, if the beta of the transistor is high, we can assume that the collector current is almost the same as the emitter current and so the left hand branch draws more current and so $Y_{1.}$ will be low and $Y_{2.}$ will be high.

So basically what is happening is by applying voltages, if you apply a high voltage of the input, you switch the current to the left hand side branch. If any of the input voltages go high compared to the reference voltage then the current is switched to the left hand side branch and the drop is less and the drop across this resistance is higher so that $Y_{1.}$ goes low whereas if both the inputs are low then the current is mostly in the right hand side branch and $Y_{2.}$ becomes low. So what is the logic at $Y_{1.}$? It is a NOR logic. Why it is a NOR logic? Because if any one input goes high there is a current flowing in this branch and this output is going to go low and when $Y_{1.}$ goes low, $Y_{2.}$ is high. So $Y_{1.}$ is an OR logic that is why any one of the input goes high the current is flowing in the left hand side branch and there is no current in the right hand side branch, $Y_{2.}$ is high. So $Y_{1.}$ is NOR of A and B and $Y_{2.}$ is OR of A and B.

The basic idea is, you are switching the current between either of the two branches and the total current is constant and if you apply an input voltage which is higher than the reference voltage, you have more current in the left hand side branch and the output voltage at here $Y_{1.}$ goes low and if both the inputs are lower compared to VR, $T_{3.}$ is conducting, $T_{2.}$ and $T_{1.}$ is not conducting, so $Y_{2.}$ is going to go low and $Y_{1.}$ is high.

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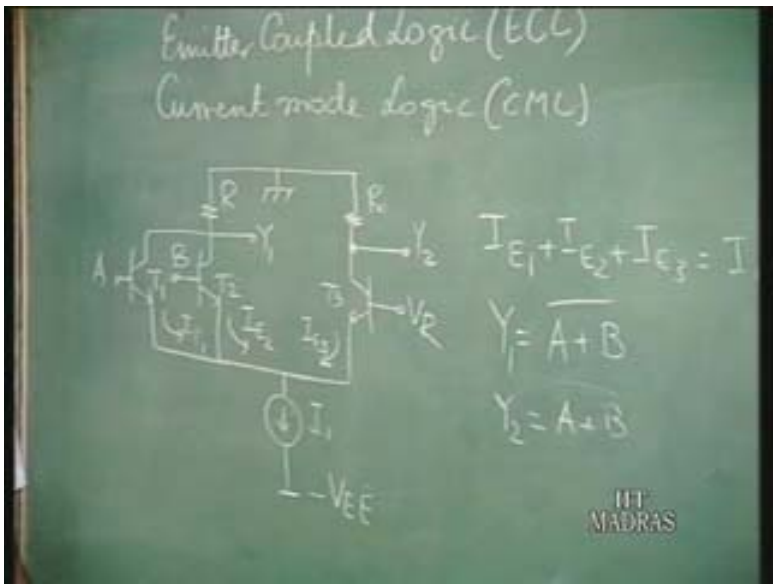

Now basically this is the operation of this ECL gate and you have these logics at the two outputs. Now just to give you an idea of how much input variation is required to switch the current from one branch to the other. Now just let us forget this say T_1 for the time being and say we have just one input here T_2 and we have the other voltage and you have T_2 and T_3..Now the input at the base of T_3 is VR and the voltage at the base of T_2 is VB.

Now if you again recall the Eber's Moll model which we had and just we assume that the transistor is in the active region that is the base collector voltage is negative, its reverse biased and also beta is large, we can write that I_E is almost equal to I_S exponential V_{BE} by V_t. So I_{E2} , that is transistor T_2, I_{E2} is equal to I_s exponential V_{BE} for that is V_B minus V_E if we call this emitter point voltage as V_E, the emitter point voltage here common emitter point voltage as V_E. .So V_B minus V_E by V_t for transistor T_3., I_{E3} is I_S same because as I said they are identical transistors, I_S exponential V_R minus V_E by V_t. This is the common emitter voltage so V_R minus V_E by V_t.

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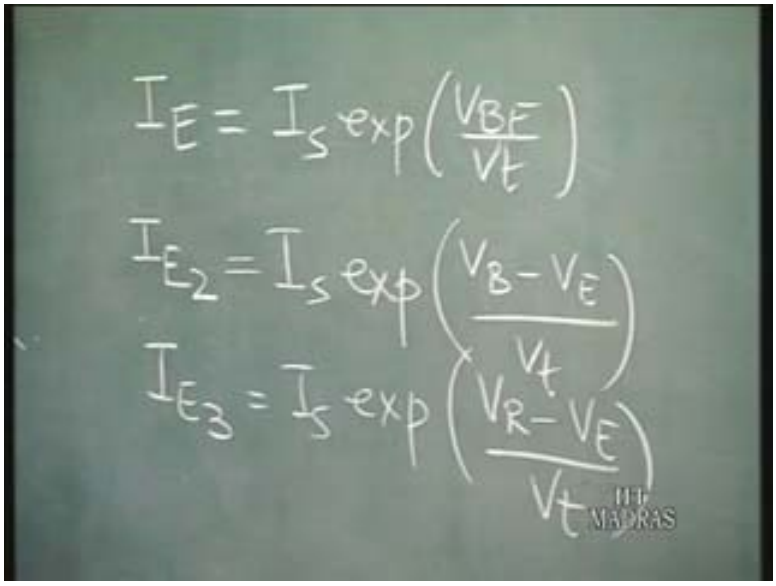

So I_{E2} by I_{E3} is equal to exponential V_B minus V_R by V_t. So next step we can write V_B is equal to V_R plus V_t in I_{E2}..

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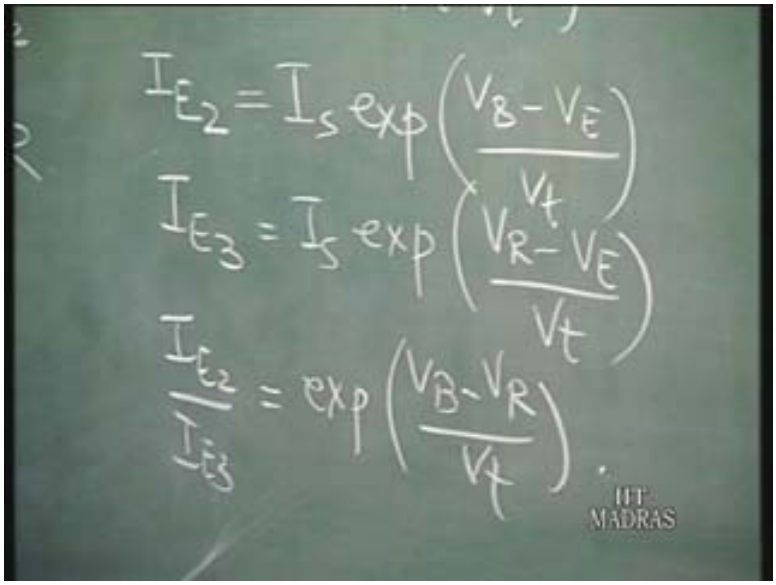

This is the relation governing the input voltage and the two emitter currents, V_B is the base voltage for transistor T_2 and V_R is actually the base voltage transistor T_3. Now this relation we can see very well that if I_{E2} say is equal to 95% of I_0 that is the total current, then what is this V_B equal to? V_B will be equal to V_R plus V_t ln, this is 95%, so I_{E3} is just 5%. So 95/5, so V_t ln 19.

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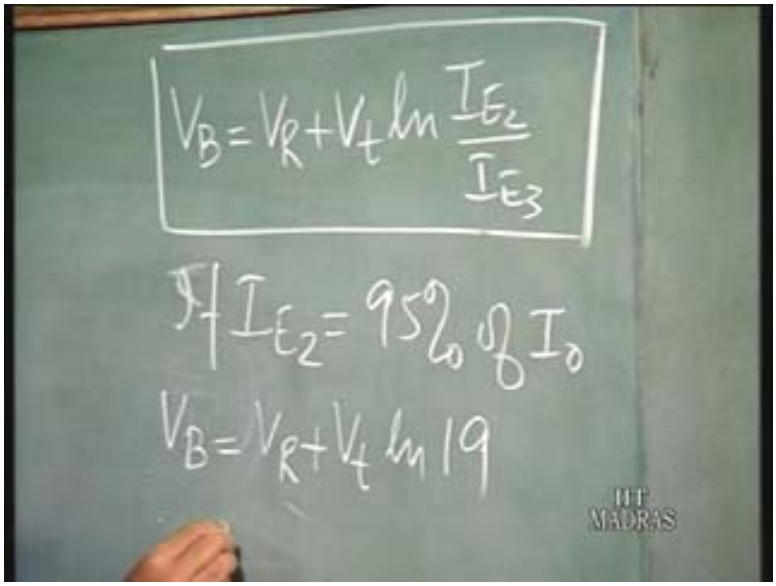

So ln 19 is around 3, so this one is going to be and this is around 25 milli volts. So this is V_R plus approximately 75 milli volts. So the point here is that, if the input voltage at the base of T_2 exceeds V_R by just 75 milli volts, then the 95% of the total current flows in transistor T_2. That means almost the entire current flows in transistor T_2. So we put 95% because you cannot put 100%, that's the problem any way.

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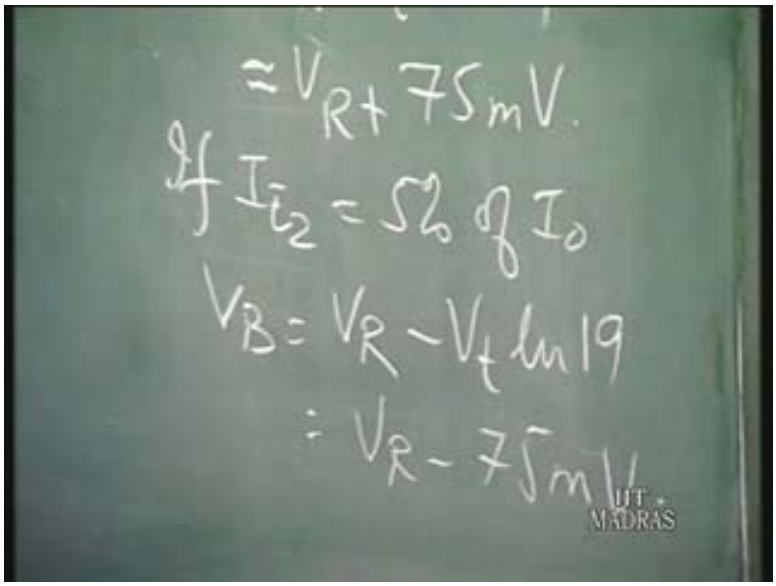

If I_{E2} is say 5% of I_0, V_B equals to V_R minus Vt ln 19, same thing 5/95. So V_R minus 75 milli volts. so you see that if V_B is less than V_R by just 25 milli volts, it's almost carrying no current. The entire current is flowing in the other branch whereas if you exceed V_R by 75 milli volts, you get the entire current closed in the branch. So you can switch the current, this

circuit from one branch to the other. Almost the entire current by changing the input voltage by just about 150 milli volts. So from V_R minus 75 milli volts, when the entire current flows in the right hand side branch, if you exceed it, make it V_R plus 75 milli volts the entire current flows in this branch. So you see the important thing here is you require just a very small voltage variation to change the state of the logic which is very important here because that gives us very high speed and that is direct result of the exponential, the dependence of current with voltage. For MOS circuits you would require a large voltage variation to change the logic. Here you require a very small voltage variation to change the logic and small voltage variation requires less time so you get high speed so all these things are related. So if I just plot it you know, if this is the reference voltage and I plot Vin or I call V_B and if this is say V_R minus 75 milli volts and this is V_R plus 75 milli volts. So here when it is V_R minus 75, see just the current is switching from one branch to the other. So when V_R minus 75 milli volts, so this is I_0 here so when it is V_R minus 75 milli volts, so I_{E2} is only 5% so this is I_{E3}, this is I_{E2} so you see that when V_R minus 75 milli volts, I_3 constitutes the entire current whereas I_2 is very small current.

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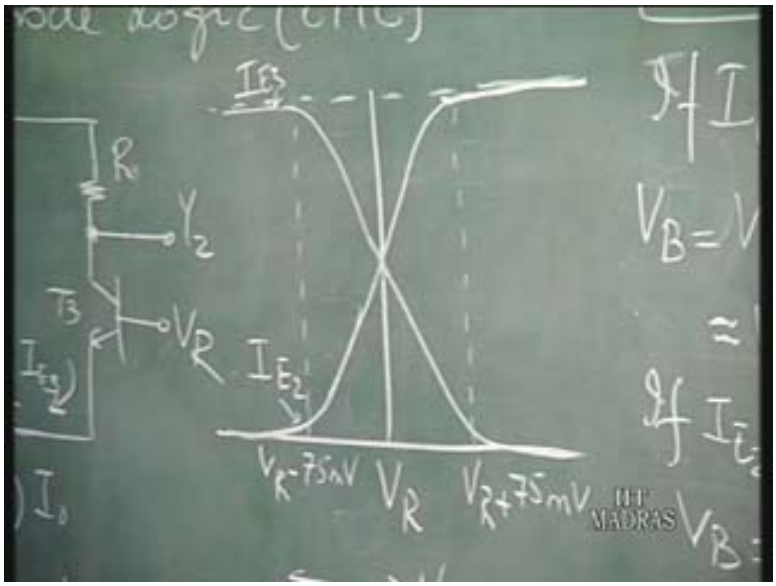

Of course when V_B is equal to V_R then both of them should carry the same current because they are identical, there is absolute symmetry and when V_B becomes V_R plus 75 milli volts, I_{E2} is going to carry almost the entire current, will I_3 goes to ((…)) carrying negligible current. So by small change in input voltage, you are able to switch the current from one branch to the other and when you switch the current from one branch to the other, the drop in these two

resistances the two branches changes. So when one was carrying the entire current, the output voltage here. When the left hand branch carries the entire current Y_1 could be low, Y_2 will be high. When the right hand side carries the entire current Y_2 will be low, Y_1 will be high.

So you are able to change the state and here you are having 2 transistors in parallel which means that if any of them is conducting, the left hand branch is going to carry the current. So you can have more than 2 I mean you can have 3 or 4 in parallel, you want a 3 input NOR gate you have 3 transistors in parallel, for a 4 input NOR gate you have 4 transistors in parallel. So this is how ECL works. So we have seen that how the circuit works. No problem but being a high speed circuit, it has to have certain important considerations, that is these transistors are supposed to work in the active region. They should not go to saturation because if they go to saturation then you have the delay related problems. So in fact these transistors switch between the cut off and the active region, they do not really go to saturation. Now how do you prevent the transistor from going to saturation? In this particular circuit the transistor is prevented from going to saturation by choosing the values of I_0, R and the input voltage appropriately. So if you choose these values appropriately, you can ensure that this transistor does not go to saturation. Now how do you do that? We shall take up that next. Suppose that we chose I_0 and R in such a way, I_0 is the current source and R is the collector resistance, that the product I_0 into R is equal to V_{on} where V_{on} is the base emitter voltage of a conducting transistor. When the transistor is conducting, the base emitter voltage is V_{on} that is around 0.7 volts some cases in ECL because these transistors are very small, this V_{on} maybe 0.8 volts also. So 0.7 to 0.8 volts.

Now let us chose I_0 and R in such a way that I_0 * R is V_{ON} that is we have chosen this. So if this is how you are chosen then we can say that the minimum voltage that we can have at the collector of a transistor is what minus V_{ON}. Because the maximum current that can flow through this resistance is I_0, in a branch is I_0 and so the maximum drop that you can have is I_0 * R. So you cannot have collector voltage which is less than minus I_0 * R. So if I_0 * R is V_{ON}, we can say that V_C min is equal to minus V_{ON} because I_0 * R is V_{ON}. So this is one thing we have seen. The next condition which we impose is that let V_I we call the input voltages is equal to V_R plus minus 1/2 V_{ON}.

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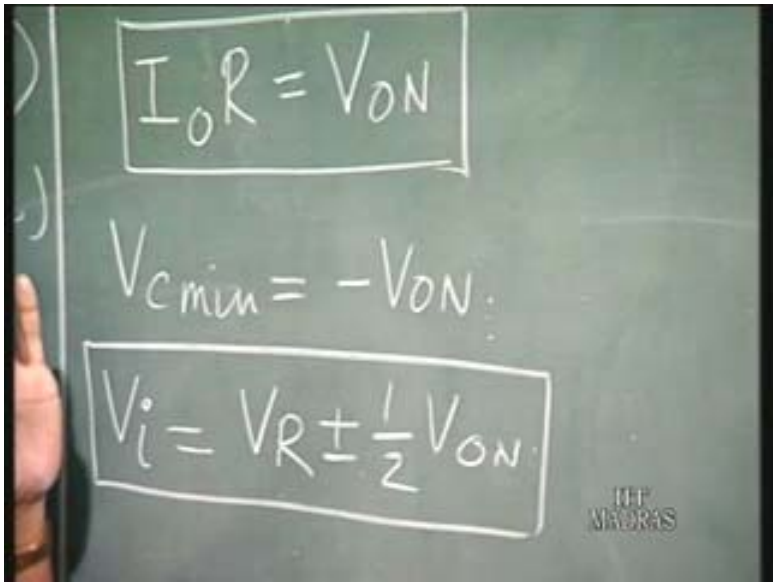

That is the input voltage variation, it is a range of V_{ON} about V_R that is the input voltage can vary from V_R minus 1/2 V_{ON} to V_R plus 1/2 V_{ON}. That is the input voltages at the inputs. They should vary within this range, we want to ensure that it should not exceed that variation. That is the total input variation will be one V_{ON} from minus 1/2 V_{ON} to V_R plus 1/2 V_{ON}. Now if we have this condition, what is V_E max? That is we have seen v_C min. Now what is V_E max? That is the maximum value voltage that we can have at V_E. That is going to occur when the input voltage is at its maximum. When this input voltage goes to the maximum that input voltage minus V_{ON} is going to be the maximum value you can have at the emitter point. So the maximum value you can have at the input is V_R plus 1/2 V_{ON}. So if this is V_R plus 1/2 V_{ON}, the drop across the base emitter drop is V_{ON}. So V_E maximum is going to be V_R minus V_{ON}. So V_R plus 1/2 V_{ON} minus V_{ON}, so this is V_R minus 1/2 V_{ON}. What is V_{CE} minimum? That is the minimum collector emitter drop which you can have is obviously V_C min minus V_E max. When the collector voltage is of the minimum, emitter voltage is of the maximum that is the minimum value of the collector to emitter drop which you can have. So this is V_C min minus V_E max.

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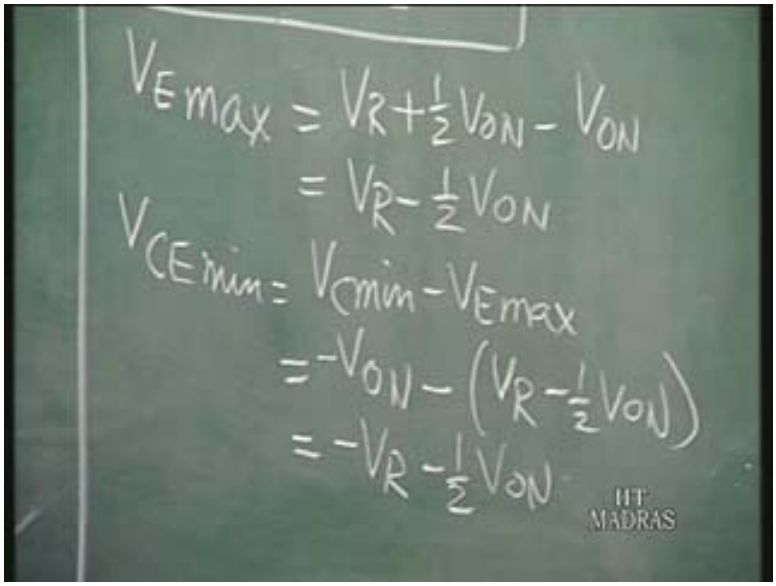

So what is this equal to? minus V_{ON} minus V_R minus 1/2 V_{ON}, So this is equal to minus V_R and plus 1/2 V_{ON} so minus 1/2 V_{ON}. So this is the V_{CE} min (Refer Slide Time: 29:28). Now we can prevent the transistor from going to saturation by limiting the value of V_C min. We know that when the transistor starts conducting more and more what is happening is the collector voltage is dropping and the V_{CE} is going to reduce. Now as the V_{CE} reduces, the transistor starts going to saturation, the collector base junction starts getting forward biased. So because base emitter you have say 0.7 volts, So when V_{CE} is 0.7 volts, collector base junction voltage is 0. If V_C falls below 0.7 volts it means that the base collector junction is getting forward bias. So we can prevent the transistor from going to saturation by limiting this V_{CE} min.

Now say we limit it to V_{ON}. That is we will not allow this V_{CE} min to go below V_{ON}, V_{CE} min is equal to V_{ON}. If we limit this to V_{ON}, we effectively prevent the transistor from going to saturation. Now suppose we put this equal to V_{ON}, so V_{CE} min is equal to V_{ON}. So what do we get? We get the third condition that is V_R equal to minus 3/2 V_{ON}, I will write it here. So these are the 3 conditions which we have, one is if we chose I_0 * R is equal to V_{ON}, We chose the current source value and the resistance values in such a way that the product is equal to V_{ON}. If you ensure that the input voltage variation is just V_{ON} around V_R that is from V_R minus 1/2 V_{ON} to V_R plus 1/2 V_{ON} and if we chose V_R is equal to minus 3/2 V_{ON}, we will ensure that V_{CE} min is V_{ON} that is the minimum value of the collector emitter voltage is V_{ON} and which effectively ensures that the transistor does not go to saturation. So collector emitter drop will always be greater than V_{ON}. So this is the design principle. Of course this is very clear now that V_R is minus 3/2 V_{ON}, the input voltage variation is minus V_{ON} to minus twice V_{ON}. So these are the design principles.

Now if we come back to this circuit again. So this is an OR and NOR gate. This is you have both OR and NOR outputs and this output is to be fed as input to another gate. So there is some problem which we see right away. We expect the input voltage to vary from minus V_{ON}

to minus twice V_{ON} because that is how we have designed it, V_R is minus 3/2 V_{ON}, V input should be V_R plus minus 1/2 V_{ON}. So it should be from minus V_{ON} minus twice V_{ON}. What is the output voltage here? Output voltage is going to change from; so if you taking the output from Y_2, when no current is flowing in this branch the output is equal to 0. The voltage here is 0 its ground voltage and when the entire I_0 is flowing in this branch, the voltage is minus V_{ON}. So the output voltage at any output is varying from 0 to minus V_{ON} whereas we require the input to change from minus V_{ON} to minus twice V_{ON}. So that is one anomaly we have which has to be solved for this circuit.

The other problem in the circuit is that what happens is if you feed this output to the input of a next gate say and there is a current source here, just drawing it here. So this output is going to the input of the next stage what happens is this is I_0. So when this branch is not conducting this output should be 0, the voltage here should be 0 but what happens is this transistor, the input is logic high for this, when this output voltage is 0. So this transistor is going to conduct. When this transistor is going to conduct there is a base current which is going to flow, which is going to be equal to I_0 by beta. I mean I_0 by beta plus 1, its almost I_0 by beta times, current which flows here and where is this current going to flow? Through this resistance into the base. So what you are having is a current flow through this resistance and so what happens to this voltage here? Because of this current flowing here, this voltage is going to reduce. So if you have a large number of fan outs I mean all this output here is logic high here. So all the current will flow through this resistance, through all the fan outs.

We have all this fan outs, so all these transistors will be conducting. So this total current here through this resistance is going to be how much? I_0 divided by beta times N where N is the number of fan outs. So this much current flows in through this resistance and so in times R is going to be the drop across this resistance. So the logic high is going to fall, there is going to be a drop in the logic high and which may give raise to problems because the logic swing here is very small. That is deliberately done as you know for high speed circuits. So these are the two problems we have, one is the input and output voltages are not matching. The second problem is that if you have a large number of fan outs, you may have problems because the logic high voltage is going to fall and the difference in voltage between the logic high and the logic low is going to get reduced. So how do you solve this problem, whether it's a very simple solution? What is done is in this circuit the output here is taken through emitter followers. So you have an emitter follower here and the output is taken from this point.

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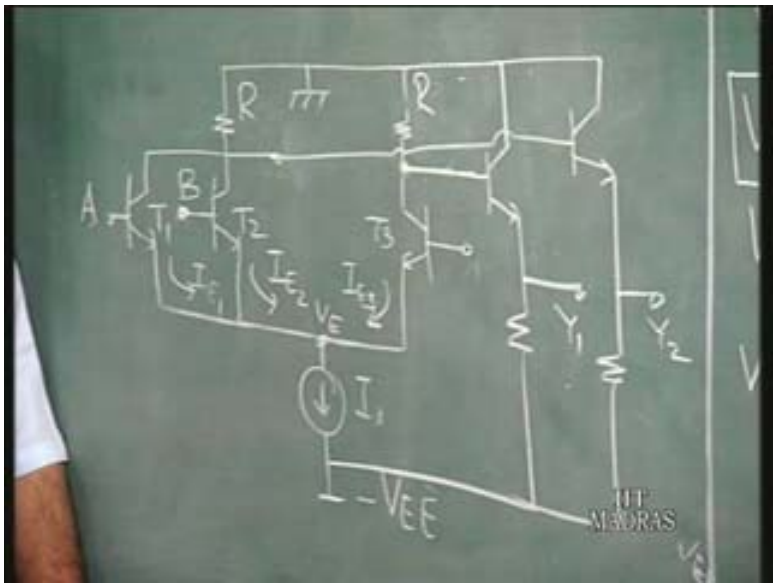

So here this output also, you have another emitter follower, these are the two outputs now. For the two outputs here, now they are taken through emitter followers. Now what does the emitter followers do? How does it solve both the problems? So here now what is the output voltage variation? It is basically shifting the output voltage by V_{ON}. Now when this voltage at the base of this emitter follower transistor is 0, the output is going to be minus V_{ON} and when it is minus V_{ON} here it is going to be minus twice V_{ON}. So it's basically shifting the voltage down by V_{ON}. So the output voltage variation now is going to be from minus V_{ON} to minus twice V_{ON} and that is our requirement for this ECL gate. We have seen V_I is should be V_R plus minus 1/2 V_{ON} and if V_R is minus 3/2 V_{ON}, the input voltage should vary from minus V_{ON} to minus twice V_{ON}. So we see that this effectively solves our problem number one. Number two, the second problem is about having a large number of fan outs, there is going to be a voltage drop in the resistance.

Now in this circuit if you are connecting the fan out here, the output here. Again you have a current I_0 here, so this voltage Y_2 is logic high say, so this transistor the next stage is going to conduct. So if this is I_0 the base current is I_0 by beta and what is the current on the base here. Because there is I_0 by beta but plus a small current this is the usually high resistance, so this current is much smaller. So again if we neglect the current flowing through this resistance. So the current flowing here is I_0, this base current here is I_0 by beta square. So the drop across this resistance here has been reduced by a factor beta.

So previously the current which was flowing through this resistance was I_0 by beta times n. Now it is I_0 by beta square times n. So in beta is quite large this resistance the drop across this

resistance can be reduced. So you see that using a emitter follower at the output we have been able to solve both this problems. So now we can see that this circuit is firstly we have seen that this circuit is going to behave as an OR and NOR gate and only a small input variation around the V_R which is the reference voltage is sufficient to switch the current from one branch to the other.

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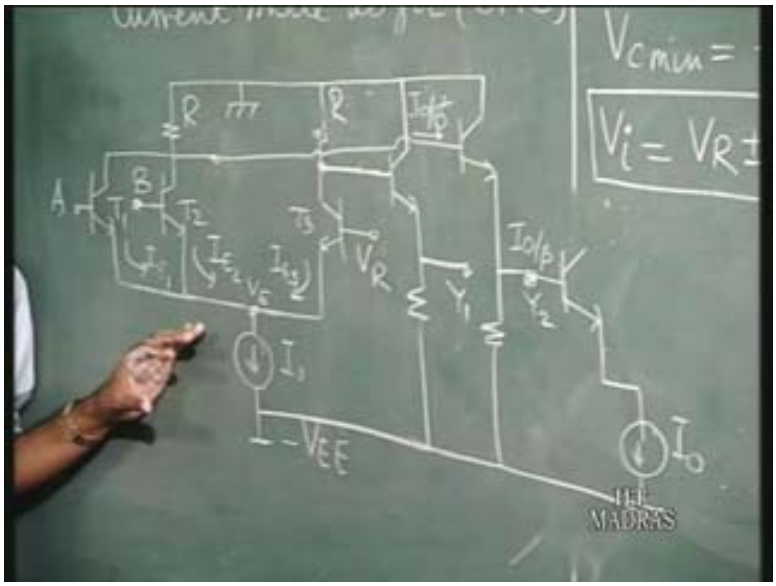

As the current switches from one branch to the other, the output voltage changes from one logic to the other. Also we have seen the condition to ensure that these transistors do not go to saturation. So we have to ensure these conditions while designing the circuit. The three conditions I_0 into R is V_{ON}, V_i must vary from V_R minus 1/2 V_{ON} to V_R plus 1/2 V_{ON} and V_R should be minus 3/2 V_{ON} and if you have an emitter follower, the output voltage is going to satisfy the requirements of the input voltage. That is the output can be fed directly to the input of the next stage and also here there was a small problem related to, if you had a large number of fan outs because that the voltage level itself would change but this could be reduced by having the emitter follower. So from this point of view the circuit is okay. So there is one small point which I think is in the back of your mind. Why we are using negative power supply voltages? The circuit would be perfectly if this was ground here, instead of minus V and you had a Vcc. There would be no difference in the operation of the circuit but why we are using a negative power supply? I will just discuss that now, before we close today.

See the ECL gate like all high speed gates, we already discussed that there is some problem due to noise, all high speed gates suffer problems due to noise because of the vary fast switching and large amounts of current are switched from one branch to the other and because there are some inductions in the circuit which normally you tend to neglect and if current is changing DIDT is fast, is very high and in the inductants you get certain voltages, LDIDT is the voltage. Now all this gives raise to what is called power supply, noise. That the power

supply, the voltage should be a constant but across the power supply you get some noise, when the switching takes place. Because of these interconnections, they are not perfect. They have certain inductants. So all these high speed circuits because of the fast switching which takes place give raise to certain noise across the power supply. This power supply voltages are not dead fixed and this noise should not affect the operation of the circuit.

Now if you take the output now, if you look at the output of this circuit now, usually I will just put some representative values this resistance which is the emitter follower is around 1.5 kilo ohms whereas this resistance is around 300 ohms. That is the resistance at the collector this is around 300 ohms. Now if you assume voltage noise source across the power supply, just take this circuit and you have a 300 ohms here resistance then you have the emitter follower output like this, you are taking the output here. This is 300 ohms, this is 1.5 kilo ohms. Now there are two options either you take the output voltage across this say let us call it V_{o1} or you take the output voltage across this V_{o2}.

Now what is the effective resistance seen from this point? This is going to be three hundred ohms divided by beta. So this effective resistance across these 2 points is 300 ohms divided by beta. Now if the beta is say about 100 for this transistor, so the effective resistance would be 300 by 100 which is around 3 ohms. So the resistance from this emitter point to the top here is around 3 ohms whereas this is around 1.5 kilo ohms and if you have a voltage source like this; this one would be almost equal to V_N and this one will almost be equal to 0. So this is the output either you take the output across these 2 points or you take the output across these 2 points. Now so you see that if you take the output across the lower 2 points, the full effect of noise would be fed at the output. Whereas if you take the output between the two upper points, the effect of noise is virtually eliminated. So it is advantageous to take the output between the upper 2 points and you see in any circuit the ground is always the reference point with respect to which you take the output.

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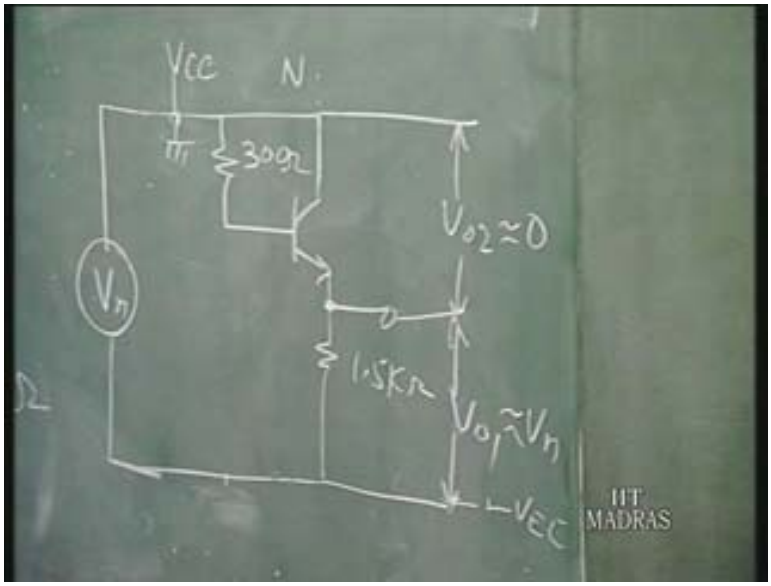

So what is advantageous is to make this ground and put a negative power supply rather than putting this as V_{CC} and this ground in which case you are basically taking the output across these 2 points. So that is one reason why it is advantageous to have the upper point this voltage here is ground and this is negative minus V_{EE}. The other reason is you see in any circuit, as I said the ground is the reference point and if you are housing the equipment in a box or something, you usually make that the ground, you earth it and there is always a possibility that the output of the circuit is coming in contact with the ground or the reference voltage. That is by mistake also the output can touch the ground. If you are taking a wire it can get shorted to the ground. Now if this was ground and you had a V_{CC} here. Now if this output is shorted to ground accidentally, what are you having? This transistor, the entire V_{CC} comes across this transistor and there is no resistance to limit the current. So very large current is going to flow through the resistance and it's going to destroy the transistor. On the other hand if this is minus V_{EE} and upper part is ground, if this point gets touched to the ground there is effectively no problem because you are just having, there is no voltage across this device. So the output point touches ground. No problem. So there is a short circuit protection as such inherently built in the circuit which is not there, where if you take the output across this point and you have a positive power supply with the ground here. So these are the reasons why ECL traditionally uses a negative power supply and that is why it is different also from the other logic families. So we stop here today, we shall continue our discussion in the next class.