Digital Integrated Circuits
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Lecture – 17
Stacked I2L; I2L – TTL Interfacing

Last class we were discussing the variation of I squared L that is the hetero junction I squared L where the hetero junction bipolar transistor is used and we have also seen the advantages of hetero junction bipolar transistors compared to the homo junction transistors and in a hetero junction bipolar transistors we have seen that even with the lightly doped emitter, you actually get a large beta and this largely offsets the problems of I squared L because in I squared L the problem came about because you have to use a lightly doped emitter and so there has been a lot of work on hetero junction I squared L and even now lot of work is going on. so we shall continue our discussion on hetero junction I squared L and what we have been discussing in the last class say hetero junction I squared L or H I squared L and we had seen that the circuit is like this, it is rather similar to the short key transistor logic except for the fact that this is not a short key transistor.

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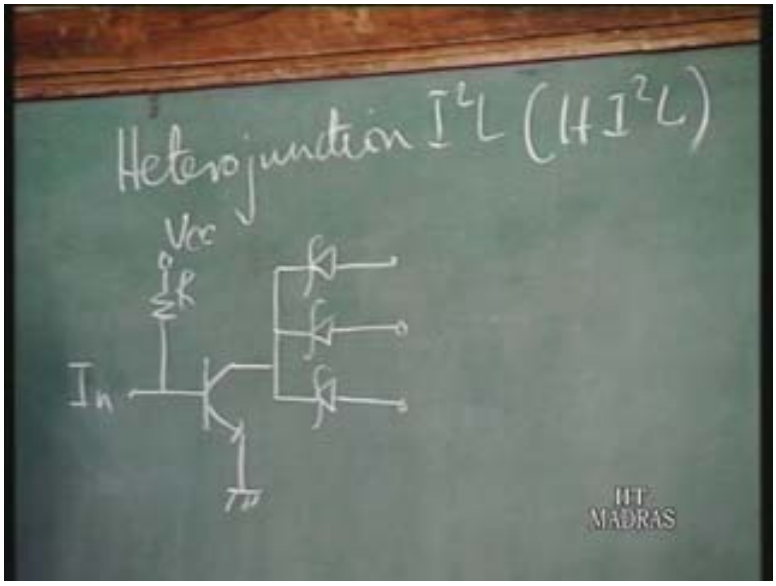

So you have a resistance from power supply which acts as a current source and this current source, this current can either flow into the base of the transistor in which case the transistor has to go to saturation and the output voltage goes slow or if the input is low or then this current flows into the input and this transistor is cut off and the output is going to be high in each case. we also derived the particular relationship or a condition for saturation of the transistor and we have seen that in order to ensure that the transistor goes to saturation beta

must be of the transistor must be greater than V_{cc} minus V_{SD} plus V_{CE} divided by V_{cc} minus V_{BE}.

So this was the relation which we have, into of course the fan out that is the number of outputs of that particular transistor. So this was the relation which we had derived in last class and if we can just plug in some values, suppose V_{cc} is equal to three volts and you see that the values in the short key diode CUT in voltage series values are going to the bit different from what we normally encounter because of the fact that this is a short key diode on compound semiconductor material with, that is the material with larger band gap. So the cut in voltages are going to be much higher.

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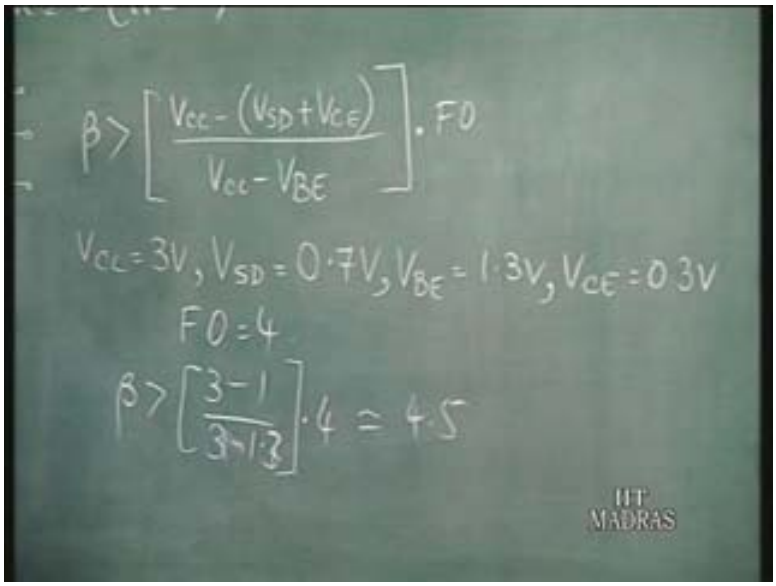

So the short key diode, the drop is 0.7 volts, the base emitter voltage is 1.3 volts and of course V_{CE} is around 0.3 volts or so. That is when it goes to saturation. So if we put these values and for a fan out of four say you have 4 collectors, the four fan out so beta will be greater than three minus V_{SD} plus V_{CE} is one and V_{cc} minus V_{B} is 3 - 1.3 and this works out into four, this works out to be almost equal to 4.5. So you see that a small beta is required in fact to ensure that the transistor actually goes to saturation. So there is no problem as such for the circuit to function properly.

Now what is the structure, I just give you the structure that is a cross sectional view of this device, how does it look like where in fact you see that most of the compound semi-conductor devices are fabricated using epitaxial wafers first where most of the layers are used in the fabrication of the devices or grown epitaxially so the processing is as such after that becomes quite simple. So what you have is as a starting material is three layer structures. You have n plus gallium arsenide, n plus aluminum gallium arsenide, we have already seen last class that aluminum gallium arsenide is a wider band gap material. So basically this acts as the emitter of

the transistor. This n plus gallium arsenide is used as a contact material because it is very difficult to take contact from aluminum gallium arsenide being a wide band gap material, it is very difficult to get ohmic contacts so basically this is the emitter, this n plus algas acts as the emitter and then what do you have is n type gallium arsenide.
So this is the starting material what you have, what is done is then some implantations are carried out that is you implant some material. So what do you do is there are three implants basically in the whole device structure. Three implantations, one for the P plus base so what is done is this region is converted to P plus base and then you have for P plus base contacts, so these are the base contact regions. See the implantation I think is some of you may be aware that through implantation, it is possible to form a junction beneath the surface. That is the different between diffusion and implantation. For diffusion the entire region has to be P, so here what you are doing is depending on the energy of the implant, the element which you are implanting can be implanted deep inside the semi-conductor.

So this P plus implant it is done under the surface of the semi-conductor. So that this region of the semi-conductor becomes P plus and then you do a normal implant like this. So this is P plus so basically this is to take contact for the base and then there is another implant for isolation. Usually in this gallium arsenide material, Boron is implanted at high energy and it creates a lot of damages in the semi-conductor and it basically creates very high resistance region which acts as an isolation. So this is the isolation region. So the basic device structure is you see and n p n transistor. So n p n transistor the P contact is taken from here that's all. Then what remains is you have to take the collector contacts, now here. So this is the base contact, this is the collector and these are the short key diodes. Then the remaining is you have to make a resistance.

So what is done is a thin film resistance, the material is deposited here and on the isolation region and this act as a thin film resistance and this is $V_{cc.}$. This is the resistance material, some material which is deposited, it gives a certain resistance, a thin film is deposited and you may contact to the P region which is the base. So what you have if you look at the structure. So this is $V_{cc.}$ so I will redraw the structure from here. So $V_{cc.}$ through a resistance it comes to the base of the transistor. So $V_{cc.}$ through a resistance comes to the base, you have a transistor this is the base, you have n p n transistor, emitter is grounded and this is the collector region, from the collector region you have number of short key diodes. So it's coming out, so this is the particular structure and this is the structure of the hetero junction I squared L basically.

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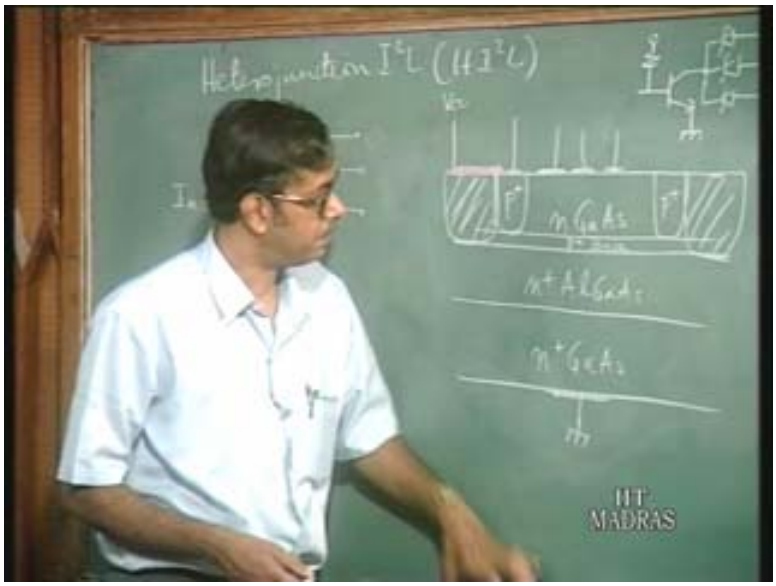

So this is you see once you have the wafer, it just the few implantations and you get this particular device. So this is the hetero junction I squared L structure which is rather simple structure as such and of course the important thing is because of the larger wider band gap material as emitter, you know that the charge storage is going to be very small and that is the most important thing here.

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So this type of structure was proposed and lot of work has been done Texas instruments and I just give you the reference again.

If you want for further reading,

H T Yuan and others, IEEE transactions electron devices, volume 36 pages 2083-2092, 1989.

So where this hetero junction I squared L was proposed, in fact they had been working on this particular structure for long time and in fact they have also fabricated microprocessor. This paper they had reported that they had fabricated 12872 gate mew P using H I squared L and with a clock frequency of 125 megahertz. Now 125 megahertz may not sound very high but you must remember that this was in 1989, when you didn't even have the 486.

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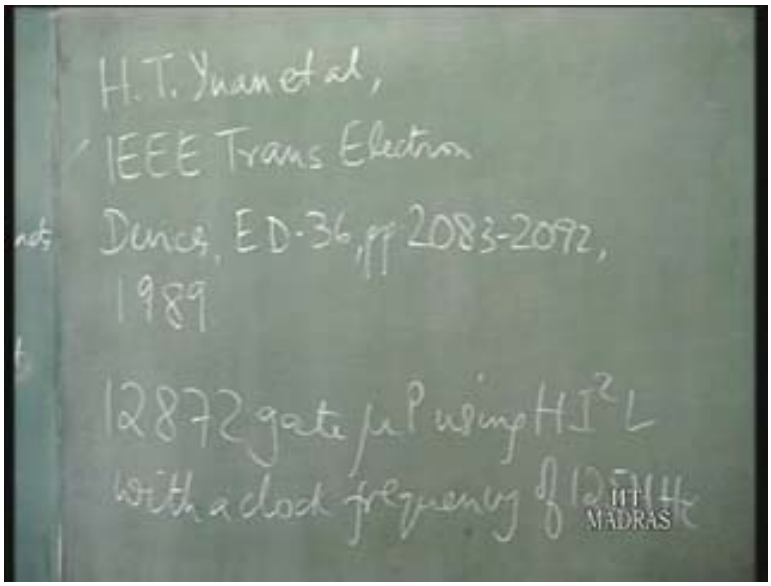

I think so and that time 125 megahertz was very high clock frequency for a CPU. I think it was those times 386 and all used to operate below 50 megahertz. So this was the high frequency and also for the gates, for a 1.5 micron process and a fan out of 4, the delay for the H I squared L was obtained as 150 picoseconds at power dissipation of 5 milli volts per gate. Power dissipation was little higher side but the delay was at, for a fan out of 4 the delay was just 150 picoseconds and the fan out of one, the delay was just 85 picoseconds. So fan out of one, the delay was eighty five picoseconds and for fan out of four the delay was hundred and fifty picoseconds.

So you see that this is a very high speed I squared L, go to sub hundred picoseconds. The point is after 1989 not much report has come out of this, although at that time this was really very high speed device. one reason is of course you know that the compound semiconductor devices are rather expensive and that is why it is very difficult to market them compared to others and also many of these companies, you can do it for research purpose but once if you go for production it requires a lot of investment and many of these companies are not willing to do that maybe that could be one reason I think but really we have not heard much about it later.

Although it was very promising at that stage but then but lot of work has been going on from other people also in this area about hetero junction I squared L in fact there has been a very recent report I should say it is as late as December 1998, again I can give you the reference just if you want, just give you an idea of the research which is going on in this area.
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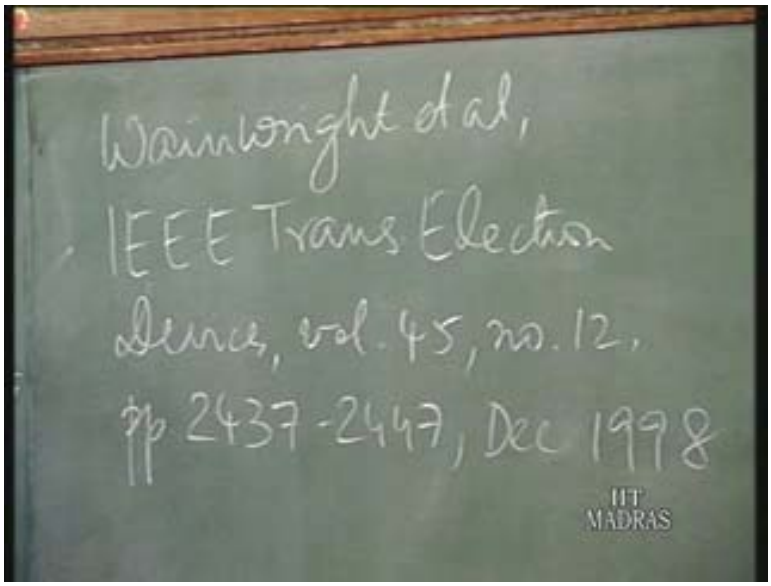

Wainwright and others, IEEE transactions electron devices, volume 45, number 12, pp 2437-2447, December 1998 that is the latest paper as seen on this topic. What they have done in this paper, I will just briefly tell you that they have examined different structure. this mostly simulation work, they have done. they have examine many structures of hetero junction I squared L and they have studied specially one particular structure which was proposed initially

what is called substrate fed logic this is another variation of I squared L basically were the injector is at the bottom. So I will just show what the structure is that they have studied. So you have the injector is at the bottom that is the idea of substrate fed logic that is the injector contact is from the bottom. So you have the P, you have an N so PNP transistor is actually a vertical transistor in substrate fed logic rather than lateral transistor.

So this is an isolation, this is N contact from here and you have layer of silicon germanium here. So this is the silicon device, this is silicon germanium. Now silicon silicon germanium is also a hetero junction, silicon germanium has a lower band gap compared to silicon and so this is the hetero junction and so this is one of the structures they have studied. So this is P plus and this is N. so if you look at this structure, what you have is PN, this is P type silicon germanium. Now this silicon germanium, this is the only region which is silicon germanium and the remaining part is silicon. So basically the silicon germanium has been grown epitaxially and this has been done selectively. Nowadays it is possible to do growth selectively, certain regions you want to do silicon germanium that is also possible.

So basically you have a silicon germanium here and the other regions are all silicon. So you have a PNP structure, this is the injector and so this P region is actually the Vin point, input point and you have the NPN transistor. So for this transistor, this is the output, this is the collector, this is the emitter of the NPN transistor. So this is grounded, see this is basically contact for this point. This side you have taken the contact for this point. So this is the NPN transistor. So I can put it this way, this is the collector of the NPN, this is the base NPN transistor and you have a PNP here. So this is also P type and this is the emitter of the PNP. So what do you have? This is the injector terminal, so you have a PNP and you have an NPN. The PNP emitter, this is the injector point, the N of the PNP that is the base of the PNP is the same as the emitter of the NPN.

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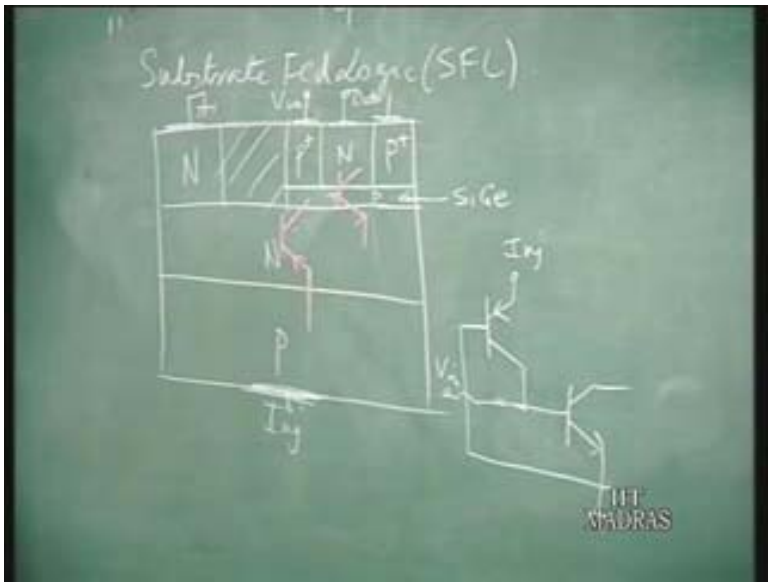

So this is the same as the emitter of the NPN and this point is actually grounded here, this N region is actually grounded. so this is the ground, the collector of the PNP is the same as the base of the NPN and this is the input point Vin and you can have multiple collectors like this, just one collector is shown of course, can have multiple collectors. now so this is the basic I squared L structure and what they have done in that paper is actually they have analyzed the structure, they have optimized this structure that is they have taken different dimensions, different charge storage in the different regions and they have done a thorough analysis and also made small modifications, slight modifications of the structure, I don't want to go into it. Because it becomes more complicated but the interesting thing is that they predict that with this particular structure, one can actually go down to a switching speed of 34 picoseconds at a minimum geometry of 1.4 micron. So that is the outcome of their work.

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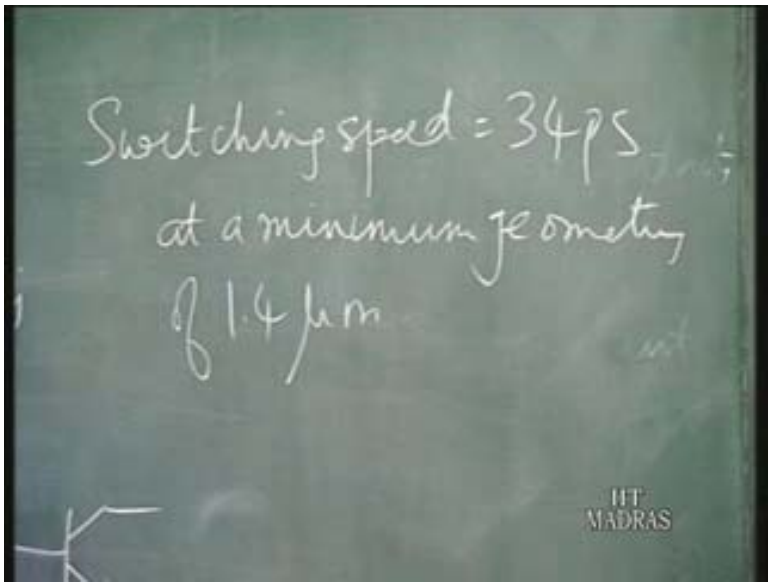

So basically by going through this, what I want to impress is number one there is still a lot of interest in I squared L, you know in terms the logic family although it had a problem high speed and people are working on it and to reduce the delays and see how it can be improved because if I squared L has its inherent advantages that is it has got low power dissipation and high packing density, if you can couples speed with that it is going to be a very powerful logic family. So people are working on that and there are one way to do it is hetero junction I squared L. in fact the delay is one talking of its quite remarkable. It is just thirty four picoseconds, if you really make it a very high speed logic family. Although we don't really associate I squared L, we don't really call I squared L a high speed logic family. So that is the why I wanted to introduce this to you and this is the very recent work. so with that I think we come to the end of this discussion on high speed, I mean the different efforts which is going on in order to make I squared L a high speed family that is from technology wise they we have seen self-aligned technology improves the speed, reduces the delays and then these efforts that is some circuit modification like the short key transistor logic as well as this hetero junction I squared L concepts.

So before we actually close the topics on I squared L, I would like to make just one or two small points about I squared L before we move on to other logic families. See I squared L, one of the major advantage is as we said was power dissipation, was low power dissipation because and one of the reason behind that is that you require a very low power supply voltage. The maximum voltage in the circuit is going to be around 0.7 to 0.8 volts that is the base voltage. It does not exceed beyond that because if you look at the circuit here, this particular I squared L cell, this is ground. This junction to be forward biased, this voltage or this point cannot exceed say 0.7 to 0.8 volts because you cannot forward bias a junction beyond that. I am talking of silicon again and any junction, if this voltage also cannot be more than that.

So you see that is the limit, so in fact an I squared L circuit can be operated at power supply voltage of low as one volt or something. so what you have is so this is the emitter of the PNP and if you have other circuits, you have this is the common point, all the emitters of the PNP's are common or you can even consider this as a multi collector transistor and this goes as current source to different nodes. Now so basically you can consider the I squared L as this is the power supply, you have a resistance and this is the I squared L circuit, I squared L block and this voltage here is going to be around 0.7 maybe slightly more. So you can control the current which is flowing in by using by this $V_{cc.}$ and R and you know we have already seen that the effect of current on the various parameters like noise margin, delays, etc. so it is important thing. One interesting thing is that in many circuits, many systems, you may have a system where not all the circuit is made out of I squared L.

You may have part I squared L, the other parts maybe TTL or any other some other logic family and you may want to have a common power supply voltage that is you have a common power supply which is driving the different parts of the circuit. now this $V_{cc.}$ maybe 5 volts, if you are having other, this $V_{cc.}$ goes to TTL part for example you require five volts and so this

is say 0.7 volts and the same current is flowing through this resistance and this I squared L. so what are you having, see you have a low power circuit here but if this is 0.7 and this is 4.3, 6 times more power is dropped in the resistance compared to the I squared L. So actually having a low power circuit is of no use because you are just wasting power in the resistance.

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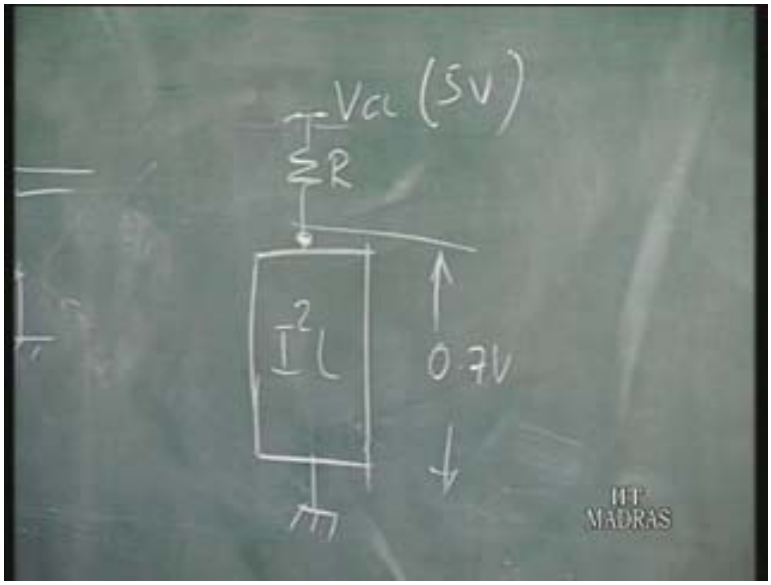

Basically you have large power drop in the resistance. So what can you do? So can we change the I squared L circuit in some way, So that you have the same power dissipation but you have a higher voltage here but say less current. That is suppose instead of 0.7 volts, I can have 1.4 volts here, at drawing half the current I would save power which is wasted in the resistance. For that is the idea which people working and they came up with particular types of I squared L, called stacked I squared L. so basically what you have in a stacked I squared L is, you have this is the current source, so you have circuits like this. So this is the I squared L, this is the injector, so this is the base which goes to ground here. So this is the one I squared L cell.

Now what you have is here again you have other circuits and for example you can have different levels that is see what do you have now. So this is one level, so you have three levels of circuitry here. This is the injector, this is going to the base I just drawn it like this, you can have more complicated circuitry. So what you have is going to the base, this is one level of I squared L circuitry and from here this is again to the injector to another injector. so whatever current flows in this you know, so all the current must flow back again in this way and again you have another level of I squared L circuitry and again all the emitter currents must add up, all the currents flowing into this level must flow out of this level and this whatever flows out flows in as injector current here and again you have another level of circuitry. So what you have done is so if you have large circuitry, say in one level and you can break up the circuitry into three parts where there is no interaction as such between the different parts and fabricate them at different levels.

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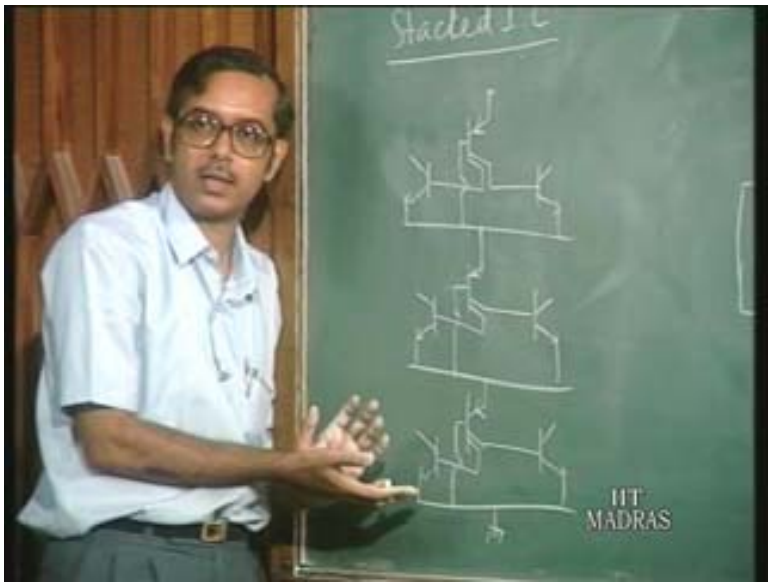

So what you have done is you see that this voltage is 0.7 volts, this one will be 0.7 volts, this one will be 0.7 volts, so the entire circuitry would be 2.1 volts and since the amount of circuitry in each level has reduced by one third. So the current which you require at each level is reduced. So you are consuming the same power but what you have done is the total voltage drop across the circuitry has increase a three forth and the current has reduced by one third.

Now if you again go back to this model which we have here, now if this is one up to "two point one" volts instead of "point seven" volts and the current which is drawing here is one third. So the power dropped in this resistance is going to become one ninth of what it was drawing initially. So basically you have saved lot of wastage of power. So this is particularly useful for when you are fabricating, when you have different types of circuits which is driven by a common power supply. So this is one type of stacking, there is another type of stacking. So you have a current source like this which is again is a PNP transistor. So you may have something like this, these maybe two inputs just like in a normal I squared L and then you have another transistor here and you may have another transistor here. So what is the logic here? This is the NAND logic because it is at the collectors so this is the output at the collector of some transistor.

So this is the NAND logic that is if any of these inputs go low A or B goes low, what happens is the current is going to flow this way, the transistor is going to cut off and the output is going to be high. So NAND is if any input is low, output is high that is the logic in a NAND gate. So this is A B bar. So if you have C here, that's a other input what is the output here? This is going to be A B C bar that is if any of A B or C is low output is going to be high. See if A or B is low then what happens is the current is flowing this way. So this transistor emitter there is no current, so there is no chance for this transistor to go to saturation. only when A and B both

are high then only this transistor turns on and then only the second level transistor has a chance, this emitter current can flow in a base current and so if now C is low, this emitter current will flow into the input, this transistor is off but if C is also high then only this transistor is turned on and the output goes low. So only when A B and C is high then only it is. So if you have D here, you have A B C D bar. This is the NAND of A B C and D. so this is another concept of stacked I squared L both can be used, it also depends on what circuit you are doing.

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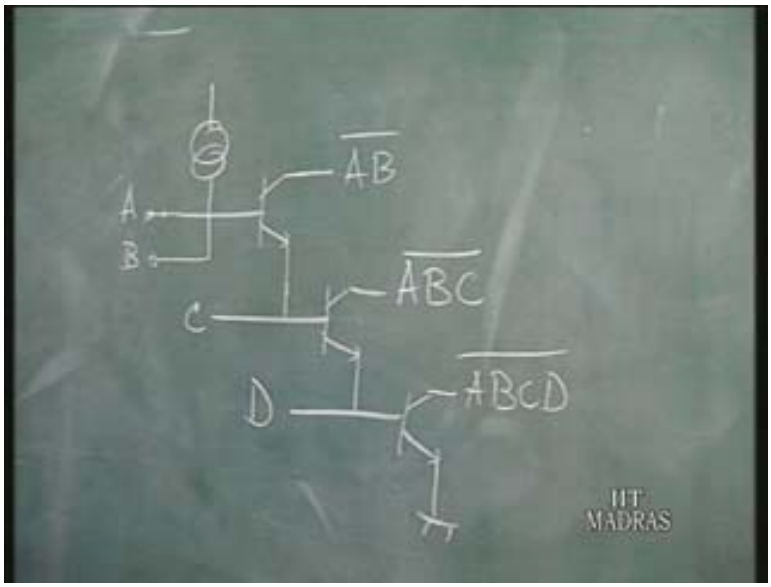

In some cases it is advantageous to use this type of stacking; in some cases it is advantageous to use the other type of stacking. So these are the some of the concepts of stacked I squared L, just one further point on this stacked I squared L that is it is possible to have the output of one level going as input to the other. It is possible. The only thing is that in some cases you may have to do a level shifting. In fact I think it is, you can see for yourself that if you take the output of one lower level transistor and you feed it as input at a higher level say here. the output of one lower level transistor and feed it as input at higher level, level shifting is not necessary, you can do it directly because of the fact that if this transistor is cut off, if this transistor is really cut off then this is not drawing any current. Basic idea is when this transistor is cut off they should not draw a current and this current source current will turn on this transistor. So there is no problem if this transistor is cut off, this is not drawing a current. When this transistor goes to saturation, current will flow in here and the upper level transistor here is not going to go to saturation. This is going to be cut off, no problem but the problem is that if you want to take an output of an upper level transistor and feed it as input to the lower level that cannot be done. Why? Because you see that if you assume that the voltage levels are shifted by “point seven” volts.

now here, at the emitter of the second level if this voltage is 0.7 volts and when this transistor goes to saturation, this collector emitter drop is 0.2 volts, its 0.9 volts and if you feed it at the base of this, you expect this transistor to be cut off but 0.9 volts is not going to cut off the transistor. So level shifting is necessary, if you are feeding the output of an upper level transistor to a lower level transistor. The collector of an upper level transistor is fed as input to a lower level but if you are feeding the collector of a lower level transistor to as input to the upper level it is not necessary. this is true for both the types of stacked I squared L. so one has to take care of that; that is level shifting means you may have to drop the output of the voltage by a one diode drop 0.7 volts. so you have to shift the voltage down, so it is possible to interact between two levels with level shifting but when you design I mean stacked I squared L, you should see to it that the levels are so chosen, the circuitry at each level is so chosen that there is minimum interaction between levels because that will add to problems.

the problem is of course that here you see that one has to really isolate each level because all this emitters are shorted in one particular level but this is not grounded actually. So this emitter point, for this set of transistors is different from the emitter point of this set of transistors. So you cannot have a common substrate in which you fabricate. You have to isolate them, these each individual levels so that creates problems also from technology point of view. So that is about stacked I squared L one point. The last point I would like to make is I squared L you know that the voltage levels are different from the normal TTL levels. So if you want to interface I squared L with TTL, TTL is generally assumed as a standard sort of. So you have to have them as some intermediate circuitry. How to do it? so suppose you have an LSTTL, I am just drawing the two ends of the circuitry, so this is the input side of an LSTTL and the output side you have something like this. These are of course short key diode. I am not drawing the internal circuitry just the two other ends.

Suppose you want to interface I squared L with LSTTL, what do you do? Now I squared L NPN transistor that's right, this output has to be fed as input to the TTL. Very simple, this output transistor you put a resistance same five volts maybe and this can be fed directly to TTL. That is if this transistor goes to saturation, this 0.2 volts of the collector so this is going to be seen as a logic low by the TTL and if this transistor is cut off, I mean it is going to be seen as a logic high. This voltage here is going to be seen as a logic high by the TTL circuit. So this is very simple, you just connect resistance here and you can connect it as input to the TTL.

In the other side if you want to give the LSTTL output as input to I squared L, what do you do? Basically what do you do is you make a sort of potential divider type of circuit and this can be fed as input to the I squared L. Idea is that this input here, if this input is low this transistor must be cut off and if this input is high, this transistor must go to saturation. Basically you also have a current source here, you must be remember. Now you see that if this is low that means when the output is low? When the lower transistor is in saturation, so this voltage goes to 0.2 volts. so there is no way this transistor can turn on because this voltage at the base is not going to be any higher and when the output of this TTL is high that is this transistor is off and this transistor is on, the current is going to flow in here and basically this is not going to sink any

current. So the whatever current source here, this current is going to flow in here into the transistor and it is going to turn on this transistor.

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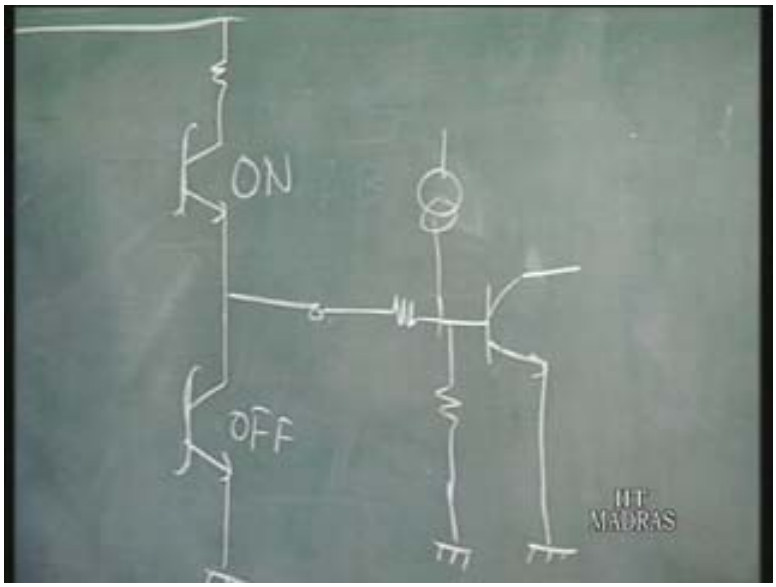

So this resistance values, one has to actually choose proper values depending on the voltages that can be done. So basically you have a circuit like this at the input and which can be used to interface the TTL with the I squared L. so I think this brings us to the end the topics on I squared L.

So we have gone through this topic of I squared L. I squared L well, it was as I just briefly summarize it was invented in early nineteen seventies in the Philips laboratories as a circuit concept, it was very I mean in those days it was sort of revolution and lot of work was done in that level because of it was felt that it is as a bipolar logic family, one can really go in for very large scale integration.

The notable things were that there is no resistance in the circuit, the low power dissipation. These are the two important things with respect to large scale integration but the problem was of course it had high delays because of the varied structure. as we had seen, lot of work is going to improve in this aspects and technology wise, technology has been improved and using self align technology one can actually reduce the propagation delay and also other circuit variations like short key transistor logic has been tried out and also hetero junction I squared L which actually is the area where people are working at present in this I squared L feel and maybe in future hetero junction I squared L will really become very attractive because it has got all the advantages of high speed, low power dissipation and high packing density. so the only thing is of course in this hetero junction I squared L, all this hetero junction the problem is nothing to do with the circuit, actually it is more expensive than silicon.

So that is one of the reasons, one of the thing that has to be sorted out and once if it happens in the future maybe this will become very popular.
With that we close this topic on I squared L and next class we shall start on ECL.