Digital Integrated Circuits
Dr. Amitava Dasgupta
Dept. Of Electrical Engineering
Indian Institute of Technology, Madras
Lecture – 14
I2L Condition for Proper Operation; Noise Margin

So we shall continue our discussion on looking at the conditions for proper operation of the I squared L cell. That is how to ensure that the NPN transistor in an I squared L cell actually goes to saturation because as we had seen the condition of the PNP transistor at the base that is the current source, this PNP transistor is actually in saturation and so it has to be ensured that the base of this NPN transistor gets sufficient current in order to drive this transistor to saturation. So we had started that discussion and so this is the I squared L cell and this is the transistor with say n collectors, n is any number.

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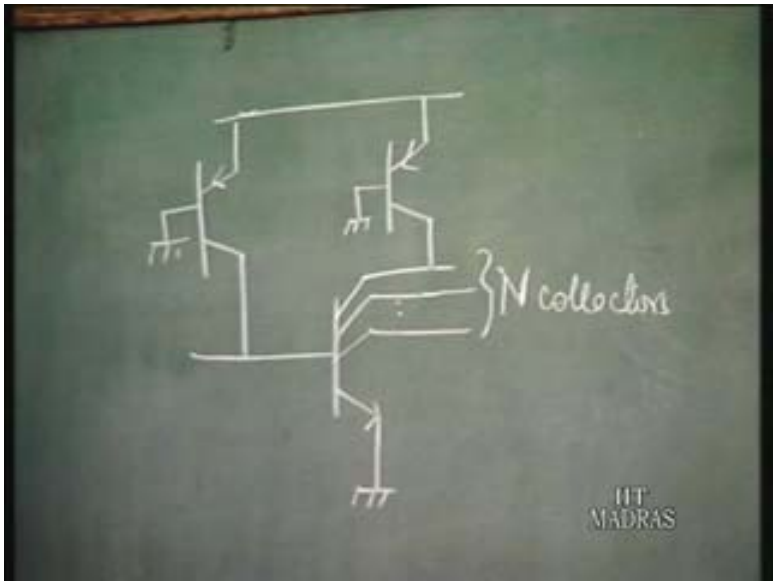

As we had said that we will assume that this multi collector transistor having n collectors is actually n transistors in parallel. That is the base and emitter are in parallel, the bases are all shorted, emitters are all grounded and they just have separate collectors. So basically they are n transistors and the transistor parameters which will talk of like IS the Ebers-Moll model refers to each individual transistor. IS, when we say is actually the saturation current for one of these transistor. So again the model which we will be using is the Ebers-Moll model, I will just draw it once more. So you have three current sources and this is the collector, this is the base, this is the emitter. So this current source is I_S by beta_R exponential V_{BC} by V_t minus one. This one is I_S by beta_F exponential V_{BE} by V_t minus one and this is I_S exponential V_{BE} by V_t minus exponential V_{BC} by V_t.

So in this model we will try to derive a condition for the values of these parameters of the individual transistor that is I_S and beta of the NPN and PNP which must be satisfied so that this cell works. That is this transistor NPN transistor goes to saturation. Now the condition for saturation we know is that when the base current, the beta times I_B is greater than I_C. So if you consider them as n transistors, so the total collector current for the n transistors is n I_0, so this is beta, I write N here to differentiate between the beta of the forward and the reverse. Beta$_N$ I_{SN} so base current of the NPN transistor, if we go back again to this model, the base current is given by the sum of these two current sources. Now assuming that V_{BC} is less than V_B, although the transistors actually is in saturation but when it is just going into saturation, V_{BE} is much greater than V_{BC}. May not be very much later but because of the exponential relation, if this V_{BE} is 0.7 V_{BC} is 0.5, 0.7 by V_t exponential is going to be much greater than "point five" by Vt exponential because of the exponential nature.

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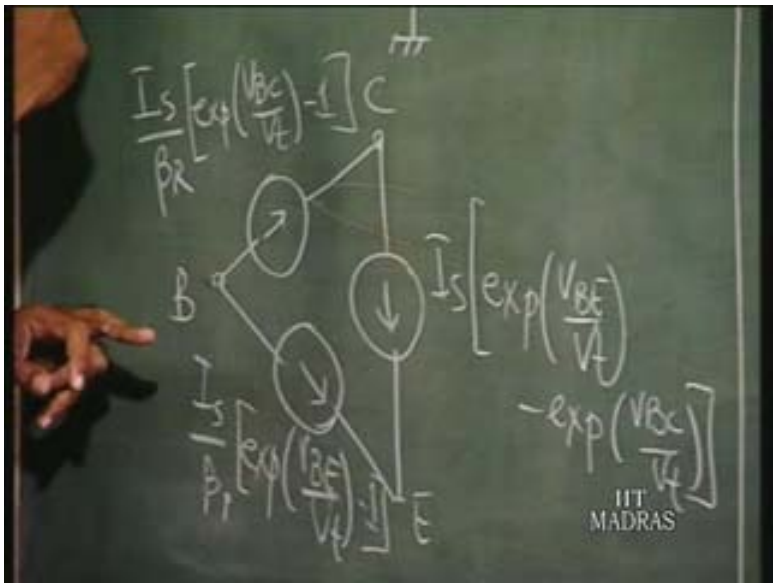

So we can neglect this part and we can just take exponential V_{BE} by V_t. Here what I will do is again I just write this voltage here, I call this voltage V_2 and I call this voltage at this point V_1. Of course this is coming from some external region but this voltage is V_1 and this voltage here as V_2. So this becomes exponential V_2 by V_t, so this is for one transistor and this must be greater than I_0 where I_0 is the current flowing in here. Now here I call this I_0 (Refer Slide Time: 07:08). So the condition for saturation is I_{SN} exponential V_2 by V_t must be greater than I_0, so this condition must be satisfied.

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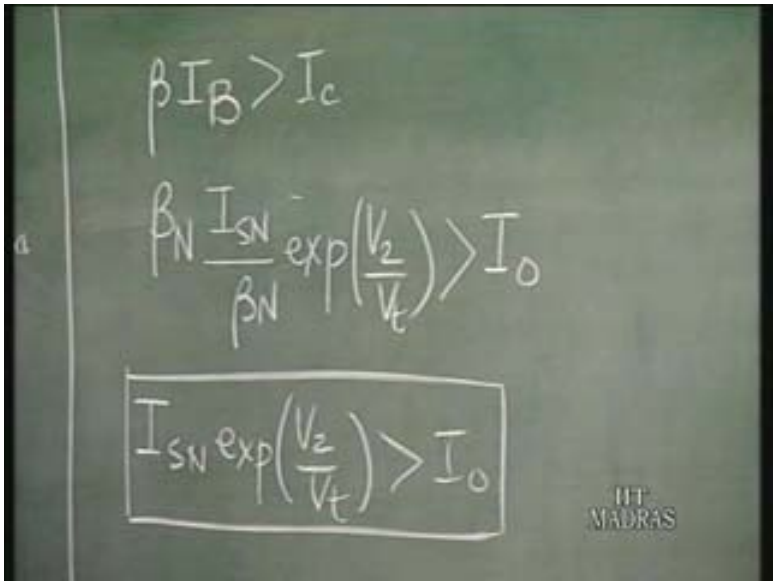

So of course if you have n transistors, the total collector current is going to be n times this and here you have to consider n times the total base current which is n times given by this expression. Now what is I_0? It is the current for this PNP transistor. Now for the PNP transistor, the base emitter voltage is going to be around 0.7 volts of that order whereas the base collector voltage, this transistor is in saturation we are looking at the condition for saturation. The base collector voltage is around 0.2 volts. The base collector voltage is much less than the base emitter voltage. When we look at the PNP transistor so it is in the active region, this PNP transistor. I call this P_2 and let me call this P_1, so P_2 is in active region and so here we can say V_{BC} for the P_2 transistor is much less than V_{BE}, the base collector voltage is much less than V_{BE}.

So the collector current can be expressed as, I_0 can be expressed as; so this is going to dominate, all the V_{BC} terms as small. So you can say that I_{SP} stands for the I_S of the PNP transistor, exponential V_{BE} by V_t for the PNP. So what is that voltage? V_1, of course V_{BE} is minus V_1 but see that the current detection are changed. I mean we can write in terms of V_1 by V_t. So I_0 is I_{SP} exponential V_1 by V_t, so this I_0 value is given by this. We have to see that this condition is satisfied.

Now at this point the next thing what we do is we write an equation of the current at this point. So when this transistor goes to saturation it means that all the transistors whose collectors are connected at this point are cut off. So whatever collector current is flowing for this PNP, that is P one flows in as base current of the NPN transistor. So we can write an expression, I will

call this node A at collector current IC of PNP is equal to I_B of NPN. So what is the collector current of PNP given by? Again we go to the Ebers-Moll equation, collector current is this current source minus this current source so I write I_{SP} exponential V_{BE}, V_{BE} of the PNP is again V_1; V_1 by V_t minus exponential V_{BC} by V_t which is with exponential V_2 by V_t minus this current source.

So I_{SP} by beta P that is the beta of the PNP transistor, actually this should be the reverse beta of the PNP transistor but since the PNP transistor is lateral transistor, it is not a vertical transistor. It's a lateral transistor with the two emitters and collectors side by side, the reverse and forward betas are almost the same. So we can take it as beta P which is the beta of the PNP transistor. So I_{SP} beta P exponential the base collector voltage; base collector voltage of the PNP is again V_1.

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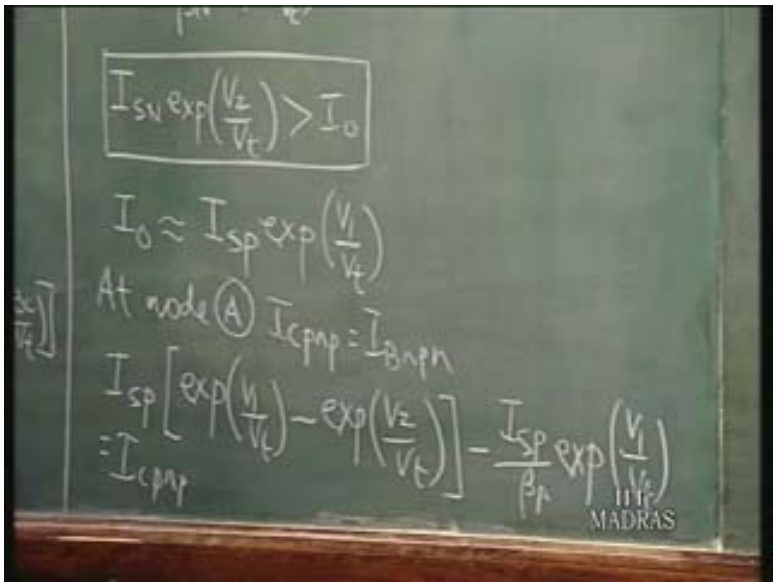

So this is the collector current of the PNP transistor and this has to be equated to the base current of the NPN transistor. So what is the base current of the NPN transistor? So this is I_{Cpnp}, I_{Bnpn} is going to be equal to again the base current is the sum of these two current sources, for the PNP. So we have already taken that so I_{SN}, so there is n times total base current I_{SN} by beta N exponential V_2 by V_t. So what do you get now? So we have to equate these two equations, the I_{Cpnp} with I_{Bnpn} and then we have to get the condition for saturation. Now once we equate that we can write it this way. The equation now what you get finally, you can write it as I_{SP} exponential V_2 by V_t is equal to I_{SP} exponential V_1 by V_t minus, so this is equal to this thing. I think there is some mistakes somewhere. At node A, ISP exponential V_1 V_t minus exponential V_2 by V_t minus V_{BC} this one is the mistake I think (Refer Slide Time: 16:28). This has to be minus exponential, this is for the PNP, this is base collector, this is V_2 we made the mistake here.

So this is I_{SP} by $beta_P$ for the PNP, just we go back here. I_{SP} exponential V_{BE} by V_t minus V_{BC} by V_t. So exponential V_1 by V_t minus V_2 by V_t minus I_S by $beta_R$ exponential V_{BC} by V_t. So for the PNP, V_{BC} is V_2, so this has to be V_2. So this is going to be equated with this (Refer Slide Time: 17:19). So now I think I just rewrite this, this becomes I_{SP} exponential V_1 by V_t equals I_{SP} exponential V_2 by V_t plus I_{SP} by $beta_P$ exponential V_2 by V_t plus NI_{SN} exponential V_2 by V_t. So this is equal to, I can write I_{SP} plus I_{SP} by $beta_P$ plus N I_{SN} by $beta_N$ exponential V_2 by V_t. Now I_{SP} exponential V_1 by V_t, what is that?

That is the same as I_0. Isn't it? ISP exponential V_1 by V_t is given by I_0, we have already derived that. So this term which we have here is actually equal to I_0. So I can write here this ISP exponential V_1 by V_t is actually I_0, the left hand side is equal to I_0, so I_0 is equal to this expression. Now again coming back here, the condition for saturation is that I_{SN} exponential V_2 by V_t which must be greater than I_0. So I_{SN} exponential V_2 by V_t must be greater than that which is again some term into exponential V_2 by Vt. So what can I write? I_{SN} must be greater than, so you see that we have removed all the voltage dependencies which is very important.

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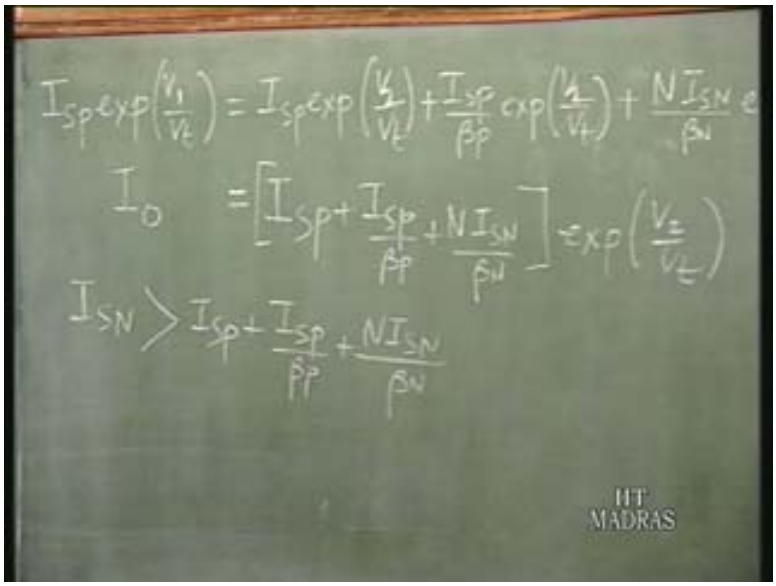

So now we have a relation between the different saturation currents, the number of collectors and the beta of the individual transistors. So I_{SN} must be greater than I_{SP} plus I_{SP} by $beta_P$ plus N I_{SN} by $beta_N$. So this condition must be satisfied in order to ensure that the transistors goes to saturation. Now you just do some small manipulation. We can write like this, I_{SN} must be greater than I_{SP} plus I_{SP} by $beta_P$ must be greater than one. Basically this divided by this must be greater than one or you can write one by I_{SP} by I_{SN} plus I_{SP} by I_{SN} into one by $beta_P$ plus N times N by $beta_N$ must be greater than one. So this condition must be satisfied.

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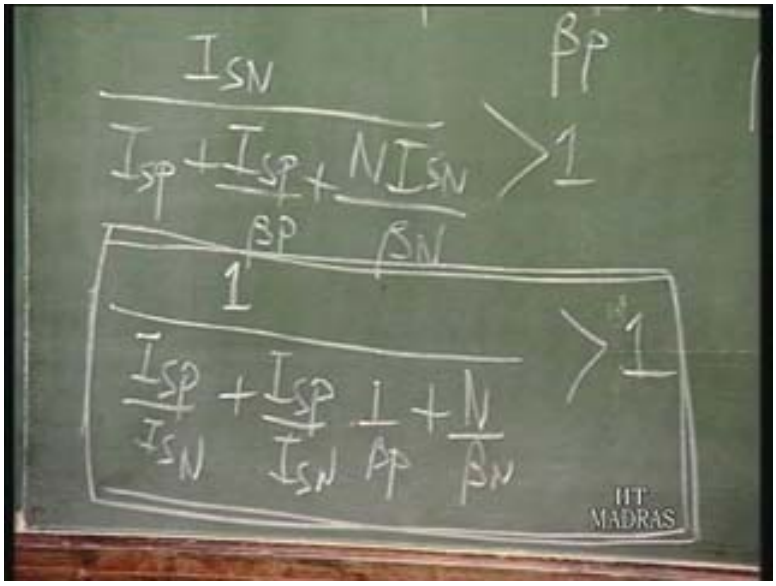

So when you say that this has to be greater than one what does it tell you about the denominator? This denominator must be less than one. Now this denominator consists of three terms so if this A plus B plus C has to be less than one, each individually has to be less than one. So I_{SP} must be less than I_{SN}. So some conditions we can write down straight away. I_{SP} must be less than I_{SN} then what we can say about beta P? So again this must be less than one, so I_{SP} must be less than beta p times I_{SN} or we can write like this, I_{SP} by I_{SN} must be less than beta. Also N must be less than $beta_N$.

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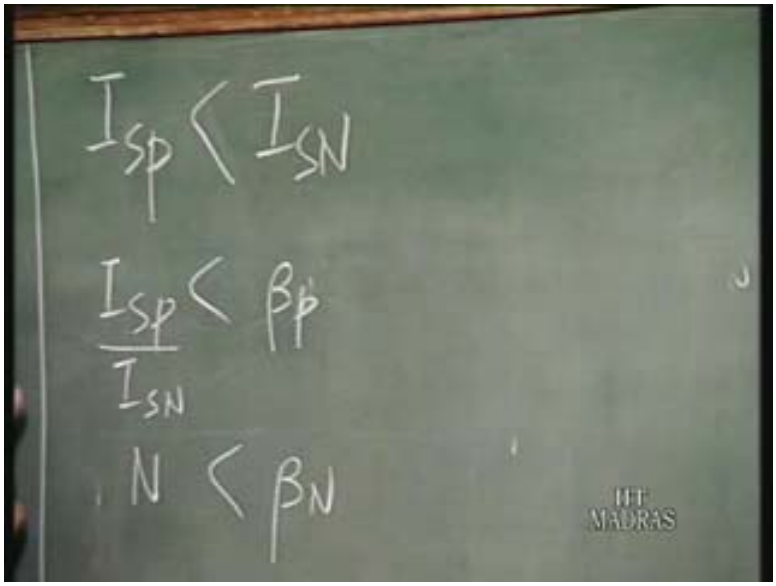

So these conditions must be satisfied but one must be careful that these are necessary conditions but they are not sufficient. In the sense that if this ensures that each of these individual terms in the denominator is less than one but if each of these terms is less than one it doesn't mean that this is going to be greater than one. So these are necessary conditions which must be satisfied but these are not sufficient conditions. So make them as small as possible. Another term which is very often used, so this condition must be satisfied. Another way of writing that expression is one term is called the beta effective is equal to beta_N. So if you multiply both the numerator and denominator by beta_N that expression there, you have beta_N by N plus beta_N by beta_P I_{SP} by I_{SN} plus beta N I_{sp} by I_{sn}.

This must be greater than one. This is called the beta effective, this term. The same, this here in this expression which we have shows that this fraction must be greater than one. Multiply the numerator and denominator by beta_N on the left hand side so it's greater than. So this term, you write like this. This is beta_N divided by where beta_N is actual beta of the NPN transistor but this is the effective beta of the I squared L cell. That is if you consider that in this cell which we go back to the cell that is if this current source is equal to this current source and then if you have an NPN transistor, if the beta is greater than one the transistor should go to saturation. That is if the collector current is the same as the base current and then the condition for saturation is the beta must be greater than one.

So this is the effective beta because from the same point, you are having two PNP transistors here. So just because of this configuration here and because of the condition of this transistor, normally if both the transistors were identically biased, these two transistors you could have equal currents and then this transistor would go to saturation if the beta is greater than one. So now what you have is an effective beta because of the different states of this two PNP transistor P_1 and P_2. So the effective beta must be greater than one. So the beta is modified as such, if you consider it as a cell instead of a transistor, effective beta of the cell so beta_N by N it's quite obvious because you have N collectors, the collector current is N times.

Again if you have same current source as I_0, the collector current would be N times I_0 and this one would be I_0, beta has to be greater than N for the transistors to go to saturation. So this N is coming because of the large number of collectors and the remaining terms in this beta effective expression is coming because of the fact that the PNP transistors at the base that actually going to saturation which means that the current source at the collector and the base they are different values. They are not the same values.

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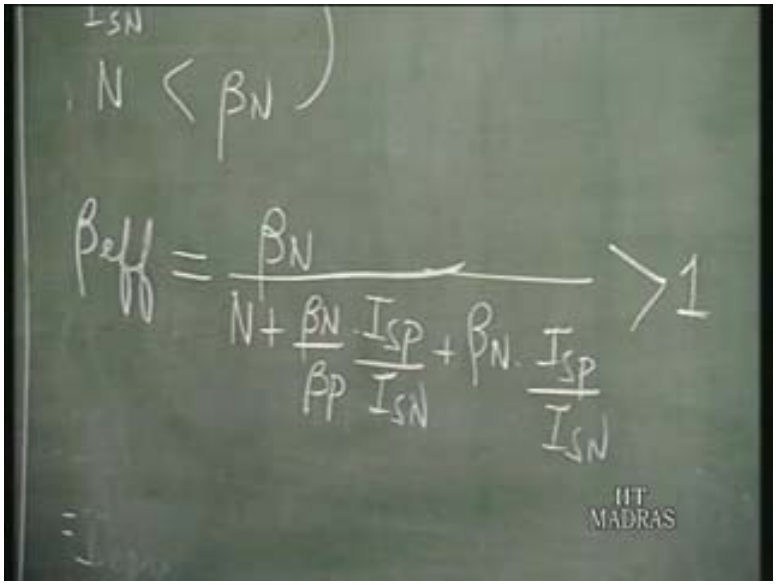

So this is effectively modifying that expression. So this is the beta effective of I squared L cell and this is the figure of merit for any I squared L cell and the larger this value, of course it is better and this must be greater than one for the transistor to go to saturation. This also tells us from this expression, we can also calculate the different values of the different parameters that is required for proper operation of the circuit. For example I just give a small problems say, suppose you design such that I_{SP} by I_{SN} is equal to 0.2 and $beta_P$ is equal to 0.25 and N is equal to 4 say that is it has 4 collectors. So what is the value of $beta_N$ if necessary? You can simply plug in the values in this expression and solve for $beta_N$ and it comes out that of course

it's not a very large value beta$_N$ must be greater than 6. So this gives us the way of finding out the individual conditions for the transistors to operate properly.

This also tells us that one must do a proper design of the I squared L cell in order to ensure that the transistor is working. That is if you just connect the transistors in that fashion, it's not going to work. For example you see that, if you look at this expression I_{SP} must be less than I_{SN}.

Now what is the expression for I_S of the saturation current? I_S in a transistor is given by, if you remember AqD_n n_i squared by N that is the base doping, I will write N_B into W_B. I_{SP} must be less than I_{SN}, so what you have to do is you have to ensure that D_n I_{SP} so D_p by Aq n_i squared they are constants, D_p by N_B W_B of the PNP must be less than D_n times N_B W_B of the NPN. Now D_p and D_n, of course D_p is less than D_n that is the diffusion coefficient of holes is less than that of electrons because of the mobility difference. So basically what we have to do is you have to ensure that this denominator which is, this is the base concentration and in the base width. So this actually means the total base dopants per centimeter square which is sometimes called by the (Not Understandable) number of the base or so. This expression on the left hand side has to be less than that on the right hand side, so this number for the NPN must be less, N_B W_B for NPN must be less than that of N_B W_B for PNP.

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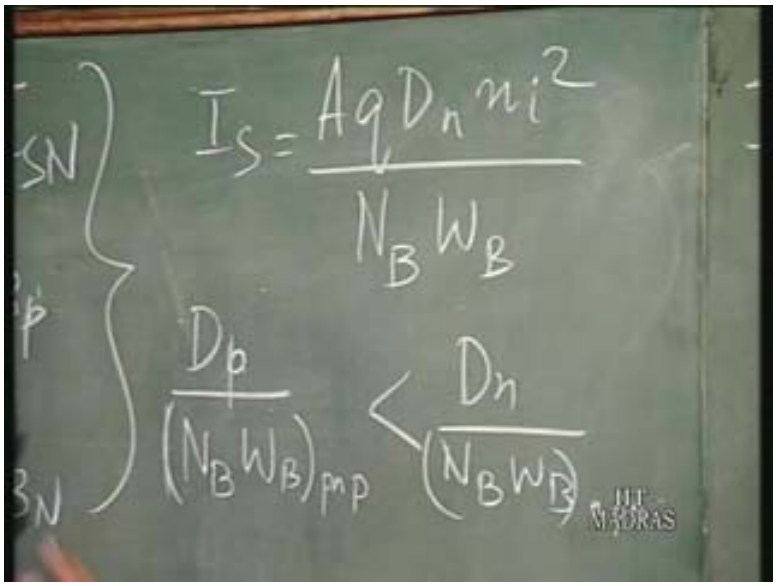

So that this term on the right hand side is much greater than the term on the left hand side. Now if you look back at the I squared L cell configuration, I just draw it again. So these are the different collectors, this is the N_1 N plus wafer so this is P, P, n plus, n plus and so this is the injector, this is the base contact and these are the collector contact.

So the base for the NPN is this region and the base for the PNP is this region (Refer Slide Time: 33:44), base concentration. So the base concentration of the PNP is this N, the substrate concentration and the base concentration for the NPN because your diffusing into the substrate, the base concentration of the NPN obviously going to be higher than that of the PNP. $N_{B.}$ for the NPN obviously it's going to be higher than the PNP because you are diffusing, you are creating that base of the NPN by diffusing into that substrate.

So again if you look back into this condition, for the NPN the doping concentration is higher which means that this term becomes smaller which is going to create problems. So what you have to do is $W_{B.}$ of the NPN must be made much smaller than the $W_{B.}$ of the PNP. That is the base width of the NPN must be made much smaller than the base width of the PNP.

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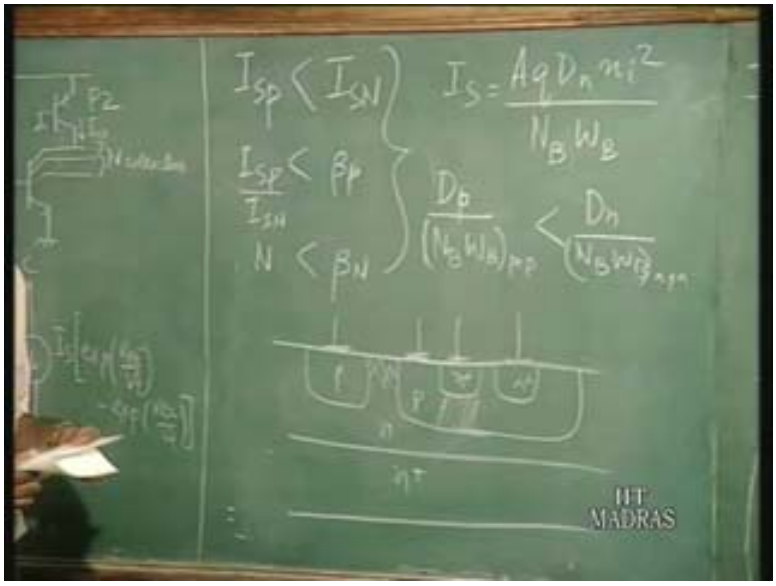

So that this term $N_{B.}$ $W_{B.}$ the product term is much less but at the same time, you cannot make the base width of the PNP very large because again you have a condition, here you see. If you make the base width of the PNP very large, the beta of the transistor is going to fall. Again

you have a condition that this I_{SP} by I_{SN} must be less than $beta_P$ so again $beta_P$ must be also sufficiently large. So you see that there are lot of interdependencies for the different conditions which must be satisfied in order to ensure that the I squared L cell works. So just wanted to give you an idea that one has to really design the cell properly in order to ensure that this cell is going to work. So we just had an idea that one must properly design the cell in order to get proper operation of the I squared L cell. So we shall go ahead with our discussion and the next topic which we shall look at is the different characteristics of the I squared L cell as such that is the noise margin and propagation delays by which you characterize a particular logic family.

Now firstly if you take up the noise margin that is quite obvious, also that the noise margin in a I squared L cell is not going to be too good because of the fact that the voltage levels are constrained to then 0.2 to 0.7 volts at each node because 0.2 volts when the transistor goes to saturation at a node and this voltage cannot exceed 1.7 or slightly more maybe because of the fact that this is a the base voltage of this transistor and it cannot exceed certain value.

So the voltage swings as going to be much low but in the I squared L case, you see that circuit is very peculiar in the sense that there are no resistances in the circuit and so there are no voltage drops across the resistance. It is just the current which is flowing and which is switched either into the base or into the collector of the previous transistor.
So usually the noise margins here are defined in a different way that is instead of defining them in terms of the voltages, here it is defined in terms of current.

That is how much current noise it can with stand and it is very difficult to get exact figures but some simplistic analysis has been done and the whole idea is how to increase the noise margin. So let us take a very simplistic case again, although we know it is not correct that we assume current sources say this is an n collectors and each of them current sources and let us assume that these current sources have the same value. Although we just done in an analysis, we know that these values are not going to be the same but just to have some idea.

Suppose this transistor is off which means that suppose in this base node you have transistors connected here which again have current sources at their base and there maybe m such transistors. So there are n collectors and here let there be M transistors. This is the M transistors at the base. Now when any of these transistors go to saturation, this current source is going to go this way. The current flows into the collector and this transistor turns off. Now suppose you have another current source here which is due to noise, I will call this IN say noise current and this current flows in here. What is going to happen is if this current is small, again most of the current will be flowing into the collectors of the previous transistors but if this current becomes sufficiently large at this node then this base may get sufficient current to turn it on, from the off state.

So what is this value of this current which turns this transistor on? That is defined as the noise margin in this case. So this is the current source and this transistor is off. So what is this value of noise current which turns this transistor on that is defined as the noise margin in this case. So this is very large that means it can sustain a very large noise current and still remain off. So

how do you calculate this value? So if you have N collectors like this, so the total collector current is N I_0. So we shall consider that this transistor to turn on, we have to assume certain base current when we say that this transistor is reasonably turned on. So base current at turn on, says N I_0 by beta. Of course this is $beta_N$ of the NPN transistor. Now at this node if you now write the nodal equation, so what you have is currents flowing in, what you have is IN plus I_0 the currents flowing in equals N I_0 by beta plus here you can have the condition where we can have one transistor on, we can have two transistors on or you can have all M transistor on.

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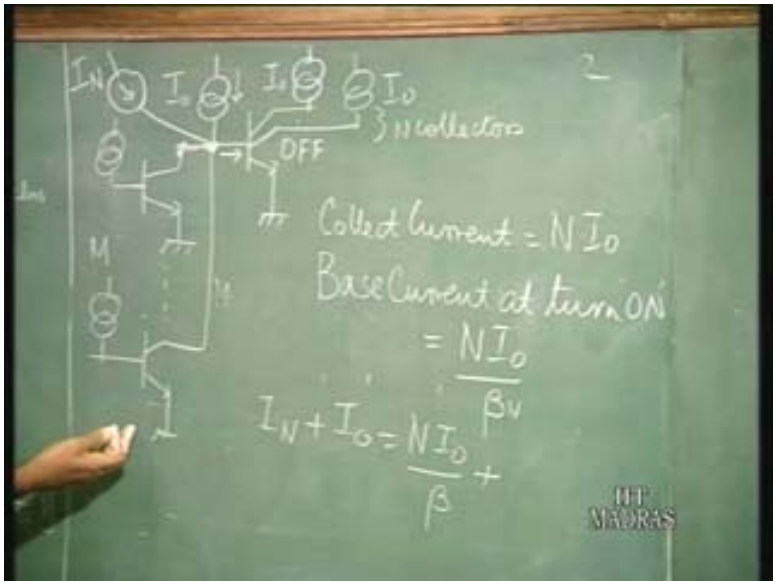

So let us say that M is the number of transistors which is on, I mean M prime or something. So now what is going to happen is if M transistors are on, so this can draw a current of beta times I_0, at the base you have a current of I_0 so these can draw a current of beta times I_0. So M prime $beta_N$ I_0. Actually this is called IN O, that is zero because this transistor is in off condition which is equal to I_0 N by beta plus M $beta_N$ minus one.

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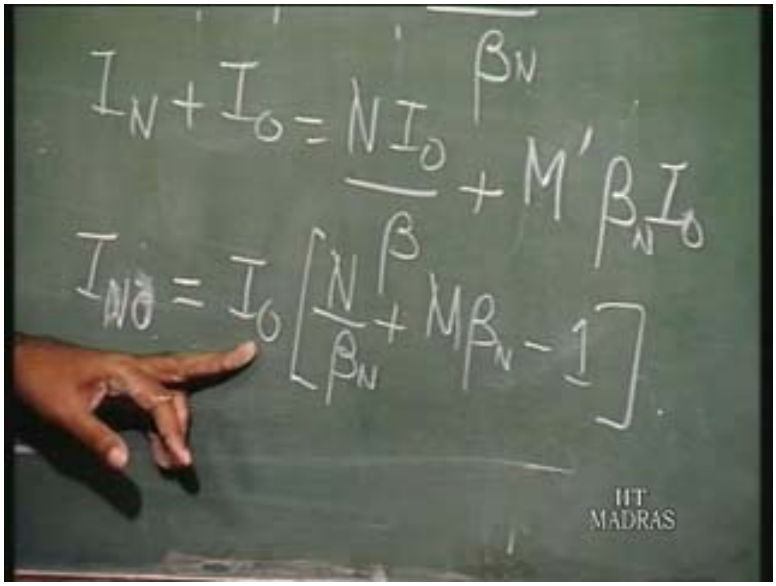

The interesting point here is that we have done this analysis with the lot of assumptions involved and we have taken equal currents but the important point which comes out from here that this is proportional to I_0. The noise current is proportional to I_0. That is if you want to increase the noise margin, we have to increase I_0. So the circuit becomes more immune to noise if you increase I_0. To improve the noise margin one has to have higher injector current, so that is the message from this expression.

Similarly one can do an analysis when this transistor is on. When this transistor is on this current is flowing into the base, when you turn it on it is simpler because it means that all these transistors connected at the base should be off. So again if you do the case for the transistor being on, what do you have to do is the noise current source, it has to be the other direction. It is basically drawing the current and so this has to be turned off. So what is the condition? Here the condition is the base current, again we will assume that this transistor goes out of saturation when you have this condition, when the base current falls to N I_0 by beta_N. So again if you write the nodal equation at that point, so all these transistors are off so they don't contribute to any current. So the current flowing in I_0 is equal to I_N plus N I_0 by beta_N. So we will have I_N equals to I_0 (1-N by beta_N). So again it is proportional to I_0 and the noise margin is going to be larger when of course beta_N is large compared to N and of course this also implies that beta_N must be greater than N in order to this for this to be positive quantity which is also a condition which we got from the previous analysis which we did, the condition for proper operation of the I squared L cell beta_N must be greater than N.

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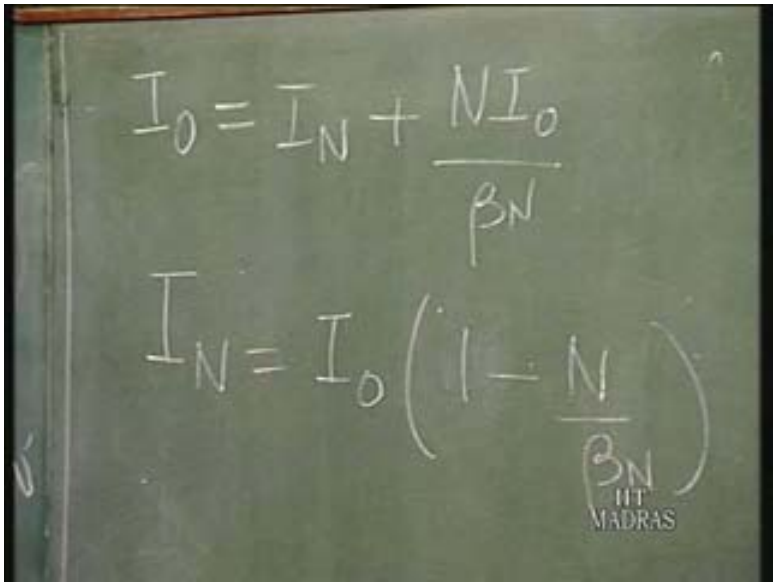

So again the noise margin is proportional to I_0 so to improve noise margin you must increase the injector current for the I squared L cell. That is the current which is flowing in, if we go back to the figure of the I squared L cell, the current which is flowing in here has to be made; if you want to increase noise margin you have to make it as large as possible but of course that is going to add to the power dissipation.

So again there is a trade of between noise margin and power dissipation. So if we increase the current here flowing into the cell that is if you reduce R because this voltage is around 0.7 to 0.8 volts. So if you reduce R you have larger current which would mean that there is going to be a proportional increase of current flowing through the individual injectors. So that is going to improve the noise margin. So we stop here today, the next class we shall take up the propagation delay problem with I squared L cell that is in fact one of the major problems which I squared L ran into after having such an impressive start, we should say because people thought initially that it is very good circuit but it ran into problem because of propagation delay. We will discuss that in the next class.