Digital Integrated Circuits
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Lecture – 13
Edge triggered D-F/F and Decoder realization using I2L

So in the last class we were looking at how given a particular circuit, we can go down to the I squared L layout, we shall continue with that. So last class we had taken up circuit based on NOR gates and it was the well-known half adder circuit where I just draw the circuit again and just go ahead. So this was the circuit. So what we said was when we want to realize it using I squared L circuit, the way to do it is first go down to the transistor level. That is first we have to number these gates and each gate output is represented by a node and the number of transistors or the number of collectors which connected to the node represents the number of inputs to that NOR gate and the number of fan outs for that particular gate is actually reflected in the number of collectors of the subsequent transistor or the next transistor.

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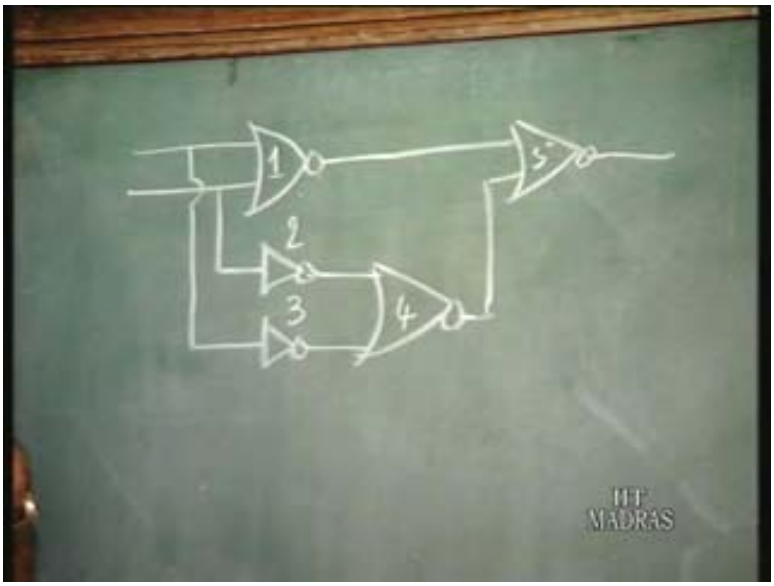

So the transistor level circuit which we had drawn is something like this. These are the two inputs A and B, so join them together. This is gate one, so gate one has inputs A and B. These are the inputs. So this is gate 1 then there is an inverter here, so gate 2. This node has just one collector connected to it that is it's an inverter, so one input. Similarly there is gate 3 which is also an inverter and then gate 4 the inputs are the output of 2 and 3. So these are at the bases of these transistors. The NOR gate configuration you remember is from base to base. So this is the output of gate 4 the NOR gate, the inputs are the output of gates 2 and 3, this is the output 4 and then gate 5 the inputs are from the output of gate 1 and the output of gate 4. So these are

the input points to that gate. So we have one more transistor here and one more transistor here and so when you join the collectors together you get another NOR gate and so this is gate 5.

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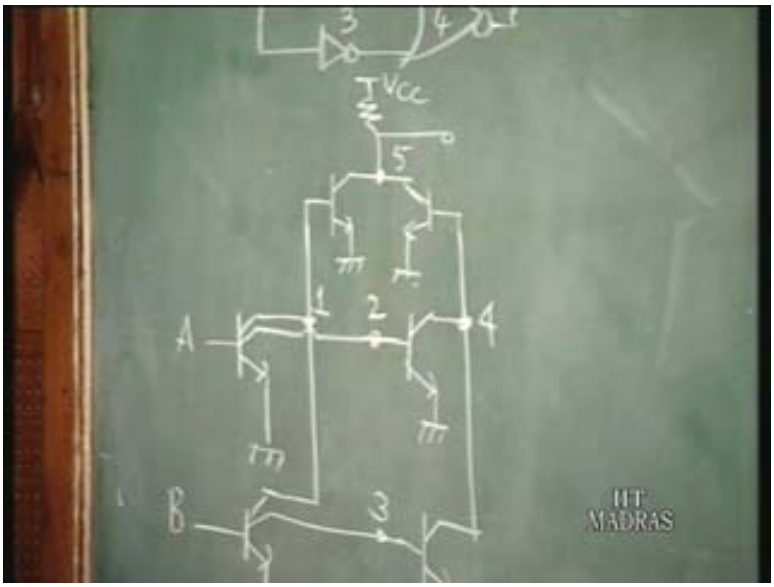

If you want you can take the output, if you want a sort of TTL levels, you can connect a resistance like this V_{cc}, take it out that means this voltage here is going to be either 0.2 volts or 5 volts which corresponds to TTL levels. So what I mean is TTL level is somewhat considered as standard that is from this output you can feed it directly to a TTL gate maybe. So internally as we said the I squared L, the voltage level at each node just changes from 0.2 to 0.7 or 0.8 volts maximum and whereas if you want to take it out for the external connection, you would like to have proper voltage levels and you can do that this way.

Now if you want to realize this, fabricate this; what you require is a layout for someone to fabricate it, the mask lay out. So once you have the mask layout, it can be fabricated because the mask layout gives you the different regions where you want to diffuse differently that is (Not Understandable) diffusion and base diffusion or collector's diffusion, the metal contracts etc. So how do you go to the mask layout? If you recall the layout of an I squared L cell, it is basically the same thing but now you have so many different cells. So you have 6 transistors, so you will have 6 cells. I will just like to say here that in this circuit of course we have not drawn the PNP transistors but it is assumed that at each base you have a PNP transistor. Sometimes we forget to draw it because it is assumed that it is always there that at every base of an NPN you have a PNP because it's not so important in the sense from the circuit point of view because it's only how you connect the NPN's that gives you the circuit. The PNP is always connected in the same fashion.

So coming back to the layout, I think we have started on this in the last class. So this is the injector L and on either side of that you have the transistor. So the first transistor, if you call

this transistor one, I think it's going to be confusing but anyway this is already 1, 2, 3, 4 on the board. So anyway if you consider this to be the first transistor, at the base of which you have the input A. this has two collectors, this particular transistor has two collectors. So collectors are drawn like this the layout then this is the contact for the collectors. So this is one cell, one base to collectors.
Then similarly you have another transistor in which at the base you have input B and again you have two collectors. So I can draw it like this, so these are the two collectors and this is the base input and you have the input B here. Now one of the collectors of these two transistors is shorted, they are shorted to give you the first gate NOR gate and that output goes to the base of another transistor. So what you can do is you can have another transistor like this, the base input is like this and this just one collector for that transistor. This collector transistor is one collector. So these two collectors can be shorted so this is the metal line running and these two collectors are shorted and this goes to the base. So this is the base of one transistor here.

Now again we come to these transistors. So the other collector of these transistors goes to the base of two other transistors. So I can draw them like this and these transistors have just one collector, so one base and one collector and there is one more one base and one collector. So the other collector of this transistor goes to the base here, the other collector goes to the base here. For these transistors again the collectors are shorted and it goes to the base of another transistor. So this transistor also has just one collector, so this collectors could be shorted and going to the base so I draw the base this side and the collector here. So these collectors are shorted and goes to the base here. So we have realized this (Refer Slide Time: 10:15).

Now what is left is these two transistors, the collectors could again be shorted and so basically we have to short this and the output we get is from this point. So this is point is the output. Now for all these transistor this is the common injector. So this requires an injector contact here where you feed the common injector. See in all these transistors, the injector point is common. You have a PNP transistor at each of these bases. This is a PNP transistor, this base is grounded, this is actually a multi collector transistor this way this PNP, so this goes here, one goes here (Refer Slide Time: 11:28). So if you have 6, this is the common point actually where you have feeding the power supply. So this is the common PNP, one emitter so basically you have a PNP, PNP, PNP. The cell consists of a PNP and an NPN. So the NPN is of course going down, so this is the PNP, this is the common injector point.

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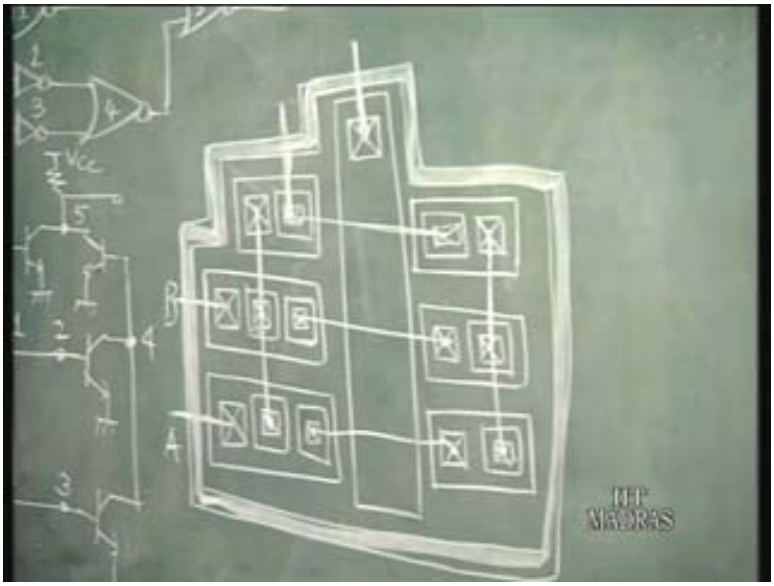

So you require a connection here and of course finally you also require the guard ring which will go around, maybe it goes around like this. So this is the n plus diffusion which access the guard ring and you can have the common guard ring for the entire structure. So these are the two inputs you have, this is actually the sum output and this is the injector input which gives the input current to the system and you have the different regions. So this is the guard ring, I think which goes around all over the play, all around the circuit, I can draw it like this. This is the common injector, diffusion gives the PNP transistors. These are the individual base diffusion for the individual cells in which you have the collector diffusion. So these are all the collector diffusion that run simultaneously and then you have the contacts. So one contact you take from the base collector and this is from the injector so these are the different mask levels.

So you see that the economy, the layout is very striking in the sense that what you have achieved using this is one half adder and you just require 6 transistors and the layout area is going to be very less compared to any other technology. So that is the big advantage of I squared L. So it is very much suited for large scale integration. Is this clear how we go from the gate level circuit to the transistor level is very easy, once you know the rules and from here to the layout. So once you have the layout, you can give it to any process engineer, he can start making the mask and the fabrication and you get the circuit. So this is about a NOR circuit, we shall also look at this as we said, we have already studied that the I squared L can be configured both as a NOR gate as well as the NAND gate.

In the NOR you remember, it's from base to base and for the NAND it is from collector to collector. I think let me remove this. So we shall go on to a NAND circuit, slightly more complicated looking circuit but it's not so complicated. Anyway this is a circuit of positive edge triggered D flip flop, it has 6 NAND gates. So this is the D input and this is here, the clock input is here and then you have one line coming here and here one line coming here then we have the latch at the output.

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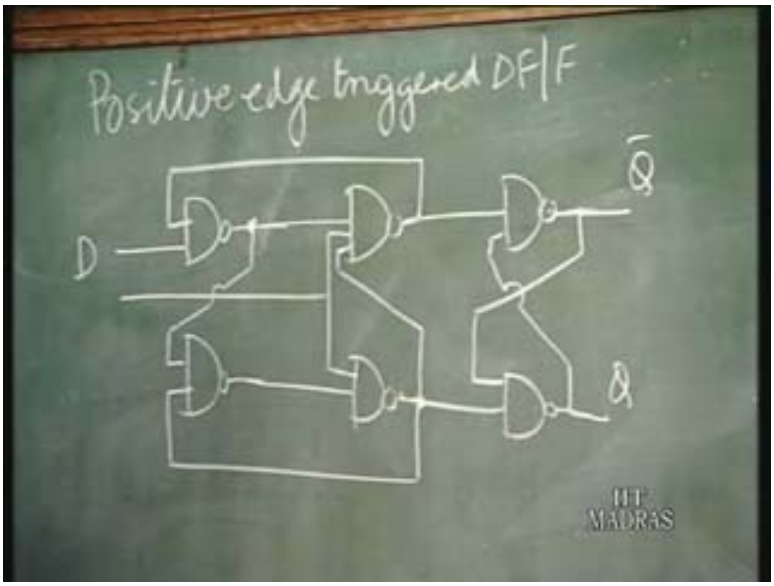

So this is actually Q bar and this is Q. so this is the positive edge trigger D flip flop, I need not go into how it works, you can do that yourself. Basically what we are trying to do is from this given circuit, this is the circuit we can again go back or realize it using I squared L. So again we have to frame the rules for NAND circuit. How to do it? to draw the transistor level circuit. Again we start with the same way, assign a number to each gate, this always helps.

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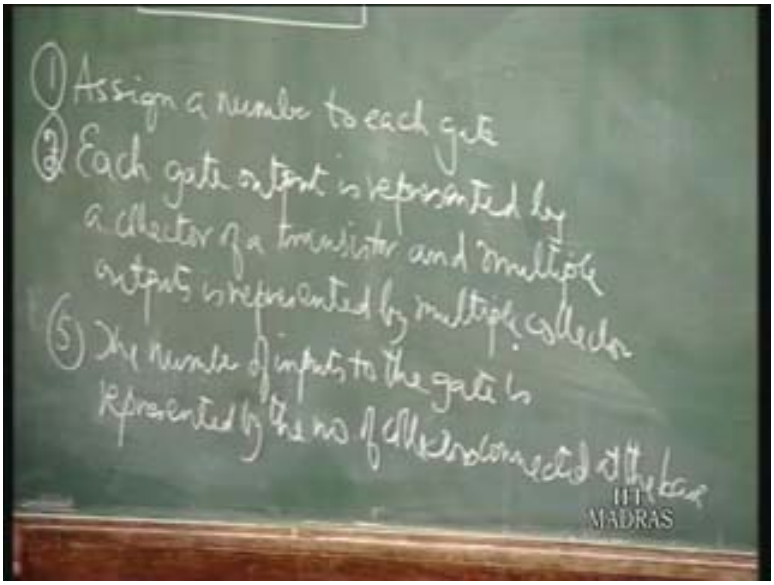

So 1, 2, 3, 4, 5, 6. Now this is the NAND circuit so you remember it's from collector to collector. So each gate output is represented by a collector of a transistor and multiple output is represented by multiple collectors. That is basically if you have two outputs from each gate,

for example one going here so its fan out of two, one going this side, one going that side. So this particular transistor which represent gate 4 must have two collectors. So multiple outputs is represented by multiple collectors and again the number of inputs to the gate is represented by the number of collectors connected at the base. So these are the set of rules which we follow similar to the one for the NOR gate. Now once we do that we can realize this using transistors in the I squared L configuration. So again here I will just draw the transistor first. So you have 6 gates and you have 6 transistors, so 1, 2 these are the numbers 3, 4, 5, 6. Gate number one has the fan out of two, so this is going to have two collectors. Draw it straight away. 2 has just 1 connection, so it is just 1 collector, 4 has 2 fan out of 2 so it is 2 collectors. 3 has fan out of 3 so 3 collectors, 6 is fan out of, if you take one out it is 2 and 5 is fan out of 2. Now you make the connections.

So one is coming here, so this is the D input, from here you have one connection to this point, from the output of one, one input goes to the input of 2 and the other output of one goes to the base of four as input to the gate 4. Then 2 goes to the base of 3 and from the output of 3, there are 3 output, 1 is going to the input of 6. By drawing I take it from this collector then one goes to the base of two here and another one goes to the base of 4 here and from 4, one of them is gone there, one goes to 5. From 5 one of the collector goes to the base of 6, from 6 one of the collectors goes to the base of 5. So these are the remaining collectors and then you have the clock.
So I have one going to the base of four and the other going to the base of 3. You must remember here that in I squared L, in the NAND configuration, each of these inputs is actually the collector of a transistor. It is coming from the collector of a transistor and then it is very important to note that you cannot have, although if you look at the circuit here we have drawn one clock input like this and one goes to 4 and one goes to 3. Here I have drawn two clock inputs, I did not draw one clock line going here and here because they must be separate. They are two collectors of one transistor from a multiple collector transistor. If I had just shorted this, I would have shorted say the input of 3 and input of 4 which is not allowed. So again you must remember why we use multiple collectors transistors in I squared L. So these clock inputs must be separate and they must come from the two collectors of some transistor where you are generating the clock. So you cannot have one clock point going to all of them because you will be shorting all these lines in that case. So in this case you must have two clock inputs going to two bases and now you can just check or verify with the rules, going back to the circuit.

So if you take each gate, gate one it has two collectors and at the base there are two points, two nodes, at the nodes you have two inputs. So if you look at gate one, there are fan out of 2 and it's a two input NAND gate. Similarly if you go to gate 4, it is 3 inputs and a fan out of 2. So at this node you have three inputs and two collectors, similarly for all of them so get 3, it has 3 collectors and there are just 2 inputs. So the two input NAND gate with the fan out of 3, so you look here it is gate 3, it's a two input NAND gate with the fan out of 3.

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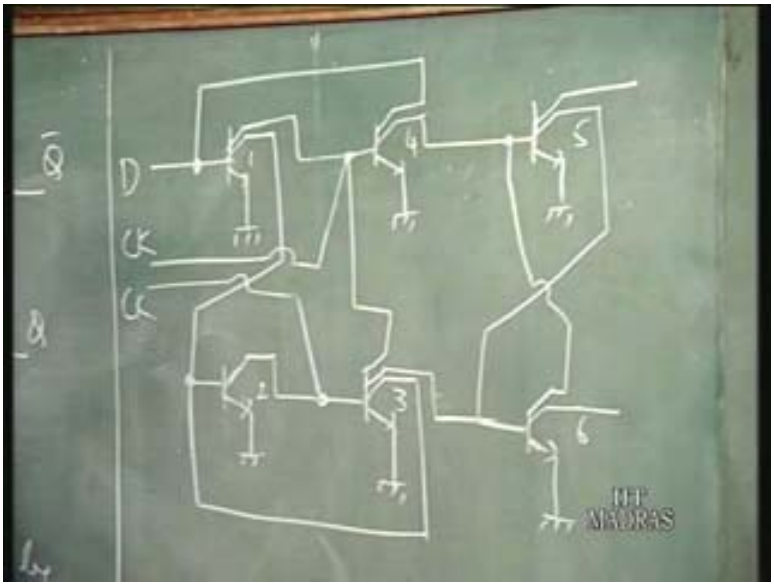

So you can verify, it's very important to verify. So it must satisfy the rules which we have laid down. Once you do that the next step is of course layout and I think I don't want to waste time here doing the layout, you can try it out yourself. So with an injector you can have again as we did for the NOR gate, once you have the transistor level circuit it is very similar. You have to draw the individual transistors and make the connections. So I leave it to you as an exercise. I think you should be able to do it. So we have seen how you do the layout for NOR case as well as the NAND case.

I will just give one more example of another circuit, an interesting circuit which is realized very easily using I squared L.

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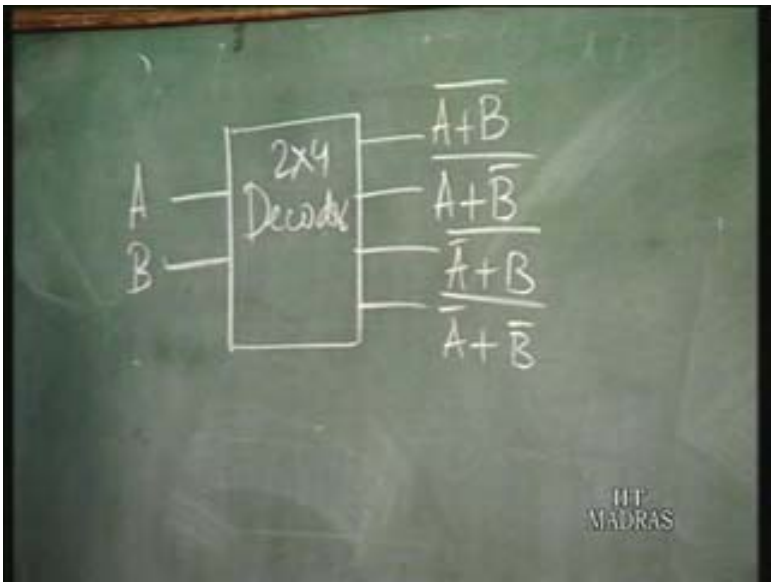

So in the circuit I was talking of a decoder, I think you know what is the decoder say very simple. The 2 into 4 decoder, it has 2 input and 4 outputs and you know that if there are n inputs you will have 2 to the power n outputs. So suppose I call this inputs A B, the outputs here are, you can write them as NOR gates, A plus B bar, so all the 4 possible combinations and this is very easily realized in I squared L. So I will just draw the transistor level circuit, you have the two inputs A and B, so you have to realize the compliments also. So here you have A bar, here you have B bar and now if you want to realize all those combinations, if you take this and join them here you have the NOR of A and B.

If you take the collector of this and this and join them together, so here you have A and B bar, here you have A bar and B bar in the NOR of these two. If you want to realize the other two, you have to take one more collector here, so this is going to give you the NOR of A and B bar if you want, you have to draw this together here. If you want the NOR of B and A bar, you have to take the collector of this and this and join them together. So you see that basically you require 4 transistors and you can just join the collectors and you can get a 2 into 4 decoder. If you have a 3 into 8 decoder, you basically require six transistors A B C, you just generate A bar, B bar, C bar 3 mode 6 transistors and you have to just tie the collectors together properly.

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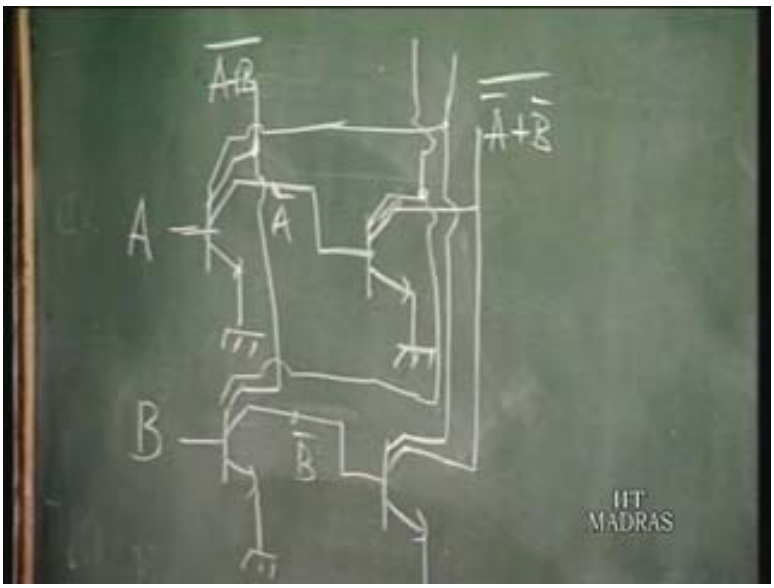

If you require a 4 into 16 decoder, you just require 8 transistors. So you see that it's very economical I mean you require a very few transistors compared to any other way of realizing. So this is another way and the layout usually one way to do it is specially for the decoder, you require 4 transistor. So how you do it is you have the 4 transistors like this, the injectors usually run this way these are the injectors in between.

Now these transistors suppose you have the A input here and the B input here, this is the base of this transistor and you have one of the collectors. So this collector here of this, so if you have A you have B, this goes as base input here to this transistor and again one of the collectors here goes in as base input here (Refer Slide Time: 31:20). So that is what we are doing, one of the collectors goes in as base input to the other transistor. So for this transistor one of the collectors goes as base input here. So this transistor has an input A, so it goes here. This transistor as an input B, one of the collectors goes as base input there. So this transistor has a base input A, one of the collectors goes as base input to this transistor, this transistor B (Refer Slide Time: 31:50).
Now what you do is so one collector here A, this is one collector. So this transistor one collector and this transistor one collector and just short them, you get the NOR of A and B.

Now this collector of this transistor and one collector of this transistor, if you short that you get the NOR of A bar and B bar. Now if you take one from here collector and this is A and say B bar and this is a metal line running all over shorting this and this, you get A plus B bar. The other one you take one from here this one collector and from here so you get the NOR of A bar and B.
So you have all the four combinations. These are the injectors, this is the one injector here, one injector contact here, one injector contact here, you can short all of them together and this in the injector. So basically what we have done is these are the injectors, the injector that is of the PNP transistor, so this is the PNP, PNP, PNP. So the injectors are injecting holes into the base of the NPN transistors.

So they are positioned in between the two transistors. This is done in case the number of collectors you know of the NPN becomes quite large then it is necessary to have this type of structure because if you have the other type of structure, this type of structure you know this is the injector and you have this type of structure and suppose this is the base contact and you have number of collectors. So we shall come to that in more detail later on. So for this collector this injector is very far away. So it results that in a lot of series resistance comes into play and that is going to hamper the operation of the device.

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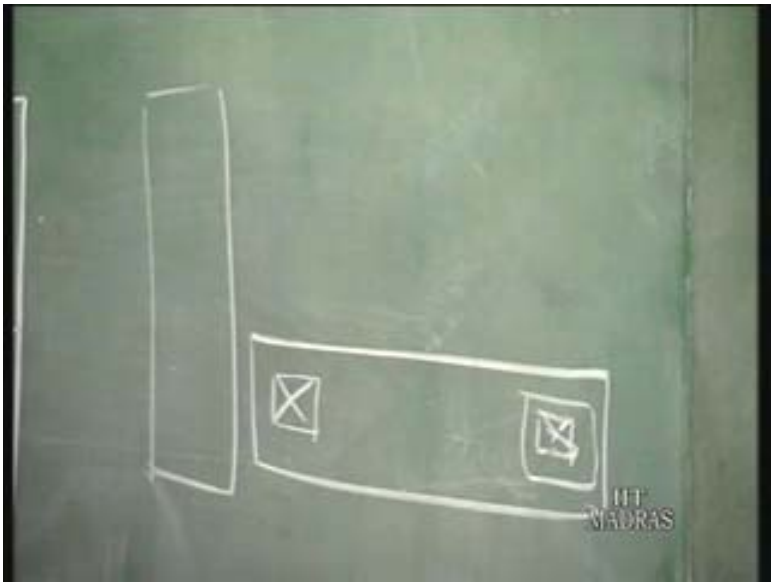

So if there are too many collectors, it is better to have this type of design where the injector is facing. So each of these collectors is actually not very far away from the injector that is the injector rail is parallel to the base diffusion. Of course for 2 into 4 decoder you might as well have this design but why I drew this is because if you go for three into eight or four into 16 it's very simple, you just have the same type of layout.

If its 3 into 8, you will have two more of this, the C input and again you will have instead of 4 lines running like this, you will have 8 lines running and you just have to place the collectors in the proper position. You make the layout in such a way that you have the collectors in the proper position and you can connect them by metal lines running straight like this. So you can have 3 into 8, 4 into 16 so 4 into 16 means you will have just 8 transistors like this and in between you have 7 injector rails and you short them injector rails with the common contact and you have the outputs running like this, straight lines where you short the corresponding collectors. So it is a very beautiful design.

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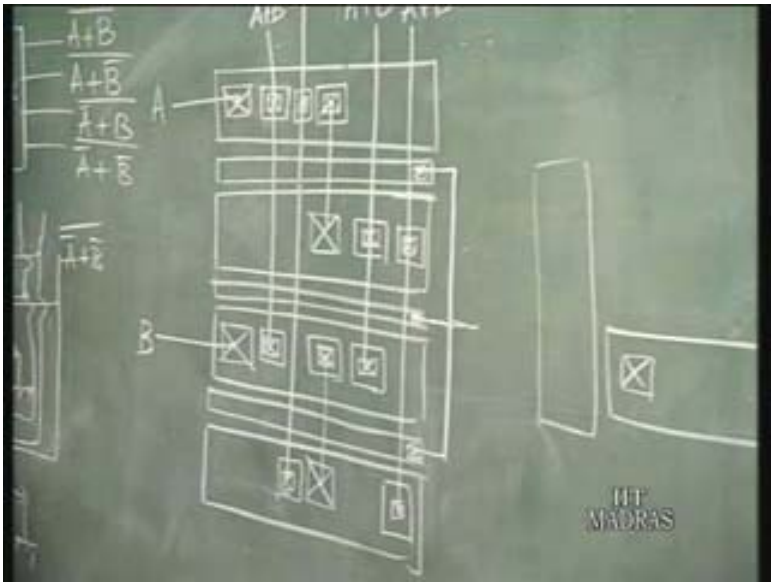

So this is how you can design I squared L decoder and it is very convenient. So this is about the layout, so we have seen how given a circuit you can go to the transistor level circuit for the I squared L and then do the layout. For a designer the layout is the final output which can be passed on to the process engineer to actually fabricate it. So we come to this section now of the discussion on I squared L and the next issue which will be looking at I squared L is some other points.

The next issue which will be looking at is you have seen how you can realize the circuit but again another important point remains to be addressed is that given a circuit, I shall again draw the I squared L cell. Given the circuit, more for a process point of view, how do you ensure that the circuit is going to work? That is from a process design as point of view, we have to ensure that this NPN transistor actually goes to saturation that is very important in I squared L because the voltage levels are such that this has to go down to 0.2 volts otherwise you cannot switch off the next transistor. So this has to go to saturation. So how do you ensure that this transistor goes to saturation? Of course this is going to some base, so you have another PNP here.

All the collectors will have some PNP at the base. Now if this input is high or you have a cut off transistor basically here then what happens is the collector current of the PNP goes in a base current and this transistor and this base current must be sufficient to drive this transistor to saturation. Now if you assume very simplistically let us say that all this current sources are same. This is I_0, this is I_0, this is I_0. Now the condition for saturation is that beta I_B must be greater than I_C, whatever is IC. If this condition is satisfied then the transistor goes to saturation. Now in this case the total I_C is equal to n times I_0. So if you assume that each of them is I_0 and the base current is again I_0, so beta I_0 must be greater than n times I_0. That is beta must be greater than n.
So beta of the NPN transistor, if it is greater than n that is the number of collectors then the transistor goes to saturation, but this is very simplistic because of the fact that when this

transistor goes to saturation, the base voltage is around 0.7 volts or so. So this is high. So what is the condition of this PNP transistor?
So the base voltage is high, base emitter drop is high as well as the collector to base voltage. This transistor is in saturation, in fact deep in saturation. So when a transistor goes to saturation, the effective beta of that transistor is quite low. So this is not behaving as a good current source that is the collector current will not be the same as the emitter current for this one. Whereas for these transistors since this voltage is low, so this is going to have larger current. So basically the base current is depleted because this transistor is in saturation whereas this current is high because this transistor is in the active region, collector base is around 0.2 volts whereas base emitter maybe 0.7 or 0.8 volts which means V_{CE} is sufficiently large and you have the transistors in the active region.

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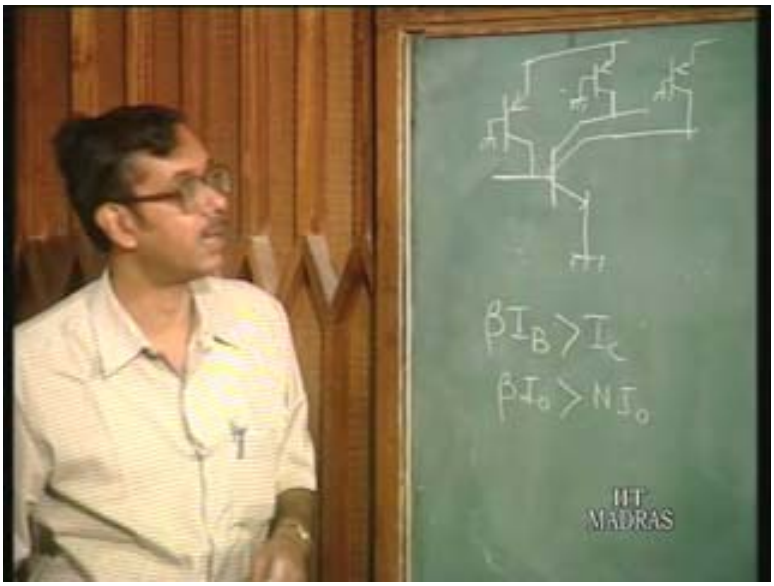

So these I_0's are obviously not equal. So we have to find out a condition for this circuit to work that is conditions for the transistor to go to saturation, in terms of the transistor device parameters. So that is what we are going to take up next. So that gives us an input into the design of the transistor. I suppose you understood the problem, now we have to look at the solution. For that what you are going to do is the transistor equivalent circuit which we are going to use is again the Ebers-Moll circuit model which you are familiar, so I will just draw that model. So you have 3 current sources, so this is the base point, this is the collector point, this is the emitter point.

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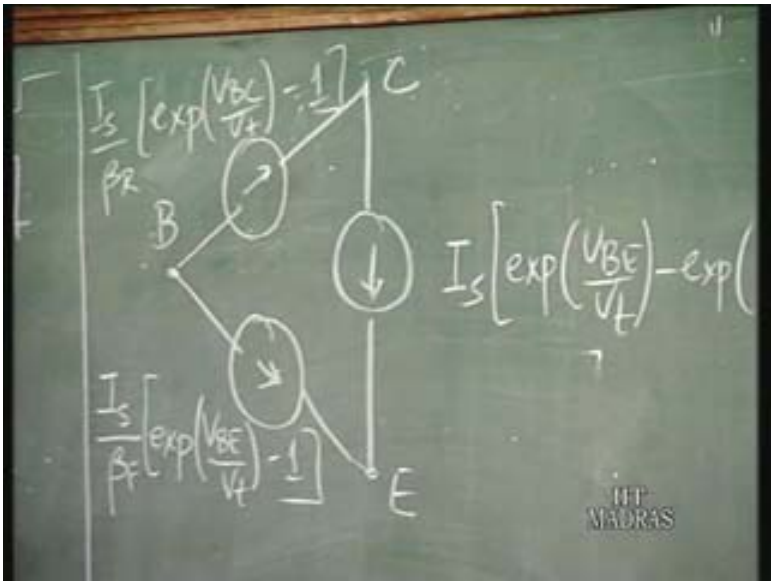

So what is this current source equal to? It is I_S exponential V_{BE} by V_t minus exponential V_{BC} by V_t. This one is I_S by beta$_F$ exponential V_{BE} by V_t minus one and this one is I_S by beta$_R$ exponential V_{BC} by V_t minus one. So this is the Ebers-Moll model which we have already derived in the first three classes. So you are familiar with so we can take it up straight away. Now again going back to the condition for saturation of the I squared L cell of the NPN transistor in the I squared L cell in terms of this parameters. Again the condition for saturation is beta I_B must be greater than I_C. In that I squared L cell it is a bit confusing because this is the multi collector transistor. Then what is the value I_S or whatever we are going to take for this. What we will assume is that a multi collector transistor is basically consisting of n collectors, it usually consists of n transistors in parallel. That is the base emitters are parallel. There are n transistors, the base emitters are in parallel and you have separate collectors. So there are n individual transistors and each transistors you have an I_S that is saturation current or beta etc.

So for these transistors what you have is beta$_F$, so you have an I_B. What is I_B equal to? There are n transistors, this I_B is given by I_S by beta$_F$ exponential V_B by V_t minus one and V_{BE} of course you have another term V_{BC} by V_t. Now we shall assume that V_{BC} because this is exponential term. Even when V_C is 0.2, suppose V_B is 0.7 and V_{BC} is 0.5 because they are exponential terms, exponential 0.7 by V_t is going to be much greater than exponential 0.5. So we shall assume that this is mostly given by this V_{BE} term. So we can write n times I_S by beta$_F$ exponential V_{BE} by V_t. Again we neglect minus one which is much smaller than that, is greater than I_C which is again n times, I will write I_0 let us assume that this current is I_0 we will see

what is I_0. So this becomes equal to I_S exponential V_B by V_t is greater than I_0 so this is the condition of saturation for the NPN transistor. Just to differentiate between NPN and PNP, I will just call this I_{SN} which indicates that this is a for the NPN transistor. I_S for the NPN transistor, I_{SN} exponential V_{BE} by V_t for the NPN transistor must be greater than I_0.

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So we have to now look at what does the values of I_0 etc and come up with the condition for actual saturation of this transistor. So it will be in terms of saturation currents and the betas of the individual transistors the NPN, PNP etc and the process engineer or the designer who is designing this must ensure that these conditions are satisfied that is the betas of the transistors and the saturation can IS values of these transistors and only then the I squared L is going to function normally. Otherwise it is not going to operate so that is very important for the working of the cell. We shall take the topic in the next class.