Digital Integrated Circuits
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Lecture – 12
I2L Technology Half adder Realization

In today's class we shall continue our discussion on I squared L and just to recollect what we were doing last class. We have drawn the basic structure of an I squared L cell which consists of PNP and NPN transistor. The NPN transistor is of course a multi collector transistor and here you have the PNP which acts as a current source. So you have the supply voltage here and this is the resistance. So this is so called injector point from which current is injected into the circuit and you have a PNP which acts the current source and this current which flows in the collector of the PNP transistor either flows into the base of this NPN transistor, turning it on or making it go to saturation or if this input is low, this is going to flow out into the input point. So this is the input point and in which case this particular transistor is going to be cut off so this transistor is either in saturation or in cut off.

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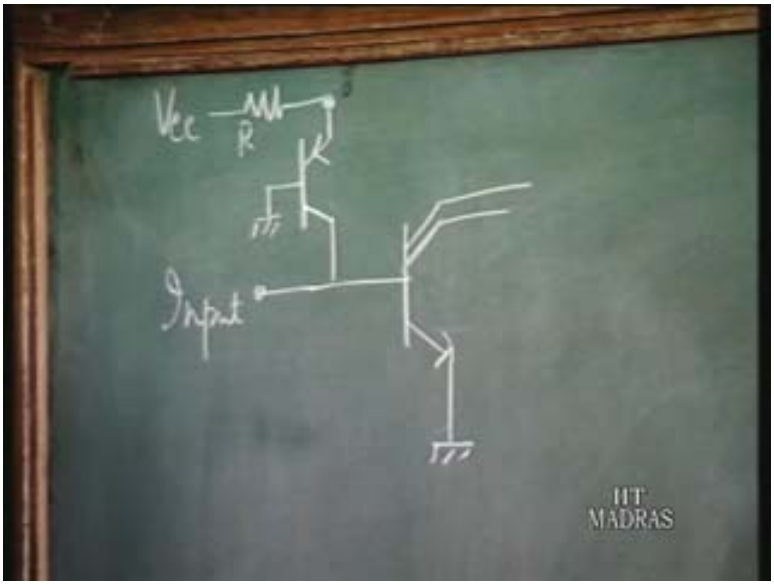

So this is the saturated logic, the transistor goes to saturation. We had also drawn the cross section view of this particular cell. So you have the structure which we have drawn is like this. We have an n plus substrate, you have the n plus guard ring. In today's class we shall discuss in detail about this particular structure. So you have the injector then the base and you have the collectors. This is also P so this is the injector terminal, this is the base or input terminal and these are the collected terminal and the ground is at the bottom. So these are the injected terminal, this is the input or the base terminal and you have the collected terminal in this case 2

but you can have more than 2 collector terminals. It is possible to have more than 2 also. This is what we did in the last class, we shall go ahead with our discussion.
Today's class we shall study little bit about the technology aspects of I squared L that is how this is realized because this is very important especially in the case of I squared L because most of the advantages of I squared L as you see it, you discussed the merge transistor structure. As well as most of the drawbacks or problems associated with I squared L is associated with this particular structure because the transistors have been merged, we have a particular structure.

So one really has to understand why we have this structure, how we realize this structure and what is the problem associated with this structure? Because you have already seen that this transistor structure which we have bipolar transistor, NPN structure is different from the conventional BJT structure where you have the emitter on top and collector on the bottom. Here the collector is on top and emitter is in bottom. Also this gives rise to certain problem. So we shall see the step by step, how this is fabricated and some associated points about this. So first what we do is in order to fabricate this I squared L cell, you start off with n on n plus substrate. Of course this is not to scale, usually this n plus substrate consists of entire I mean this is very thick, I have just drawn it because of convenience. I have to draw lot of things in this n region.

This n region maybe about 5 microns thick whereas this maybe depends on the wafer which we are using maybe 300 or 500 microns thick. So this is mostly n plus, this n region is grown epitaxially on top of the n plus region. A few about 5 microns maybe. Why do you require n on n plus for this fabrication, why not a total n plus structure? Because if you go back to this structure here, so this is the n epitaxial region you have to diffuse and make all these junctions. Now if you have to make a junction by diffusing P regions so in this region the P concentration that is the accepter ion concentration must be greater than the background donor concentration which means that the donor concentration must be low. Otherwise you can never make a junction. So it is necessary that you have n on n plus wafer. Why an n plus at all, why not a total n region? Because this n plus actually acting as the emitter of the NPN transistor so you require high concentration.

So you require n plus but you cannot make a totally n plus up to the junction because you have to actually fabricate this PN junctions which is done by diffusing from the top and so you require a lightly doped region in which you actually fabricate or diffuse this P regions. So you have to start with the n on n plus wafer. So that is what is the starting point. Then what you do first is you make the guard rings, you diffuse the guard rings that is these are n plus regions, just something like an isolation in a normal BJT process. I also draw the mask drawing that is from the top view,
So if you look at the wafer from the top so this is the region in which you diffuse this n plus. Its ring like this, this is from the top view, this is the cross sectional view. So you have an n plus ring, tub sort of thing in which you fabricate this. Now why is this n plus guard ring necessary? Again I come back to this figure, it is necessary because of few reasons for example you see the NPN transistor. If you look at the NPN transistor this is the base of the NPN transistor and n region is the emitter.

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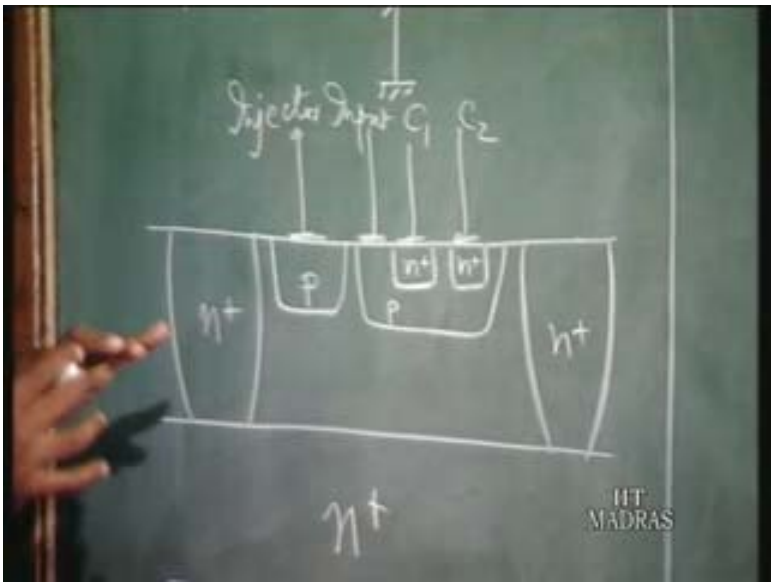

Now the base current of the NPN transistor depends on how much hole is injected from the base to the emitter and that depends on the emitter concentration. When there is minority carrier stored in the emitter region they recombine, minority carrier in the emitter means holes. The holes when they recombine, to compensate for that holes are injected from the base to the emitter. So if there is more minority carrier stored in the emitter, in this case lightly doped emitter, you have more hole current injected that is more base current which is going to reduce the beta of the transistor. So you have to reduce the minority carrier stored in the emitter that you can do by increasing the doping concentration on the emitter side because if the emitter doping concentration is increased, you know the minority carrier is proportional to NI squared by NP. So that is reduced. so basically by making this n plus, you are reducing the holes injected in to this side of the emitter because you are reducing the minority carrier concentration here.

So basically it is for this reason you would like to have a guard ring because any unnecessary n region left, here there is going to be some unnecessary stored charts which is going to create problems. Why guard ring this side also? Because again if you look at this PNP transistor, the useful holes are those which are injected from the emitter towards the collector. We do not want holes injected this side because they are not going to be of any use. So again to reduce this injection of holes on the other side, you can make an n plus which means that the hole concentration here is suppressed because of if you have an n plus here, n plus means highly

doped n region, large concentration of donors so the hole concentration is going to be proportional to n I squared by n d.

That is already we have seen so basically you suppress the hole injection on this side which is going to be a waste actually. You make a guard ring, so all the activity is confined to this region and there is no injection of charges on these side which is actually going to be a waste and it's going to be a waste and reduce the performance of this circuit. So you have a guard ring like this. So you first make the guard ring and then you do the P diffusion to make the PN junctions.
Actually you should make it as d plus possible so that this n region which is actually the lightly doped region is as small as possible. The thickness of this n region is going to be as small as possible because this n region whatever is the thickness, you have lot of minority carriers stored charge here. Again from the same principle, if you have a lot of minority carrier stored charge here there will be more hole injection from the base to the emitter which is going to reduce the beta of the transistors. In a PN junction, say if you have a P plus n junction, it is mostly holes injected from P plus to the n because n is lightly doped and so the minority carrier concentration is more. Whereas if P plus there is going to be very little electron injected from n to P because that is highly doped, minority carrier concentration is less.

Similarly here, if you reduce this n region, you actually reduce the hole injected because in the n plus region there is going to be very little hole concentration. So if you reduce this n region, there is going to be less injection of holes into the emitter which is the base current and the electrons injected from the emitter to the base is going to dominate. So this must be made as thin as possible. This is the cross sectional view, in the top view the mask is going to be something like this and this is the base, so this corresponds to this region and this is the injector. In fact sometimes a second P diffusion is done on the injector side just to increase the acceptor ion concentration here because this is going to act as the emitter of the PNP transistor. So this should have a higher concentration compared to this but we can also avoid it but this is going to act as the base, you cannot make it very high concentration.

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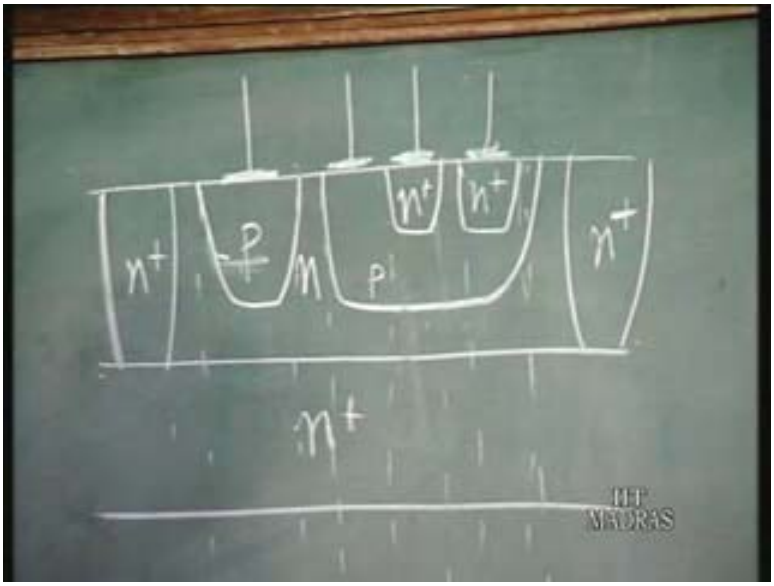

This is the P region and then the next step is you diffuse the collectors in the P region, so these are n plus. This is the mask through which you diffuse the n, this corresponds to these regions and these are P P (Refer Slide Time: 14:48). Finally what you do is you take the contacts. You take a contact from here, here and so on. So you draw it like this which is the convention for drawing the mask layer, this is the hashed region, you have a contact here and so on. So this is the I squared L cell, this is the mask drawing.

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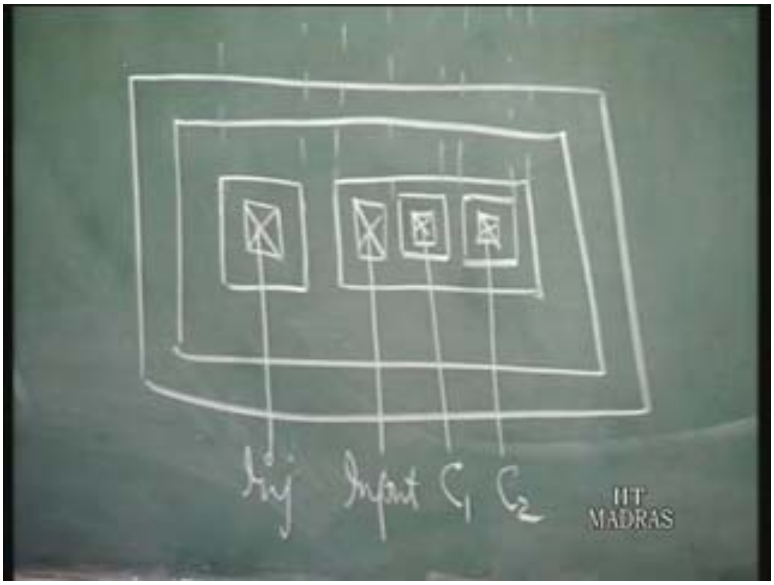

So you have an injector here, this is the injector, this is the input or the base it's also sometimes called the base contact, it's the collector C one, C two, this is the two collectors here (Refer Slide Time: 15:25). So this is the mask drawing or the top view and this is the

cross sectional view. So this is how you fabricate the I squared L cell. This is very important because we shall be coming back to this again mask drawing, we shall look at mask drawings for more complicated circuits.
So this is how it looks like from the top. Now with that we move on to more general circuits that is we have now seen an I squared L cell that is the NPN, NPNP combination here that is the I squared L cell.

Now of course our interest would be to see how you can make for example NOR gates and NAND gates because that is going to act as the basic structure around which you make more complicated circuits. So that is the next step. You shall see now that when I am drawing more complicated circuits, I am actually repeating the I squared L cell. Basic cell is being repeated many number of times. So these are two cells, I joined them here, another cell I draw here and I connect all the injected points together and short them. Then you can have a connection to $V_{cc.}$ through a resistance. So usually as I said this resistance which you have here is usually external to the chip, you don't require a resistance inside. So if this is an I squared L circuit, you don't require a resistance as such. So if this point is made available, you can connect $V_{cc.}$ through a resistance.

So that is one advantage of I squared L, you don't required any passive components and also this structure is the merge structure, so require very little area. So as I said that I squared L is more suitable for large scale integration amongst the different bipolar logic families. Now suppose I have the inputs A and B here for this circuit and the output say this point is F. So A and B are the inputs and output is F here, I call this $F_{1.}$. Now what is the logic that you achieve here? So if you draw the truth table A B, $F_{1.}$ say 0 0, 0 1, 1 0, 1 1 these are the 4 combinations. Now when A and B a 0 0 that is these 2 points are low, in I squared L when we say this points are low that means basically you have a saturated transistor connected here that is the output is low.

Now what is going to happen, what is the state of these transistors? They are both going to be cut off because these inputs are low. So these transistors are cut off, when this transistors are cut off what happens to this current in this current source here? It flows into this base of this next transistor, this voltage here is going to be around 0.7 volts and this output is going to be high. So that is hear we refer to high as the base emitter drop of a transistor that is around 0.7 volts and low will be around 0.2 volts which is the voltage when a particular transistor is saturated. So that is the range 0.2 to 0.7, the voltage at all nodes lie within that range in this circuits. So when it is 0 0, it is 1. When one of them is 0 and the other is 1 what happens?

Suppose this is 0 here, A is 0, B is 1 this transistor is cut off. What happens to this transistor? One means here there is a cut off transistor which is cut off, so this current source, the current from this transistor flows into the base. This transistor goes to saturation and when this transistor goes to saturation this voltage here is pulled low. Because this current source, this current will flow into the collector of this transistor and here this transistor is not going to get any current. So this point is going to go low, this transistor goes to saturation. Similarly 1 0 also you have the same case and when it is 1 1 both the transistors are conducting. The same

situation where this point goes to low because this voltage here is going to become low because both these transistors are in saturation so the output is going to be low. So what is the logic here? NOR, so this is the NOR function. So F is equal to NOR function of A and B.

Now let us look at it in a different way. Suppose I have another circuit here say another transistor here, another cell basically and suppose I look at the logic values at these points. Suppose I call this X, I call this Y and suppose I call this F_2 that is X is the value at the collector of this transistor and Y is at the collector of this transistor and F_2. That is if this transistor is in saturation, we shall say X is low and if this transistor is cut off we say X is high.

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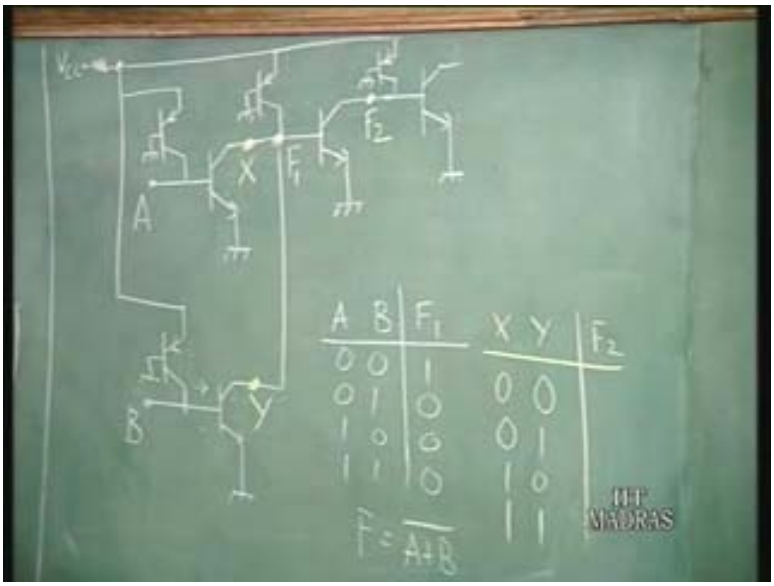

Of course you must be a little bit worry about this, actually you see these 2 points are shorted here. So how can one be high and one be low? The definition here is more strictly in the sense that here when we say high and low, it refers to the state of this transistor. That is if this transistor is cut off we say X is high, if this transistor is in saturation we say X is low. So if you define it that way and we write another truth table, so what is the logic here? Again F_2 is high if this transistor is cut off and low if this transistor is in saturation. Then if 0 0 means both the transistors are in saturation, so this current flows here, so this transistors is cut off so this is 1.

Now if one of them is zero and the other is one that is one of them in saturation and the other in cut off. Saturation means the current is going to flow this way, this output transistor here is going to be cut off. So what is the output going to be? When both of them are cut off then only this current flows into the base here and when it flows into the base, this transistor goes to saturation and the output is low (Refer Slide Time: 25:16). What is the logic here? It is NAND. So you see that with this particular circuit basically what we have done is you have

taken some I squared L cells and we have just wired the outputs that is the collectors of this and we have achieved some logic. You can achieve either NOR logic or NAND logic. For NOR logic the inputs are considered at the base of a transistor and the outputs are also at the base of the next transistor.

Whether the input base voltage is high or low that is what we are considering. From base to base it is NOR logic. If we are considering whether the base voltage is high or low at the base of a transistor and if you consider at the collectors that is whether the transistor is in saturation or cut off then it gives a NAND logic. From collectors to the next collector, it is a NAND logic. So you can consider it in both ways. the idea is that basically what you have to do is in order to obtain I mean you have to realize the circuit, you have given a circuit which is drawn using NAND gates or you should be able to go to this circuit, you should be able to draw the transistor circuit. We shall come to that subsequently that is given a NAND circuit that is circuit drawn using NAND gates, you should be able to draw this transistors level circuit for I squared L and once of course you have this circuit, you can go back to the layout and you can do the design. Even if you have a NOR circuit you can do the same process. Go to the transistor level and from there you know how the cells would look like from cross section and then you can go to the layout. So that is what we shall do subsequently.

Again just to repeat from base to base it is NOR from collector to collector it is NAND. Before we go ahead and do that that is just from a NOR level to or NOR circuit and NAND circuit to the transistor level, how you obtain that, just one point I would like to make is that we have been talking of these multi collector transistors. This NPN transistors having multiple collectors. Now why do you require multiple collectors, is it necessary? So the question is suppose you want to obtain a NOR of, this F is equal to, you want to realize these functions. That is NOR of A and B and NOR of A and C. Now how do you do that? You have again A B the two inputs, just sort them. Of course it is going to the base from other cell. I have not drawn the PNP, I am just drawing the current sources here.

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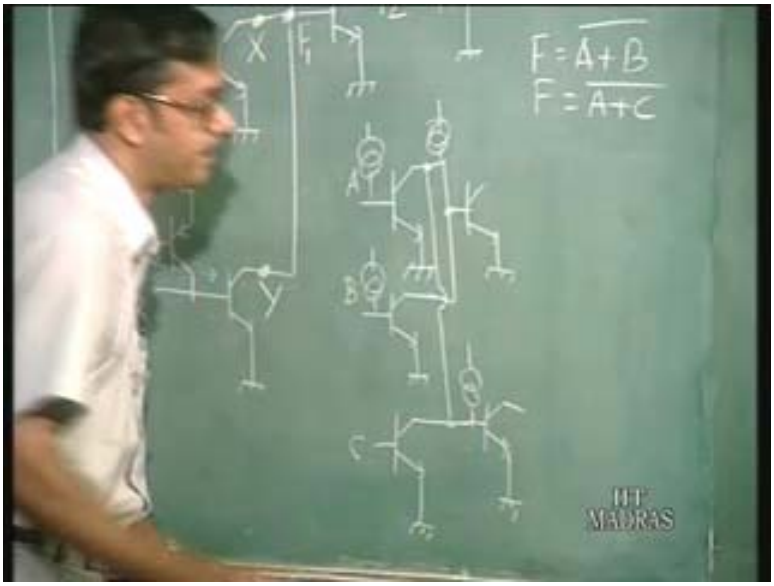

So here you will get NOR of A and B. now if you want to have a NOR of A and C, what do you do? You have a C input, suppose you want to do it like this, if you don't have multiple collectors you take this point itself, connect it here. Now do you have a NOR of A and B, its C here that is the question. What you have here? Because at this point you have shorted A, B and C. So basically what you get at this point is NOR of A, B and C, not A and C because basically at this node the outputs of all the three collectors are shorted. So here also you get NOR of A B and C instead of just A and C. That is the problem, you have basically shorted all the 3 collectors.

So you have a three input NOR gate. So what you have to do is you have to have a multiple collector like this and coming here like this. So in that case here you have shorted the collector of these two transistors, at the inputs you have A and B so this is NOR of A and B so here at this point you have just shorted these two. At the inputs you have A and C so this is going to be NOR of A and C (Refer Slide Time: 10:56). So using multiple collectors I mean if you want to have logic functions may derive using the same inputs, you just require multiple collectors. So that is also an advantage of I square L using multiple collectors it improves your functionality in the sense that you can have more logic functions derived using less circuit. So this is the reason why you require multiple collectors.

Now what we shall do is next as I said we shall try to take a simple circuit drawn using NOR gates and try to see how you can realize the equivalent I square L transistors circuit. Now let us take the circuits. Can you say what this circuit is? So here you have NOR of A and B, here you have the NOR of compliment of A and B and then again you have following it up with a NOR. This is a half adder circuit basically, so here you have the sum and here you have the carry that is here you have A bar and B bar and if you take the NOR of A bar and B bar you have here A B and here you have actually A bar B bar. You get the exclusive OR, so this is A exclusive OR B. So this is the sum output and this is the carry output, so this is the half adder circuit, a famous circuit. Now let us try to realize it using I square L.

Now I shall just note down some points, how you should go ahead with converting this into I squared L. So first I think if you follow this point by point it is very easy. Assign a number to each gate, so you call this is gate 1, this is 2, 3, 4, 5. Each gate output is represented by a node, see by a node what you mean is in the I squared L circuit, when you are just connecting two collectors that is the node. Basically the logic is being achieved by connecting the collectors of each individual cell. So each gate output here is represented by a node in the actual circuit.

Number three is number of inputs to the gate is equal to number of collectors at the node. That is if you have a 2 input gate here, you will have 2 collectors connected at the node. Of course you don't have 3 input NOR gates, if you have 3 input NOR gates you will be basically tying up three collectors at that particular node. Number of fan outs equals number of collectors of the next transistor. Next transistor means the node is at the base of a transistor. So the number of collectors for that transistor at whose base you have the node denotes the number of fan outs. For example if of course this is a very simple circuit, if you have more than one fan out suppose this point is going to some other circuit, so here you are connecting this output to 2 points.

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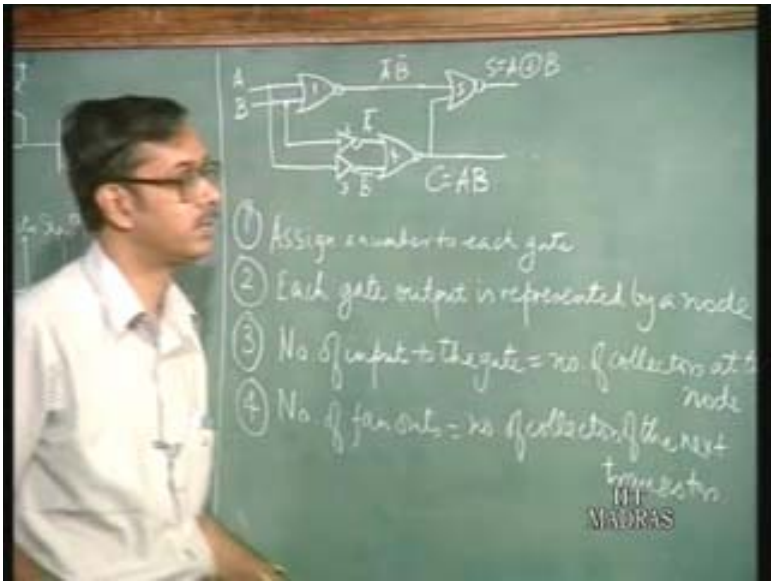

The next transistor has to have 2 collectors because the output of this gate is going to be fed to 2 different points and you cannot use the same collector to feed 2 different points. Just as we had seen in the example where you are making A plus B and A plus C that is if A has to be fed to 2 points, you require 2 collectors for that transistors. If the number of fan outs for this gate is more than one, you require more number of collectors. So this is the general rules we have to follow, once you follow set of rules you can very easily obtain the circuit.

Now let us look at how to realize this circuit. First we shall see here A and B, they are tied together, this is 1 node and this node represents gate 1. So this output is represented by this node, at this 1. Now the next gate is number 2 is an inverter. Inverter of course you can consider it as a one input gate. So basically in the node there is just one point, one connection that is actually not a node and so you have connection coming from A so like this, so this is 2. If you go back to this circuit you will again see that from point A, we are actually taking two connections. So you require for this that particular transistor must have two collectors. Similarly for gate 3, so this is the node 3. Now what about gate 4? It is a NOR gate, again the inputs are 2 and 3, so this is 4 and then that leaves us with 5 where the inputs are from 1 and 4. So this is 1 and this is gate 5. So that completes the circuit. So that particular circuit can be represented by this layer. Of course here one thing is that we have not drawn the PNP's, we have just drawn the NPN's. Usually in many cases you will find also in text book the PNP's are not drawn because it is always assumed that at each base you have a PNP. So that is common, you need not it, you can just write separately that at each base it is assumed that there is a PNP at injector.

So many cases people just avoid drawing it but it is assumed it is there otherwise circuit looks very cumbersome. So that completes the circuitry. Of course if you want to take outputs, these points 4 and 5 where you have the carry and the some logic values but suppose you want to take an output directly from those points, what do you do? You can put a resistance here and connect it to supply. So this point will give you the sum value that is when any of these transistors goes to saturation, the voltage here is going to be 0.2 volts because is the current flowing here and the voltage will drop to 0.2 volts and both of them are cut off the output is going to high, we can put that. Now if you want to take the carry output what do you do? You must take the output from this point, actually it is 4. So basically what do you do is you cannot take the output from here because this voltage cannot rise to more than 0.7 volts. What you can do is again you have to make another NOR gate and do that. That is basically you can take another collector here and connect it here.

Now what is the logic here? It is the same as 4 but here you can connect, this is constant V_{cc}. This is going to give you the carry output A. So if this transistor goes to saturation, this voltage is going to go low. Any of these transistor goes to saturation this voltage is going to go low, when both of them are cut off then only this output is going to be high. So if you want to take an external connection, you have to do this way. It's very simple, you don't require any additional transistor as such, you just require additional collectors for this. so you see that the advantage of I squared L is that you may have the half adder, a complete half adder which requires 5 gates or here 1, 2, 3, 4, 5 and you just required 6 transistors. Whereas in TTL for example just one single gate you required so many transistors. So this just six transistors you required a half adder. So you can look at the savings in area when compared to TTL I mean it's really great. That is what made I squared L so much when it was first invented, it become so popular. That we can really make very large scale circuits and also we don't require really require any resistance, any passive components, you can just connect the transistors like this and achieve the results.

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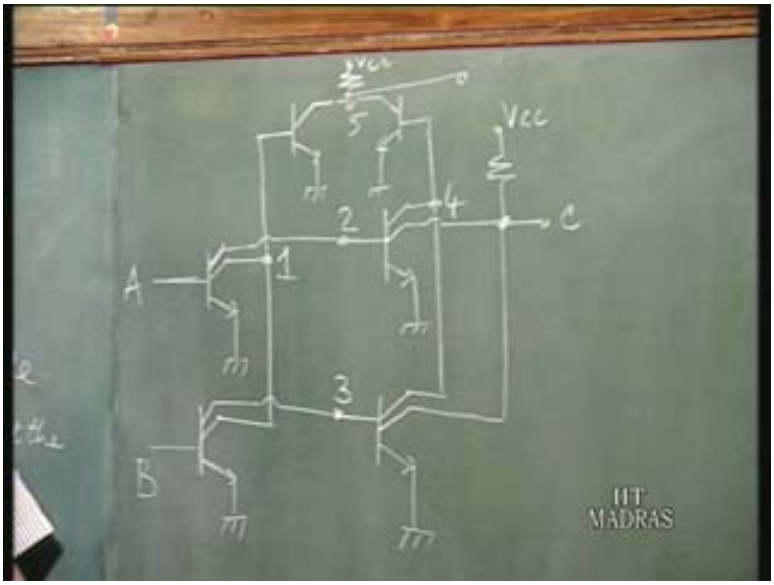

Now from here once you get the circuit, the next step is finally you have to go to the layout and once you have the layout one can really fabricate it. You have the mask drawing, you generate the mask that is the regions where you want to diffuse different regions and then you can go for the mask transistors. The next step is the layout which is simple actually. What we have seen is one cell, now we have so many cells to be connected. Now if you look at each transistor now say for example we have one transistor here with input A. So this is the transistor with two collectors, this transistor with input B this is also a transistor with two collectors. So you can draw it like this, so this is the base, these are the two collectors.

This is the base, these are the two collectors and then what do you do is you short one of that collectors. So one input is A and the other is B and then you short one of them and it goes to the base of another transistor here. That particular transistor has just one collector. so we draw the base like this, this is the collector so you short them, this is the metal line running, you short them so this is how you make connections and you can actually sort of draw the layout of the entire circuit. I will leave it to you, you can try it out and maybe next class I will draw the circuit for you. I will give you an opportunity to try to draw out the entire circuit.

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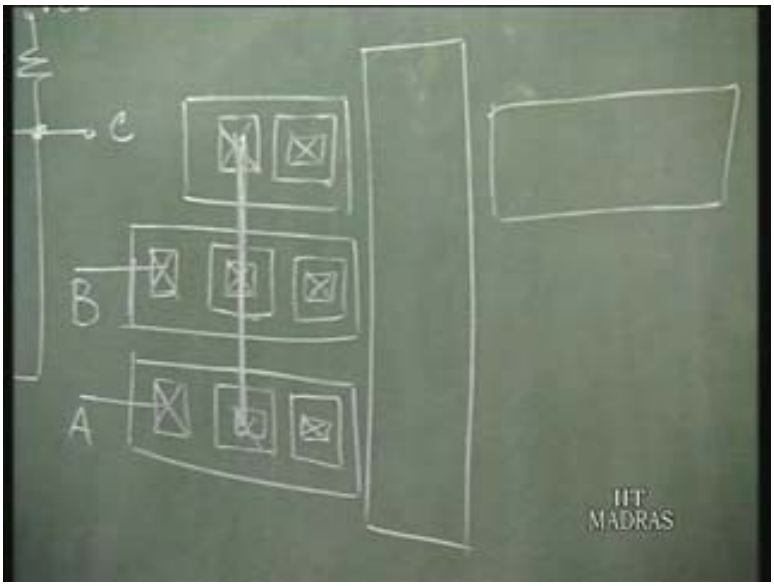

So the main point is this is the injector and you can have circuits on either side of the injector. So injector will be injecting on both sides. So anyway I will leave it to you, please try it and in the next class I will draw it for you.