Digital Integrated Circuits
Dr. Amitava Dasgupta
Department of Electrical Engineering
Indian Institute of Technology, Madras
Lecture – 11
Advanced TTL Circuits Introduction to I2L

We shall continue our discussion on TTL gates, we were discussing the LS TTL gate and some variation of it. What we saw in the last class was the open collecter which is used mainly so that you can wire the output of two gates, you have the wired and connection which cannot do otherwise in a normal TTL gate with active full up because in such a connection you may have cases where the output is not defined as well as you may have the problem of a very large currents flowing. You can only do it with an open collector gate and the advantage you derive is because of the wired connection you save a lot of gates, you can obtain more complex logic functions using fewer gates but at the same time you have to pay for it in terms of speed. It is not going to be as fast as the normal TTL gates.

Toady's class we shall look at just one more variation, I will just draw the LS TTL gate once again, this is the LS TTL NAND gate. By now I think you must be quite familiar with the circuit and you should be able to draw it very easily. There is some resistance here, then you have the input diodes, I will just note down the resistance value. This is 20 k, it is 8 kilo ohm, this is 1.5 k, 3 k, 120 ohm. This is the LS TTL gate. The variation I was talking of in the last class was the try state logic that is normally in a logic circuit you expect the output to be other logic one or logic zero. That is either the output is high or the output is low. Now you may have a third option where the output is neither high or low but it is called the high impedance state.

For example when you require it, if you are connecting a number of gates say few number of NAND gates to a common line, the common bus. These maybe the output of some circuits connected to a common line and at any particular instant you would like the output of this gate for example to be available on the line and the other should not effect it. For some other instant you may want this, the output of this gate to be available on the line. When you enable this gate, all other gates should be disabled. Disable means they should not have any affects, as if it is an open circuit. There is an open circuit here. It is as if only one gate is connected to this line. This is possible only when this output is in the high impedance state that is the output is neither sourcing any current nor sinking any current as if it is open circuit.

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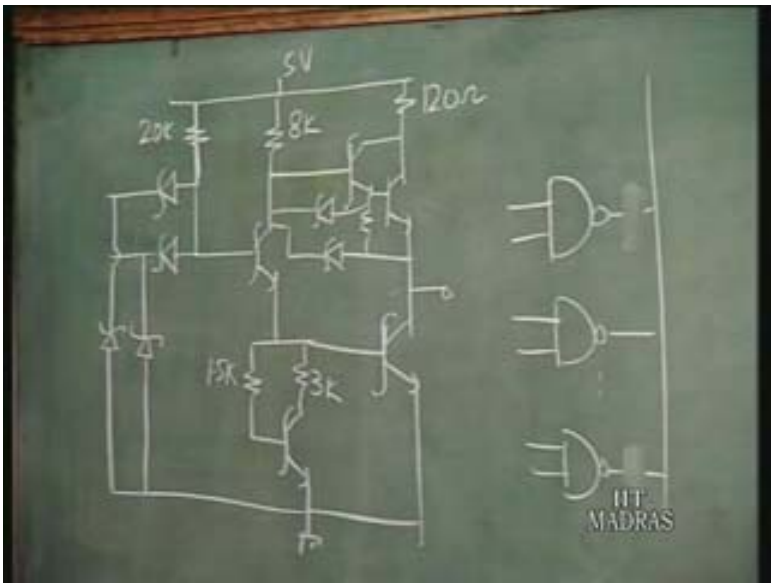

That is possible in this configuration here, if you can switch off both this transistor the pull down transistor and also the upper half. Of course you have complete circuit, you have more diode here anyway. When you switch off this lower half, this pull down transistor as well as the pull up. In that situation it is as if this is floating that is neither it is going to source current nor it is going to sink current. How do you do that? It is very simple alteration or a simple additional components are required. What do you do is we have another input here, diode here just like this one and there is another diode coming from this point here. It joins up with this input here. You have two diodes here which is connected to this common point, one is connected at this point here and the other is connected in this one. Now what happens is when this input goes low, this diode is conducting. It is going to pull this voltage down here low. What is going to happen is these two transistors are going to turn off, at the same time when this point is low you see that this point also is going to be low enough so that these transistors cannot conduct.

Basically what is happening is when this input goes low here, all the transistors here are going to switch off. This diode just acts like another input here to this gate, at this point because of this diode. So when any input is low you know these two transistors are off and by this additional connection here, this point is also made to go low. If this is 0.2 volts, this is going to be an around say 0.5 volts or so because of the drop of the short key diode and if you have 0.5 volts here, that is no way that these transistors can turn on. It ensures that all these transistors are off and as well as these are off. Now when the voltage at this point goes high what happens? None of these two diodes are going to conduct. This is like a NAND gate when any input is high, output is governed by the other inputs, it has basically no effect in an NAND

gate. When this goes high then the output is going to be governed by these two inputs. That is basically in a NAND gate when any input goes low then only the output goes high. If all the input goes high then the output is going to be low.

When you make this high, this diode does not conduct so it doesn't have any affect, also this diode doesn't conduct, this also doesn't have any effect. Basically when this input is high, it behaves as a normal to input NAND gate and when this input goes low, it goes to the third state that is the high impedence state and the output is going to be floating. This is another variation, this types of gates are also available in the TTL series. Basically these are used as buffers where you can either connect or disconnect the output of a particular circuit on to a common line. I just wanted to tell you, as a small variation of the normal TTL gates. Now continuing our discussion on the advances in the TTL family, the next series of TTL gates came out in the eighties and called the advanced series, you have the advanced short key as well as the advance low power short key.

Now the advance short key is basically the circuit is similar to the short key gates or I should say it is very much similar to the circuit of the 74 LS, this is 74 LS 00. The advanced short key 74 AS 00 is very much similar to the 74 LS 00 circuit except for the fact that since it is supposed to be a high speed gate, the resistance values are quite low. It is similar to the short key series. The circuit itself is quite similar to this, there is no variation in circuit except that the resistance values are same as the 74 S 00 but for all these advanced short key gates there is a lot of improvement in technology.

For example all these advanced short key LS series they are fabricated using 3 micron technology. You see that it is come down from 6 micron to 3 micron as well as other improvements like instead of junction isolation which you had in the previous gates you have oxide isolation. That is the individual transistors which were isolated using PN junctions, I have drawn in the previous transistors configuration you are seeing that there are PN junctions which are used to isolate the individual transistors. Instead of that you use a more improve technology where you have silicon dioxide which is used to isolate the individual transistors and this reduces the parasitic capacitances to a large extend and improve this speed. These are some of the improvements in technology which took place in the intermediate time and these were incorporated in the advanced series. So 74 AS, the improvements for quite remarkable that the delay was 1.5 nanoseconds whereas the power dissipation for this gate was 20 milliwatts.

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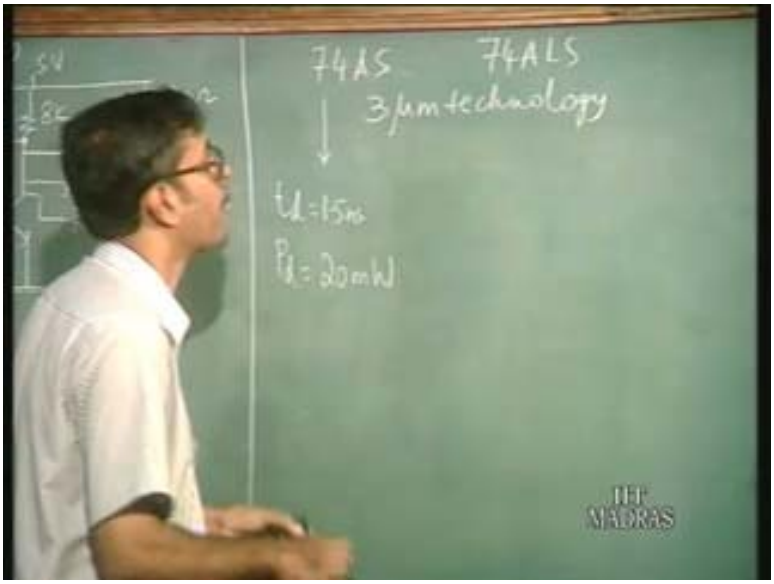

The delay has come down to 1.5 nanoseconds from 3 nanoseconds in the short key 74 S 00. In the power dissipation of course remains the same. You see that there is a lot of improvement, in fact this advance short key series is the fastest of all the TTL series available. This is the minimum delay which is reported then you have the advance low power short key which is again a variation of the 74 LS but here some modifications of the circuit has taken place. I will just draw this circuit, you will observe that in the seven four ALS, this part of the circuit remains the same, whatever modifications are on this side (Refer Slide Time: 14:39). The inputs you will see is slightly different. You have PNP transistors at the inputs, I will explain the reason for that. Here you have PNP transistors then you have one additional transistor as you can see here and then you have the normal structures on this side as I said. Here you have some diodes going to the input.

Then the resistance values I showed you, just write them down, 40 kilo ohms, 60 kilo ohms, 15 kilo ohms, 3 kilo ohms and 6 kilo ohms. This is the circuit of the 74 ALS 00. As you can see that this part of the circuit is the same except for the fact that of course as you see here that the resistance values have been increased even more that is to achieve even lower power dissipation. When you compare with the 74 LS 00, in the 74 ALS 00 the resistance values have been increased but this part of the circuit remains the same. What has been done is an

additional transistor has been introduced here. The purpose of introducing an additional transistor is to have an additional current gain. Normally you see that when this transistor turns on, basically you have to turn on this transistor. If you have an additional transistor, this entire combination of transistors, if you put one more transistors you have an additional current gain. This transistor is going to switch on faster.

An additional transistor has been introduced here for that purpose but if you introduce an additional transistor here, what is going to happen to the input output characteristics?
The input output characteristics is going to get shifted by another say 0.6 to 0.7 volts because the input voltage in order to turn this on, the input voltage has to be more by 0.6 to 0.7 volts, because here at this point now you require 3 diode drops to turn on this transistors now. So the input output characteristics is going to shift to the right by around 0.6 to 0.7 volts but you see all these TTL families have made compactable to one another. They are all upward compactable that is if you have a circuit made of the earlier TTL gates, if you replace it with later version, just take out the older chip and put a new one with the later version, it should work. It should not create any problem. The compatibility must be maintained. How do you ensure compatibility? To do that they had introduced the PNP transistor here. Now this PNP transistor is in the emitter follower configuration basically. So whatever voltage you apply here, this is the emitter point of this PNP transistor. Instead of the diode you have a PNP transistor and this PNP has a drop V_{BE} drop here in this direction. The base emitter drop in this direction. This compensates for the additional V_{BE} drop because of this NPN transistor.

In order to compensate for this V_{BE} drop of the NPN transistor, another PNP transistor has been introduced which is in the emitter follower configuration. That is the purpose of the PNP transistor, you also have some additional diodes, this point here that is the base of this transistor is connected to the two inputs so that when any input goes low this transistor will be switched off, this transistor must be switched off fast. When this input goes low, it is direct connection to this point. This base charge can be removed and this transistor can be switched off, the voltage here is going to fall instead very fast. That is why you have diode connections from this point to both the inputs.

This part basically again to summarize, you have an additional transistor here that is the purpose is to increase the internal current gain so that the output pulled down transistor can turn on faster but to compensate for this additional V_{BE} drop here because the characteristics is going to shift, PNP transistor in the emitter follower configuration. This is the emitter point that has been introduced and together with that these additional diodes have been introduced so that they have direct connection to this point also. So that when any input goes low, this transistor here which is basically the phase splitter part, when we talking of this transistor can switch off faster.

That is the circuit modifications in the ALS series 74 ALS and the other modification is higher resistances. In the ALS series the properties, the delay is 4 nanoseconds and the power dissipation is 1 milliwatt. If you look at the evolution of TTL gates starting from the standard

TTL where you had the power delay product of 100 Pico joule, this is the best or you can say the minimum power delay product of just 4 Pico joules. You have 4 nanoseconds delay and a power dissipation of just 1 milliwatt which is very good.

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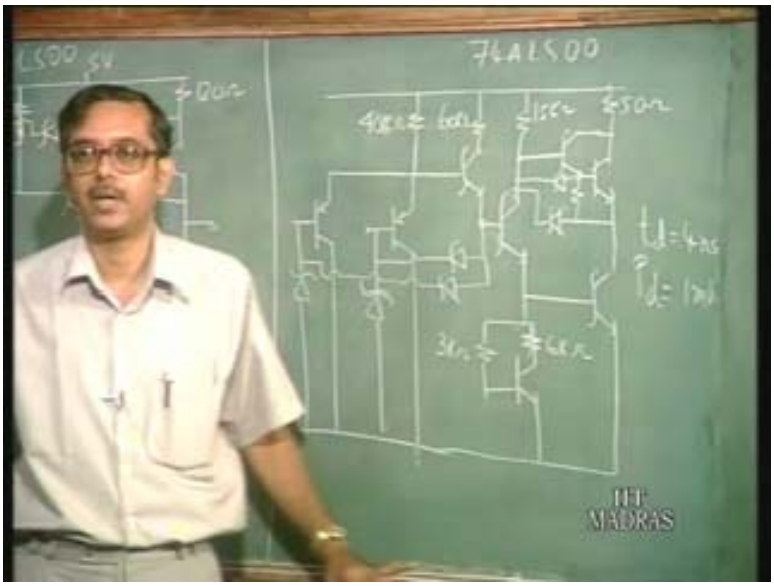

From the circuit point of view this is the last word in terms of TTL gates but of course if you are interested in very high speed you can go for AD AS series advanced short key which gives you the minimum delay but if you are not so much concerned about speed and of course go for ALS series which gives you reasonable speed and very good power dissipation. I mean very good power dissipation in the sense very low power dissipation. This is how TTL series had gone from over the years, it has changed for about 2 decades and after that of course not much has taken place. In fact the trend has shifted now in the sense that later there was some 74 series compatible schemas gates which have come up. They are basically seemas gates but with the pink compatibility and total compatibility with 74 series. That is basically you can replace 74 series gate with the seemas series, they are 74 AC family or ACT.

These are some of the family. they are basically seemas families but they have pin compatibility with the 74 series as well as the input output compatibility and there of course the delays are about 5 nanoseconds or so but of course the advantages of seemas says very low

power dissipation even much lower than this. That is another advancement which has taken place of course they are not the exact TTL family but now that is also available where lot of further advancements have gone in that direction.

We will just summarize about TTL gates. TTL gates which are available are medium scale integration chips where you get the different flip flops or even more complicated circuits like counters, shift registers and some other of these multiplexers and you can use them to make some small or even complicated systems. These are what available and being widely used even today to make systems but the problem with TTL is that you cannot make very large scale integrated circuits out of TTL because of several factors. It involves a number of transistors and the prevalence of large number or resisters in this configuration.

In integrated circuits it is very difficult, I should say that it is not advisable to have too many resisters because resistances take up a lot of area on the silicon wafer. If you want to make large scale integration, you must be able to avoid these passive components resisters, capacitors as far as possible. In fact the active components that is the transistors or the diode take much less area compared to the passive components. So for large scale integration this is not suited at all. We do not have large scale integrated TTL circuits but they are available in very large wide variety of circuits as I said like in gates, flip flops then counters, shift resisters with which you can make a big system and you can make your own circuit. If you have a circuit you can connect them together and make reasonably good circuits. That is about TTL gates. We shall stop here about TTL gates and take up the next logic family.

The next bipolar logic family in a course that is I squared L that is integrated injection logic. We shall again go through the same process that is we shall see how it developed and what is its present status. So I squared L or I I L stands for integrated injection logic. To start with IIL, we shall first take up very old logic family in which it has its roots. We again go back to familiar transistor as an inverter circuit using a BJT. This is the circuit of an inverter using a BJT. Suppose I connect another transistor here in parallel. If these are the two inputs and this is the output say, A B are the two inputs and Y is the output what is the logic functions that this circuit performance. It is a NOR gate because when any input goes high basically this transistors conducts and this transistor is going to go to saturation, the output is going to go low. When both the inputs are low, both are off output is high and when one is high, one is low of course because one transistor is conducting, the current will flow and as a current flows there is drop across this resistance and the output is going to go low.

Basically when any input goes high, the output is going to go low which is a NOR gate. This is a NOR gate (Refer Slide Time: 31:30). Now suppose this output is connected. We have a two input NOR gate, now this NOR gate output can be connected to some more NOR gates, say some more two input NOR gates. Let us look at this circuit. This output of this NOR gate is connected to 2 further NOR gates I mean these are the two fan outs. You should be able to connect it. Suppose I connect it here; there is another similar circuit here, it comes here and another two input NOR gate and you have another two input NOR gate. This is this particular

configuration, this three 2 input NOR gates, these two input NOR gates is driving these two 2 input NOR gates. This particular logic family which in early days, it was called DCTL which stands for direct coupled transistor logic. This is because these transistors are directly coupled; this output is directly coupled to the input of this transistor.

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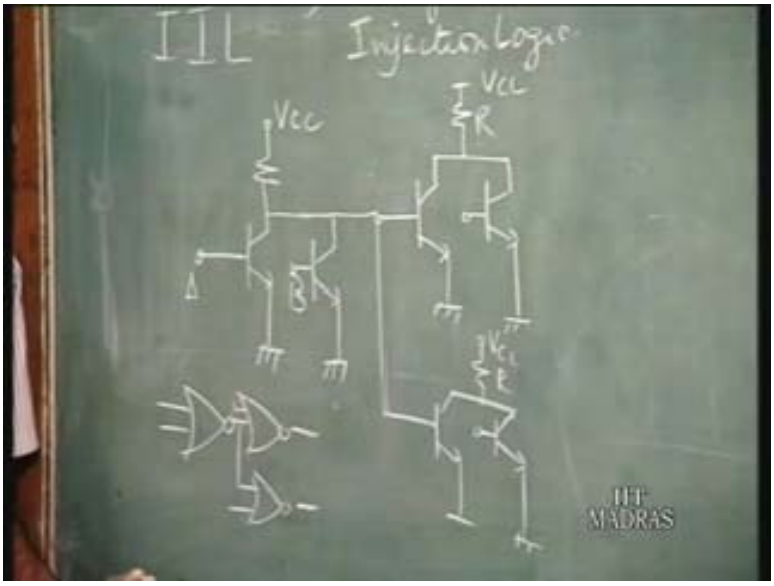

Now this logic family did not survive because of a particular drawback. The reason is the drawback is like this that the output is connected to the inputs of the different logic gates and basically what you are doing is you are shorting the basis of these transistors. Now these transistors may be on different chips also. They may not be identical. This transistor and this transistor, they may not be absolutely identical and the cut in voltages of the base emitter junction of these transistors may be slightly different. That is the voltage at which this transistors starts to conduct, the base current starts to flow maybe different from this particular transistors. These transistors may be slightly dissimilar.

What is going to happen is that when this transistors starts to conduct say suppose the difference maybe very small maybe 0.01 volts also or maybe 0.02 volts but what is going to

happen is because of the exponential nature of the IV characteristics of the input, what is going to happen is if this base starts conducting at a lower voltage, when this starts conducting the voltage will become more or less clamped and this transistor is not going to get current because if the input voltage is not going to raise to the point when this is going to start conducting because these are shorted, when this starts conducting the voltage here becomes clamped and this is not going to get the current.

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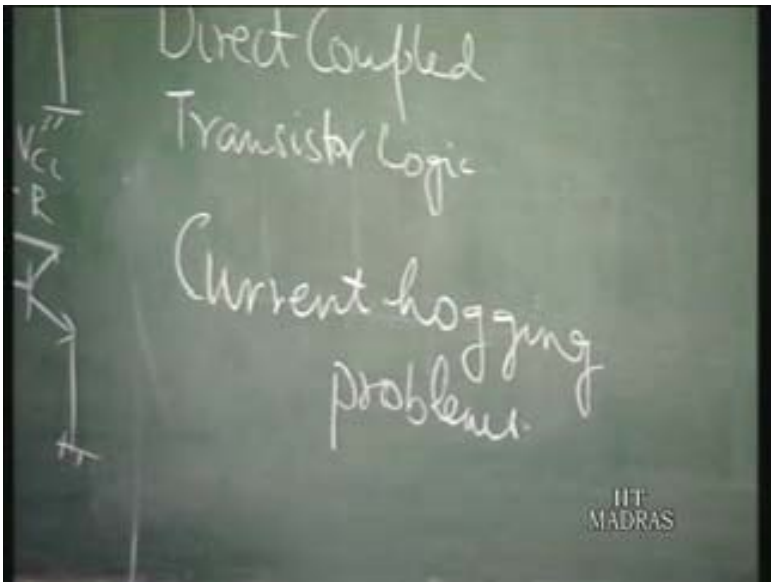

This particular problem has got a definite name, it is called the current hogging problem and that is basically one of the transistors is drawing most of the current and depriving the other. This is the problem due to which this particular logic family could not gain ground as such. Then now if you look at this circuit again suppose I take this part in the circuit, this for resistance up to here. That is this part of the circuit that is this resistance here and these two transistors. I can draw it like this, you have two transistors one more transistor like this which is to going to V_{CC}, this part of a circuit. Now just like we had multi emitter transistors, now if we can have a circuit which is something like this one base emitter junction and two collectors and this one instead of a resistance what we have is a maybe current source. This is going to

be an equivalent circuit that is basically what we are looking at is here the two base emitter junctions that is if you have transistor with common base emitter junction then of course you don't have the problem of current having because there is a same base emitter junction and because these base emitters are in parallel and these emitters are grounded and the base points are shorted, you can have a common base emitter junction and multiple collectors.

A transistor with the common base emitter junction and separate collectors and instead of this resistance you have this current source. This you can think of it this way. Now you can realize this current source, the next circuit which I draw is I will just replace this current source. I realize this current source using a PNP transistor. Here it goes this way, we have a V_{CC} and a resistance here. Now this is the PNP transistor, the base of the PNP transistor is grounded. Now this emitter point is going to be more or less fixed at 0.7 volts so the constant current is going to flow V_{cc} minus this emitter voltage by R and if this transistor has high in a beta, you can say that the collector current is almost equal to the emitter current. This behaves as a current source. We have realized this current source using a PNP transistor, this configuration is derived from the DCTL family, this particular configuration which you have here is the basic I squared L cell, unit cell of the I squared L family.

A PNP transistor and an NPN transistor. Now the way it works is like this. Again it is just similar to a DCTL that is you have a current source. Now if the input is low what is going to happen, basically you have another cell connected here. You may have another of this connected here, output point. If this point is low which means that the next transistor is going to be off, it's not connected and how this is low? Because this transistor is in saturation. The current which flows here is going to flow into the collected of this transistor. If this transistor is off, this output point is going to raise high and this current which is flowing here goes into the base of this transistor.

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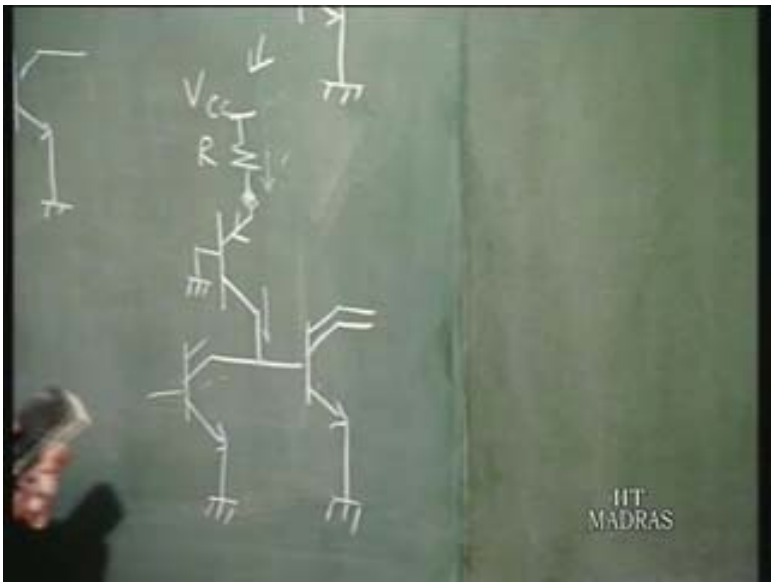

Basically the current from the current source either flows into the previous transistor, if this is conducting or it is going to flow into the base of this transistor making this transistor go to saturation. The voltage at this point is going to be either 0.2 volts if this transistor in saturation or 0.7 volts if this transistor is conducting. Basically the voltage here changes by very small margin 0.2 to 0.7 volts and the current either flows here or there. We shall see later how you can realize the different logic circuits using this. In fact the I squared L logic family was invented I should say in the Philips laboratories inovan, Holland. Late sixties I think or early seventies. You see that you have a structured here which is a very simple structure one PNP, one NPN this is the I squared L structure. Now how do you realize it? We need to draw the cross section to see how this can be realized. How do you realize it is start with a wafer which is n plus on n, when just you have guard ring then this is the PNP transistor. This is P, this is n, this is P, n plus, n plus. These are the contacts. Now the PNP transistor which we have here, this is the PNP transistor and this is the NPN transistor and this n, the contact this is ground.

If you look at it this way the PNP transistor, this P region acts as the emitter of the PNP transistor, this n region is the base and this P region is the collector and this NPN transistor the collector is here, base and this is the emitter. This n region actually acts as the base of the PNP transistor as well as the emitter of the NPN transistor. You see that the base of the PNP transistor as well as the emitter of the NPN transistor is grounded. This is the ground region, this n region acts as both the base of the PNP as well as the emitter of the NPN transistor. This P region here acts as the collector of the PNP as well as the base of the NPN transistor. Collector of the PNP so this is shorted here, collector of the PNP as well as the base of the NPN transistor and this is the collector of the NPN.

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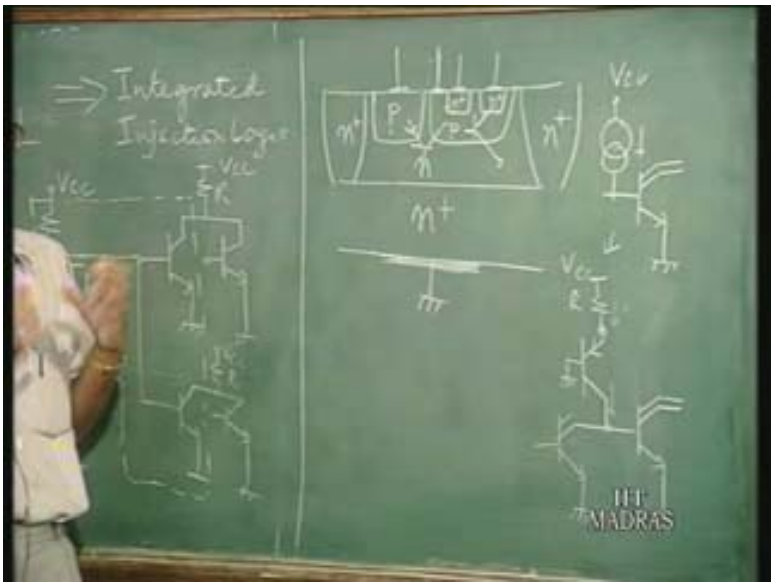

These two transistors, the PNP and the NPN are basically merged together. In this particular configuration and that is why this logic family is also called by the name of MTL or we stands for merged transistor logic MTL or merged transistor logic. Initial days it was also called by that name. This is the particular configuration of the I squared L structure. The advantage we can see is that because of this merged transistors, the area required is very small because you are merging the two transistors and in fact the I squared L family does not require any resistances. In fact this resistance which you see is usually external to any chip which you fabricate. It is this point which is available and this you can connect the supply voltage through a resistance and this I squared L family is ideally suited for large scale integration that is very complicated logic circuits, even microprocessors have been made using I squared L. This is the only bipolar logic family which is suited for very large scale integration. That is the strong point of I squared L.

In fact I think there will be lot of questions in your mind about this particular structure. Why we start with n on n plus and the point here is because of this particular structure, the NPN transistor is actually inverted. That is normally you have the emitter on top and collector on the bottom but in this particular configuration just to enable us to have a merge transistor structure, the collector is on top, this is the collector. That is the collector is on top and the emitter is on bottom. I will also draw the top view of this cell because we shall be doing a lot of this. This is the n plus which is the guard rings sort of, I shall also explain later why we require a guard ring. These are the collector region, this conduct is called the injector conduct that is basically the emitter of the PNP transistor that is called the injector contact.

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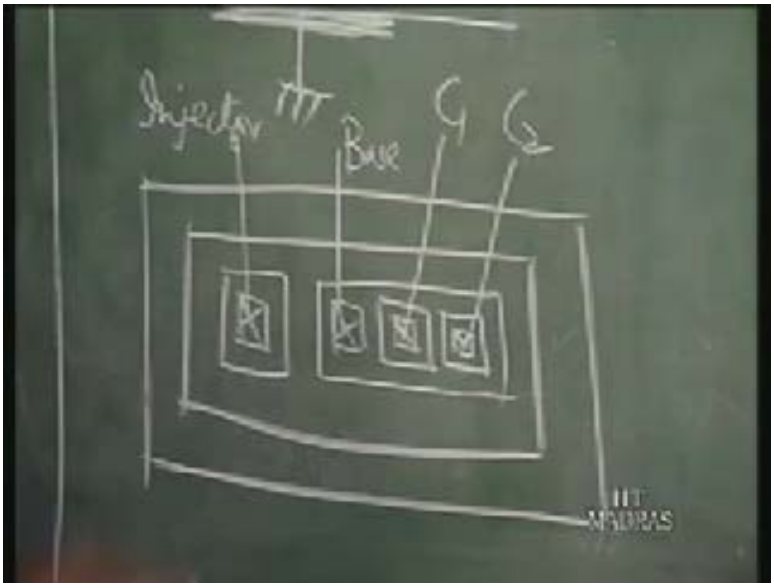

Then you have the base conduct then you have the two collector conducts. I will call $C_{1.}$ and $C_{2.}$, $C_{1.}$ and $C_{2.}$ the two collector contacts. These are the collector diffusions done inside the base region. This is the base contact and this is the injector contact, this just gives you the top view and this is the cross section view. In the next class we shall take up more detail and discuss why we require this particular structure and then we shall go ahead and also see how you can realize other logic gates like NOR or NAND using the I squared L structure and even more complicated circuits.