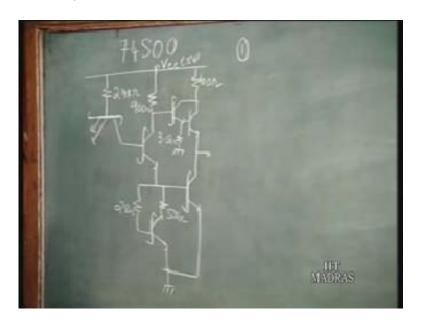
## Digital Integrated Circuits Dr.Amitava Dasgupta Department of Electrical Engineering Indian Institute of Technology, Madras Lecture-10

## Schottky (74s..) and Low Power Schottky (74ls..) TTL Circuits

We shall go ahead with our discussion on TTL gates and we shall see how the TTL gate evolved as such from its original circuit to the present day circuits. So in the last class we were discussing the Schottky TTL gate 74 S 00 and that is the Schottky TTL NAND gate and we have drawn the circuit of this particular gate and we have also noted down the major differences or the differences of this gate from the corresponding standard TTL gate. In today's class we shall look at the importance of these changes and how they affect the characteristic of this TTL gate. Firstly all these transistors are actually Schottky transistors of course except one as I said this one because this transistor has no possibility of going into saturation. This V.cc. is 5 volts, the resistance values are given here. Now let us see we shall again write down the major changes of the circuits of this circuit when compared to the previous circuit that is the standard TTL circuit 7400.

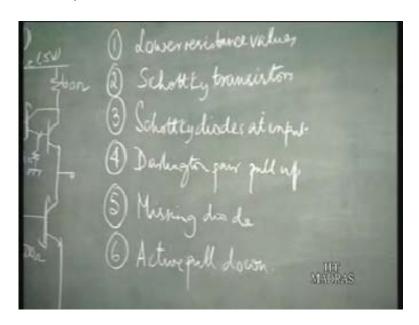
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What are the changes? Number one is lower resistance values, number two Schottky transistors, number three that is there are diodes at the input, Schottky diodes at input Darlington pair pull up, number five missing diode and number six active pull down. So these are the six changes which we have mentioned so we shall look at the significance of these changes in improving the performance. Now some of them are quite obvious and which we have already discussed like lower resistance values. As I

said the Schottky diode, this particular family Schottky TTL family is aimed at high speed performance.

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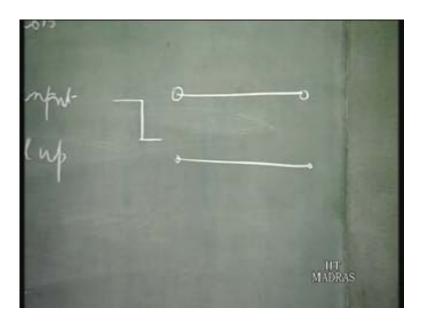


It is aimed to achieve high speed and so the low resistance values, when we discussed the bipolar transistor inverter circuit that how lowering the resistance is going to improve speed in the sense that the charging and discharging currents are going to be more. Of course you cannot go on loading the resistance indefinitely because once it goes into the regime where the diffusion capacitance starts to dominate then it is no longer so effective. When the junction capacitances are still effective then this lowering this resistance values is going to improve the speed. This we have already discussed. So this lowering resistance values helps to improve speed, of course at the expense of power dissipation. So you get more power dissipation but here the stress is on speed as I said. We would like to get higher speed.

Then Schottky transistors, this again is an obvious change because what we want is the Schottky transistors as you know do not go to saturation and as the transistors do not go to saturation, the storage delay times are eliminated and so we have higher speed. The delays are going to be much less, so these changes I think are quite obvious. Next we shall look at the Schottky diodes at the input. So if you look at the circuit here, there are two diodes at the input. What is the purpose of these diodes? In any high speed circuit that means the charging and discharging times are very short. The rise times and fall times of the signals are very small then if you have a wire like this. If you have a sudden pulse like this, now this is a very sharp transition then basically any wire has a delay of its own. The signal does not go instantaneously at the other end. Now if the

delay of this line becomes comparable to the rise and fall times of the signal then one cannot just consider this line to be a short.

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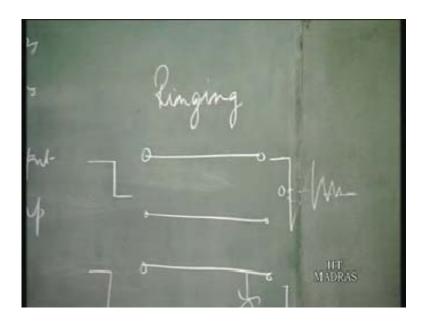
What does one have to do? One has to consider the inductances and capacitances of this line basically it behaves as a transmission line, it's no longer a short but it behaves as a transmission line. Then you have some of the effects, one of them is called ringing like the signal may be it takes some time to settle down, at the other end you may get something like this. So finally is going to settle down here but you have ringing. This is very dangerous in a digital circuit because for example if this is a clock and it goes like this what you want to do is there is supposed to be one transition and if it is a clock to a flip flop say, the output should change only once but if you have something like this which may result in a number of transitions. If you have a shift register, you just want to make one shift but you will have many shifts. This is quite dangerous and this is there in a digital high speed circuit.

So in fact it was the end of the course, we shall deal specifically with this problem because this is a very important problem specially in present day high speed digital circuits where the delays and the rise and fall times have come down and interconnects play a more and more important role. I mean you cannot just neglect the interconnects and think of them just as short circuits. You have to model the interconnects, in fact when you do a circuit simulation using SPIC or anything you have to use the transmission line models to interconnects, when you go to very high speed circuits. So

this is very important. Basically you have something like this. Now if you have a diode at the input just like this, what is this diode going to do? When the input voltage becomes negative, this diode is going to start to conduct. This side is ground, so this is a Schottky diode so this cut in voltage of around 0.2 to 0.3 volts around 0.3 volts say. So this voltage cannot go more negative than minus 0.3 volts or so. This is going to clamp this input voltage to that value.

So what is going to happen is suppose if you have a diode like that across this end a Schottky diode, so if you have a transition like this basically this is the zero point, so it doesn't go negative by much. It just sort of reaches the steady state much faster because it doesn't allow it to go much negative. If it is plus V<sub>CC</sub> to zero, it may go all the way to minus V<sub>CC</sub> and then it will take a long time to settle down but since it cuts it off here, it doesn't go much negative it reaches the steady state much faster.

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This type of the diodes of the input is basically used to prevent these problems due to ringing. What is called ringing? This phenomenon may be you have seen an oscilloscope many times. When you have digital circuits instead of settling down they take a long time to settle down. Specially if you use very long wires from one end of connecting this two circuits. These diodes are basically to remove or reduce the problems due to ringing which is present at high speed circuits and this Schottky TTL is supposed to be a high speed circuit.

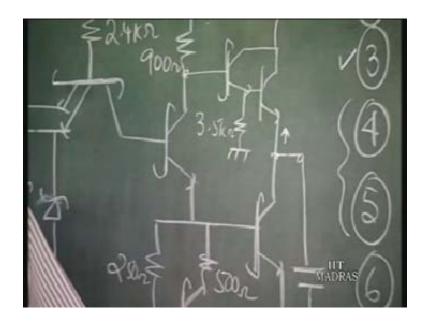
Otherwise you see normally in a TTL circuit, the voltages are always positive. When you have positive voltages here, these diodes are always reverse biased and so they have no effect on the working of the circuit. Only when this input goes negative, this

diode is going to conduct and this is going to prevent the input from going negative below a particular value. That is the function of the Schottky diodes at the input. So we have looked at these three changes. Now the fourth one which we will look at here is the Darlington pair pull up and I think we should discuss these two together and the missing diode. Now in a standard TTL gate we had a diode at this point, we had one transistor and a diode at this point. The diode was there to ensure that when the lower transistor here that is the pull down transistor here was on conducting, the upper transistor was cut off. That was the only purpose of the diode. Now why is the diode removed here because you now have a Darlington pair, so you have two transistors here.

So in any case from base of this transistor to the output point, you have two diode drops because of two emitter base junctions. There is no necessity of the diode anymore because of the presence of two transistors here. That is why once you have a Darlington pair here, you don't require the diode. Now why do you put a Darlington pair that is the question, how does it improve the performance? What does the Darlington pair do? You have two transistors like this, so the effective beta you can say of this pair is equal to beta square that is the current gain provided by this pair is going to be beta square. Now what does it do? Why did we put an active pull at first place? Because we wanted faster charging up of the output capacitance. Now that can be achieved by higher current.

If you have two Darlington pair, you have a higher current which is charging because the gain current gain is very high or if you look at it in a different way, if you have a capacitance here which has to be charged up the Rc time constant is important. This is the output capacitance say load capacitance, the Rc time constant, the r is the resistance seen at this point. Now what is going to be the resistance? The input resistance divided by beta square in this case. If you have just one transistor, it is going to be divided by beta. So effectively resistance at this point is going to be very much reduced in fact it is now going to be just few ohms.

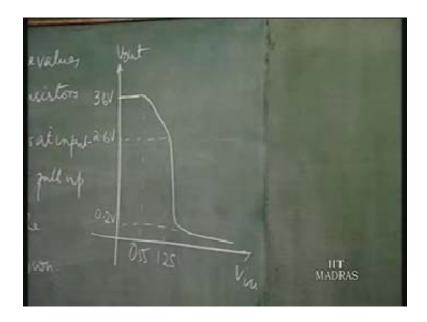
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So this results in a very low resistance, effective resistance for the pull up. This Darlington pair improves the characteristics, the speed of the device of the gate by having a faster pull up of the output voltage because of the low output resistance of the Darlington pair, inherently Darlington pair has a very low output resistance. So that is why you put a Darlington pair and since we put a Darlington pair, the diode here is no longer necessary. I think 4 and 5, these points are now clear. That leaves us with the last one that is the active pull down. Come to this part of the circuit.

Instead of a resistance, just a resistance in the standard TTL gate we have replaced it by an active circuit element, the transistor with some associative resistances. Now so what does this do? We have to look at it. It has its effect both on the static characteristics that is the input output characteristics of the gate as well as on the switching performance of the gate, both the input output characteristics are affected as well as the switching performance of the gate. Now let us see how it affects the input output characteristics of the gate? Now if you look at the input output characteristics of the 7400 gate, it was something like this. So here you had two regions, this was 3.6 volts, this was 0.2 volts then this one was around 2.6 volts. If you remember this one was 0.55 and this one was around 1.25, so this is V<sub>out</sub> now.

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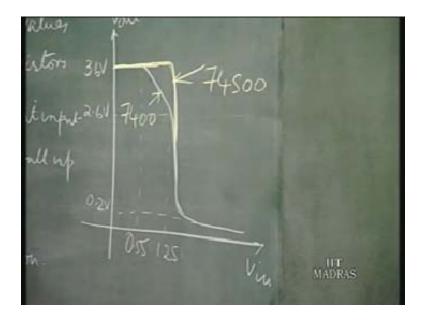


How is this characteristic is going to be affected when you put this transistor here? I will just number the transistors I think that is T<sub>2</sub>, T<sub>3</sub>, T<sub>4</sub>, T<sub>5</sub>. In this particular region when the output is at 3.6 volts both T<sub>2</sub> and T<sub>3</sub> are off. In a standard TTL when you come to this region of the characteristics what happens is this transistor which is the phase splitter, the transistor which is doing that T<sub>2</sub> that turns on, T<sub>3</sub> is off. Now what is the change that is going to happen here? Now can you have a situation when T<sub>2</sub> is on and T<sub>3</sub> is off. Now because if T<sub>2</sub> has to be on, there has to be some connection. Emitter has to be connected to ground through some resistance, now the current must flow but here at the emitter point you have either the current can flow this way or it must flow this way. This transistor may be T<sub>6</sub>.

Either it must flow to T<sub>3</sub> or through T<sub>6</sub> here. So either T<sub>3</sub> or T<sub>6</sub> must be on. Otherwise there is no connection from T<sub>2</sub> to ground. If T<sub>3</sub> or T<sub>6</sub> has to be on then they must have either the base emitter voltages or these two transistors must at least be 0.65 volts or 6 volts whatever. So the emitter voltage here must at least be around 0.65 volts before this transistor can be on, T<sub>2</sub> can turn on.

Suppose when this input goes to 0.65 volts, T<sub>2</sub> cannot turn on because there is no path to ground. So only when it reaches say around 1.3 volts or so, if we assume that 0.65 is the cut in voltage when base current starts to flow. When it reaches 1.35 volts, when this goes to 0.65 volts here so you have 0.65, 0.65 drop or 0.65 here. Then only both T<sub>2</sub> and T<sub>3</sub> will start conducting simultaneously. You don't have the situation here where T<sub>2</sub> is conducting and T<sub>3</sub> is off, both of them will start conducting simultaneously because of this part is active. So this has to turn on, this requires 0.65 volts before it can turn on. It is not a resistance when even with any voltage it will start conducting. So what happens to this characteristics? This characteristics, instead of being like this, it is going to go like this and then both of them turn on and it will have something like this.

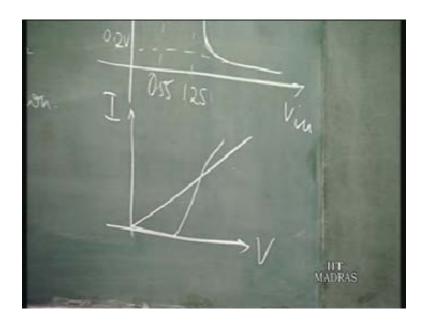
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This is the characteristic of 74S00 and this is 7400. So you have a more ideal inverter characteristics as you see here. Obviously noise margins would be improved because the input V<sub>IL</sub> that is going to be more here. That is even for much higher input voltages the output will be retained at V<sub>OH</sub>. It is a sharper transition from high to low. So that is because of that active pull down so there is one advantage of the active pull down. The other advantage is from the switching point of view. Now from the switching point of view if you look at it, when T<sub>3</sub> turns on we would like all the base current which is available to flow into T<sub>3</sub>, I mean all the current which is available to flow in the base of T<sub>3</sub> when T<sub>3</sub> is switching on, turning on.

Now if you have a passive resistance it is going to draw current but here you see initially this is not going to draw current. When T<sub>3</sub> is turning on, most of the current flows in to the base of T<sub>3</sub>. If you just compare the characteristics of passive resistance with an active pull down, the IV characteristics current voltage characteristics I versus V, if it is passive it is just a straight line like this and if it is active up to 0.6 there is no current and then it just goes like this.

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This is passive and this is active. Now we see that initially this active is drawing less current compared to the passive. The IV characteristics for the same voltage across so which means that initially when it is turning on this is drawing less current. So the emitter current part of it flows into this part of the circuit and the remaining goes into the base. So if this is drawing less current it would mean that the base is getting more current so it will switch on faster. On the other hand when this T<sub>3</sub> is turning off then what happens is that this transistor at that point is fully conducting. When this turning off, going from the on to the off state. Then what happens is this transistor because is conducting is going to draw out the base charges faster compared to a passive resistance.

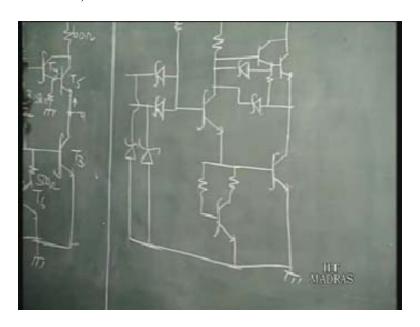
This transistor T<sub>6</sub> here in the active pull down is a more effective way to remove the base charge of this pull down transistor here. This active pull down has a very important role to play as we have seen both from the static input output characteristics point of view because it improves the characteristics compared to the standard TTL as well as from the switching point of view because it enables this pull down transistor to turn on faster by drawing less current, when it is actually turning on and by drawing more current when T<sub>3</sub> is going from on to off because this is already in the active region. So it is going to pull more current compared to the passive resistance, it switches it off faster. This is a very important change.

We have discussed all the changes in the 74S00 circuit compared to the 7400 and these changes in fact had effect on the performance in fact the propagation delay of this standard 74 S 00 is 3 nano seconds, when you compare with the 10 nano seconds of the standard TTL gate and the power dissipation of course is higher it is a 20 milli watt per gate. So this gives rise to a power delay product of 60 Pico joules which is much less than the hundred Pico joule we had for 7400. That is 7400 had 10 nano seconds and 10

milli watt, power dissipation is obviously higher because we reduce the resistances values.

So this power dissipation has gone up but this reduction in speed is much greater. You see that this is a much better circuit because of all these modifications, results in a much lower power delay product. So 3 nano seconds and 20 milli watt. So this is the 74 S 00 circuit which came in 1970 or so. We shall go ahead. The next modification was the 74 L S, the L S series which is the low power Schottky series which came around mid-seventies, 75 or so. Of course that also had some modifications, the circuit was modified so this 74 L S, I will draw the circuit.

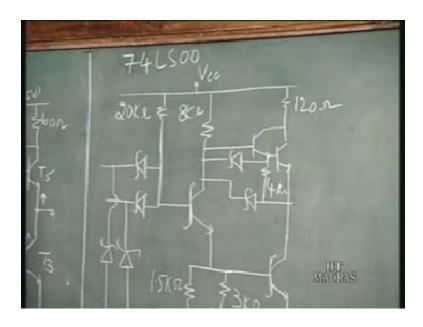
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You will see some important changes and some surprising changes also in the sense that the input which you look at it now is very much different from the inputs. In fact if you look at it, the input configuration which you have now is quite similar to the DTL type of circuit with which we started. In fact we have gone back to the DTL type of inputs. Why we shall discuss that.

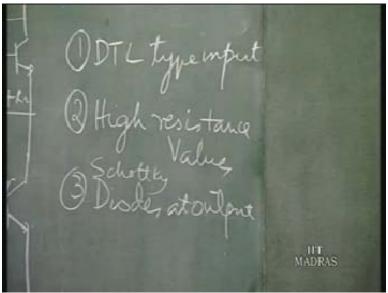
So that's a very important change. We shall look at some other changes also, there are some more modifications as we shall see here, not as much as the previous case but even then there are quite a few. So the stress here as we said 74 L S, it is called low power Schottky so stress here is on low power unlike the previous case where it was high speed. So we shall see here that is quite evident in the resistance values which we are drawing now.

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So this is the circuit of the 74 L S 00. Now again let us look at the changes. What are the basic changes in this circuit? The obvious change is at the input side. Instead of the multi emitter transistor we have diode inputs, just like DTL type of inputs, I will write DTL type of inputs. Then what are the other major change which we observe here is that there are two transistors Schottky diode basically two Schottky diodes at the output side. That is all I think, if you look from a Schottky diode, the Schottky series 74 S series, the resistance values have been very much increased because again the stress here is on low power, high resistance values and diodes at output Schottky diodes. Mostly Schottky diodes at output.

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So these are the major changes which you observe from the 74 S series. Another major change which occurred at that time you see, the original circuit was 65 then 75, with years you know technology has changed. Usually these older generation TTS's. The technology they were using was twelve micron technology whereas here it came down to 6 micron at that time, 6 micron is the minimum feature size of the transistors. Now any change like that when you reduce the dimension of the devices is going to improve the speed. Why because any capacitance, if be a junction capacitance or diffusion capacitance, all the capacitance depends on area and if you reduce the area the capacitance is going to come down and if capacitance comes down, the speed is going to go up because basically the delays are because of charging and discharging capacitances.

So they are going to come down. So there was an improve in technology, you had smaller size devices which is obviously not obvious from circuit but that is an improvement in technology. That is a continuous process, as years pass by the device dimension keeps reducing.

Now what is the purpose of this DTL type input? Why did people go back to DTL type? It was rejected at one and the DTL was replaced by TTL. So what is the necessity of this type of inputs? One reason is that when DTL was replaced by TTL, it didn't have Schottky transistors. The reason why we had multi emitter transistor because that it was removing the base charge faster and those transistors were normal transistors which were going deep into saturation and we had to remove the base charge but now all these transistors are in fact Schottky transistors. So these transistors since they are not going into saturation, so the problem of having of excess base charge storage is very much reduced because these transistors are not going to saturation. So that is one important point, so this is not so much of a problem anymore, the base charge storage problem here.

Number two these Schottky diodes have many inherent advantages compared to the multi emitter transistors number one Schottky diodes just a metal semiconductor contact and the area of the diode they have taken up by the diode is very much less compare to a multi emitter transistor because it is just a metal semiconductor contact so it requires very much less area compared to a multi emitter transistor. Number three a Schottky diode as such is different from a p n junction diode or any of these devices which we have defined the p n junction diode or a bipolar transistor in this way that it is a basically a majority carrier device or you can call it a unipolar device, unlike a bipolar p n junction diode where you have minority stored charge.

In a Schottky diode there is no minority stored charge, if you have a metal say n type semiconductor Schottky diode the conduction is due to electrons in the n type semiconductor, tunneling through the barrier at the metal semiconductor junction and say for example in n type there is no holes stored in the n type semiconductor. There is no minority stored charge so Schottky diodes as such are very much faster compared to a normal p n junction diode because the p n junction diode the delays are due to minority carrier stored charge whereas a Schottky diode is a majority carrier device, you don't have minority carrier stored charge. So it is a faster device, switching is much faster compared to a p n junction.

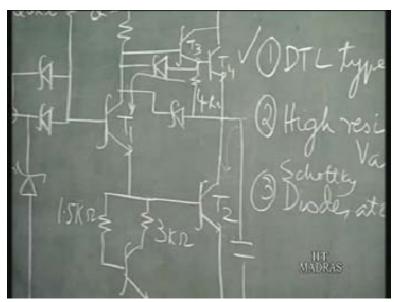
So it has its advantages, so all these factors that is less stored charge in the base then it requires less area Schottky diode compared to multi emitter transistor then it is a faster device compared to any bipolar transistor or bipolar diode, p n junction diode. So all these factors point in favor of having a Schottky diode at the input. In fact when you apply a low voltage because the Schottky barrier diode has a lower cut in voltage, this charge is 0.2 volts the charge the base of this transistor can be discharged through this also, through the Schottky diode at the input. So that is why we have a DTL type, we have gone back to the DTL type of inputs. Then of course high resistance values that is quite obvious again because this 74 L S series it is aimed at low power Schottky TTL, so high resistance.

In addition there are some small changes here, that at the output side you observe two diodes, Schottky diodes again. These diodes have been included here, one you see at the base of this transistor here. So this diode is there so what it does basically is when this transistor turns on, this Darlington pair configuration it should turn off. So these transistors must turn off. So as we have seen that these two transistors, again I shall call them by some name which is here. So when T<sub>1</sub> and T<sub>2</sub> turn on, T<sub>3</sub> and T<sub>4</sub> should turn off actually. So when T<sub>1</sub> and T<sub>2</sub> turn on what happens is this T<sub>4</sub> is turned off faster because of this presence of this diode, there is a current path which flows into this because T<sub>1</sub> is turned on, this T<sub>4</sub> will be turned off by a flow of reverse base current through this diode.

The base charge of T<sub>4</sub> will be removed faster because of the presence of this diode here. There is a connection from T<sub>4</sub> base to the collector of T<sub>1</sub> and since T<sub>1</sub> is turned on, it will remove the base charge faster. So this T<sub>4</sub> will be turned off faster. There

must be a mechanism to remove the base charge and there is another diode here which is connected to the output point and again connected to collector of  $T_{\perp}$ . That is when  $T_{\perp}$  and  $T_{\perp}$  turn on what happens the output should fall faster. Now you again think of a capacitive load here, the capacitance should be discharged faster for the output to fall.

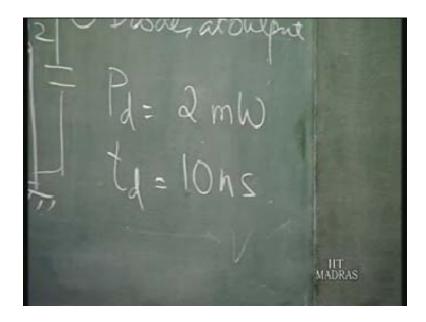
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It is done by, as  $T_2$  turns on the capacitance is discharged through  $T_2$  normally but it gives an additional path here. If  $T_{.1}$  is also turned on so through this diode into the collector of  $T_{.1}$ , so there is an additional path for the capacitance to turn off. So there are two additional diodes here at the output side. The function it does is when  $T_{.1}$  and  $T_2$  turns off, it turns off  $T_4$  faster as well as it discharges the output capacitance faster. So these are the modifications in the LS circuit, 74 LS 00 circuit basically at the input side two additional diodes here, high resistance values as well as in improvement in technology.

So these are the basic modifications LS TTL circuit and in fact this 74 L S series even today is very popular. One of the most popular TTL gates which is used and the performance wise the power dissipation is 2 milli watt, its low power and the delay is 10 nano seconds, propagation delay is 10 nano seconds. Now if you look at it, if you compare with the original 7400 circuit, you will observe that the propagation delay is the same but the power dissipation has gone down to two milli watts. The improvement is quite dramatic you can say, it's quite a bit. So the power delay product will come down to 20 Pico joules compared to the 100 Pico joules you had the original circuit and 60 Pico joules in the Schottky TTL circuit. The delay is 10 nano seconds but the important thing is the power dissipation which is quite low and that is what it is meant to be. It is meant to be a low power Schottky TTL gate.

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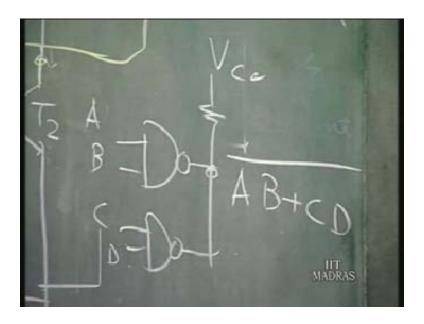


So this is the version which came out in the mid seventies and even today it is quite popular. Before actually going into the other modern versions of this gate, further improved versions of this gate i just like to tell you a little bit of some variations of this L S TTL gate. This is just a NAND gate. Now I just want to tell you about some other versions of this NAND gate. Now one point to be noted, when you use TTL gates is that if you have a NAND gate like this, you cannot connect two NAND gates together like this.

The output of two NAND gates together that is totally forbidden. Why because when you do that, you are basically connecting two outputs like this together and it may so happen that in one gate this is on, say T<sub>4</sub> this Darlington pair is on, T<sub>2</sub> is off. Whereas in the other gate because of the inputs, this Darlington pair is off and the lower half is on, in which case there is going to be say suppose you have another gate like this. There may be a current flowing like this because for this gate, this is on and for the other gate this is on. So a current will flow through this.

So on one hand there will be a large current flowing, also the output voltage becomes indeterminate. You don't know whether the output is going to be high or low. So that is the problem. So you cannot connect it like that, so what is done is you have what is the open collector gates. The open collector gates basically this part is missing (Refer Slide Time: 45:59), this box part is missing. So the output is given like this here. So in which case what you can do is if you have open collector gates two NAND gates, you can connect them together and with a pull up resistance. So you don't have an active pull up but you have a passive pull up. Of course you sacrifice in terms of speed but the advantage you derive is you have an wired AND connection.

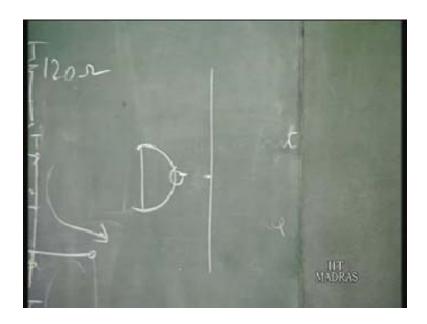
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So if you have A B C D, they are the inputs here, you will get A B plus C D bar and that is the advantage. That is you get a wired AND connection and if you were to realize this using NAND gates, you will require more number of NAND gates. So this is the advantage of doing the wired connection. So you have open collector gates also available, everything else remains the same only the output side this is missing (Refer Slide Time: 47:30). Then you have another type of gate which is called the tri state logic where you know normally you expect the output to be either high or low. Now you can have a third state which is called the high impedance state that is basically what happens is at the output if T<sub>2</sub> is conducting and the upper part is off.

Then if you just consider a capacitive load again, it is going to be discharged. There is a current flowing into the circuit, it is sinking current and the output voltage is going to be pulled down towards the ground. Now if on the other state if T<sub>2</sub> is off and this Darlington pair is conducting so this is going to pull this voltage up to V.cc., it is sort of connected to V.cc.. So it is going to sort of source current and it is going to pull it up. Now what happens if both these are off that is both the pull up and pull down is off then what happens is it is called the high impedance state. Then nothing is happening at the output. In fact you can say if you connect a gate like that, it's like in the high impedance state. It is as if this is an open circuit here, as if it is not connected to this line.

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So I think we shall take up that in the next class and together with the further advances, the newer advanced series of TTL series, you have advanced LS and advanced Schottky TTL's which have much better characteristics performance and we shall see the modifications in the next class and I think we should have enough time to go over to the next logic family that is i square L. Thank you.