Analog ICs
Prof. K. Radhakrishna Rao
Department of Electrical Engineering
Indian Institute of Technology, Madras
Lecture - 09
IC Negative Feedback Amplifiers
(Multiple stage)

So, in the last class we saw something about negative feedback and how negative feedback can result in wide band amplifiers. We started discussing with the single stage negative feedback amplifiers. How these single stage amplifiers can result in y feedback and z feedback amplifiers the negative feedback amplifiers possible only in y and z feedback and how these can be cascaded to realize wide band voltage controlled voltage sources and current controlled current sources.

Today we will see another basic principle. We would like to cascade one common emitter amplifier with another common emitter amplifier that means two stages. So, instead of one stage amplifiers we considered earlier, now we need to consider two stage amplifiers. We have a single stage amplifier being cascaded with another common emitter amplifier. This is the AC picture. Now obviously the loop gain can be enhanced considerably by cascading two stages. The disadvantage being, now the time constant involved in these two stages, the minimum number of time constants that will figure in the gain will be three instead of the two originally present.

Therefore there will be difficulties in giving negative feedback and sustaining a stable configuration because the order of the system has already become three and the loop gain has increased so it is likely to become unstable. Therefore we have to be very cautious in using this with high loop gain. It is highly likely that this is going to become unstable.

Now, however, because of its great advantages of desensitizing the performance factor with respect to active parameter you would like to go for more number of cascaded stages so that the loop gain become large. Now, in this configuration we have two possibilities of negative feedback. What are they? They are h and g.

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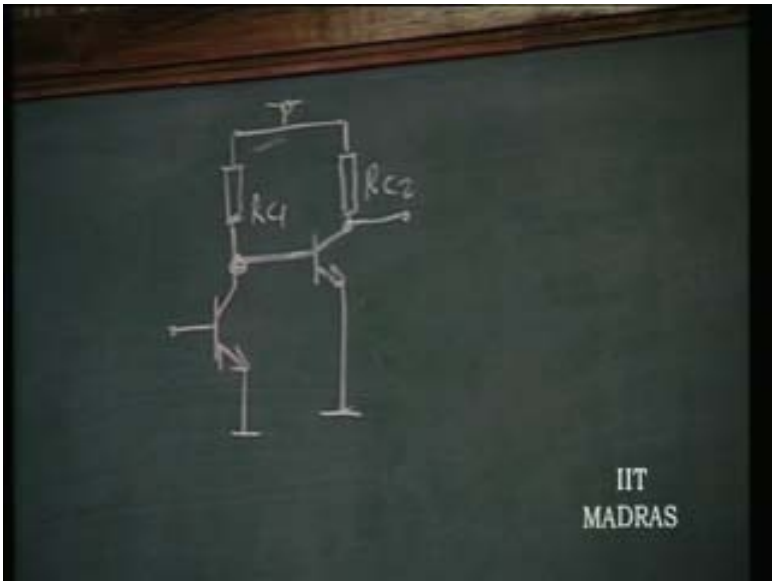

Obviously y and z will be positive feedback configuration. So let us consider the negative feedback configuration which we have perhaps studied in our Under Graduate days. The h feed back, output voltage is sensed and fed back in series as voltages. It is called voltage series also otherwise popularly. So we have the feedback resistances being called as RE1 and RF.

Now h feedback, it is easy to use h parameters in the analysis because h parameters of the amplifier and h parameter of the feedback can be easily evaluated and added together and the modified parameters will be the g parameters. And obviously all the g parameters except the forward transfer parameter will go towards 0. It is an idealization towards a voltage controlled voltage source. What happens obviously is that, as far as the forward transfer parameter is concerned is going to become desensitized with respect to the active parameters and will become purely dependent upon the passive parameters. The resultant in fact for that particular forward transfer parameter is a wide band configuration. For that particular forward transfer parameter it is going to be a wide band configuration.

So voltage controlled voltage source is the idealization to which it goes and therefore V_0 by V_i is the parameter for which it is showing wide band effect. And the bandwidth is going to be enhanced by a factor of the loop gain by the same factor by which all the other parameters are decreased and made to go towards 0. So this configuration in a simple analysis is, V_i is the input voltage is going to almost entirely occur across R_{E1} so Vi by R_{E1} is the current and this is almost entirely the current through the R_F and therefore this current into R_F is the voltage drop across R_F and the voltage at the output V_0 is going to be original Vi plus the drop across R_F. So, with the result the voltage gain is going to be R_F by R_{E1} plus 1 which we have analyzed by variety of means in our Under Graduate days. This can be also analyzed in terms of purely h parameters and e parameters and you will obtain the same value.

The input impedance is going to be increased by the extent of the loop gain the output impedance is going to be decreased by the extent of the loop gain and it is going to become very near ideal voltage controlled voltage source with a gain linear equal to 1 plus R_F by R_E.

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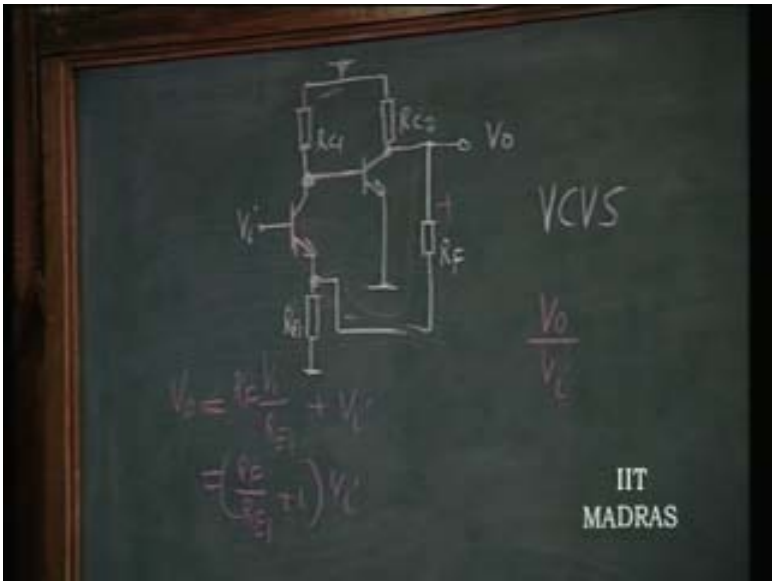

This is a popular voltage controlled voltage source wide band amplifier which has been used in integrated circuit quite often. Obviously for biasing purposes we have to either do, if you are using only NPN devices almost all wide band devices, ICs used only NPN transistors no PNP transistors was present. But in a technology where both good NPN and good PNP are present we can sort of get over the problem of cascading and biasing by coupling these together. These are all old wide band amplifiers and in most of these configurations only NPN transistor is present because the PNP is a bad PNP with a bad frequency response characteristic.

And also you will notice that, since the time constant has to be made very low in order to make the amplifier wide band the resistors used are all of the order of kilo ohms and hundreds of ohms. This is a characteristic feature of all high speed amplifiers, comparators, smith triggers anything that you think of in terms of integrated circuits where we design high speed comparators or wide band amplifiers or logic circuits we must use low value resistors and this happy with low value of gain.

Now, in order to convert this configuration, if you want, I will fabricate this as an IC therefore I want to make my job of biasing easy then I can convert this into the basic principle which is the differential mode. By converting this configuration into differential mode by converting l_v discrete circuit configuration into differential mode you are getting over the problem of stable biasing. Or otherwise you would have required level shifting and also bypass capacitors and so on. This is what is tried here.

You can see that this is one of the commercial integrated circuits fabricated using this kind of h feedback. I have just exactly repeated the identical stage here, you can do the same kind of analysis we did while converting the differential configuration. You can do that here; just simply repeat the configuration here then convert every one of them into the differential mode by introducing current sources or common emitter resistance.

In this particular case these differential configuration has been achieved by lifting this above ground and putting a common emitter resistance and also here or this can be connected to ground or in this particular case it has been connected to, here this is connected to plus, this has to be connected to minus.

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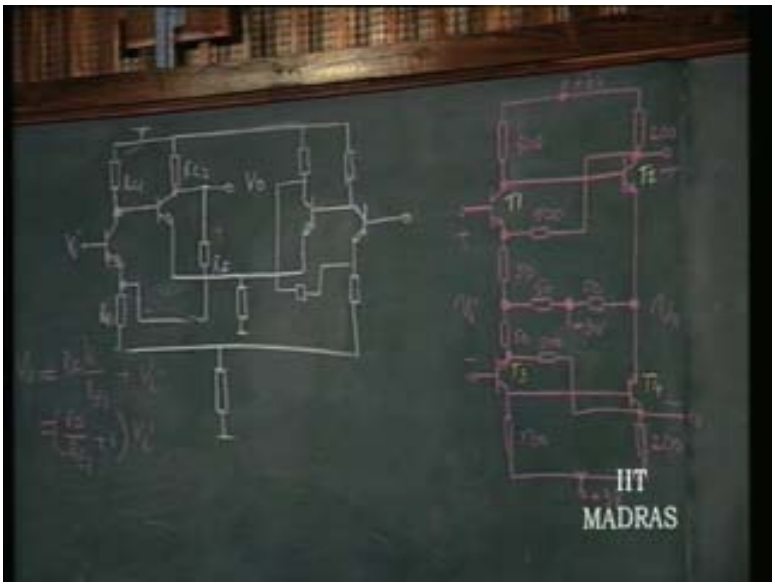

So this is the DC picture, you can see how the circuit gets transformed simply into an integrated circuit once you have the basic feedback configuration. If you see this configuration it is nothing but essentially this configuration. See how that can be synthesized simply by adopting the basic configuration and converting into differential mode by simply lifting the ground to a common point where the common emitter resistance or the current source is connected. And the current source in turn can be connected to negative or ground depending upon whether it is dual supply or single supply.

So this is the wide band IC which is making use of h feedback but what we will see when we design such a circuit is, invariably if it is designed well, if it is designed to have high loop gain it will go into resolution because all the three time constants; the input time constant, output time constant and the intermediate time constant become comparable to one another. Therefore in the region of interest all the three time constants come into picture causing instability for the negative feedback. Therefore, how to make it become stable without loosing bandwidth?

This is normally done unlike the case of op-amps and others where you are not so much bothered about the bandwidth where we are bothered about its used in low frequency configuration as operational amplifier for mathematical operations of addition, subtraction, integration, differentiation, etc. There it may be used in a variety of negative feedback configurations and therefore you would like to make it work for all negative feedback configurations so the compensation adopted is dominant pole compensation. What it means is, simply increase one of the three time constants so much that the gain reduces drastically within the frequency band that when actually other poles come into picture the gain has already fallen to a value less than y. So there is no question of the negative feedback turning itself into positive feedback at any cost. This is by drastically cutting down the bandwidth. This technique is not at all suitable for wide band amplifiers with negative feedback. The negative feedback should not be used if it is possible at all.

If you want to design wide band amplifiers we had seen those pairs where no negative feedback is used but it will do the maximum bandwidth and gain bandwidth product. But these are not such configurations. The single stage is one configuration where it is possible to sustain negative feedback without causing frequency instability. But this two stage configuration is not at all like that and invariably they go into oscillations.

Now how do you prevent oscillations?
To prevent oscillation here what is adopted is not dominant pole compensation, it is pole zero compensation. I will introduce a zero to cancel out one of the three poles but I should ideally introduce a 0 to cancel out one of the three poles so that it becomes a second order system. But in the process of doing it using a capacitor I cannot but introduce another pole. But this pole I am going to introduce is going to be coming into picture at a very high frequency so it is of no consequence. Therefore you can consider it for all practical purposes. That is, pole zero compensated amplifier is essentially a two pole configuration rather than three pole configuration. This is called pole zero compensation. And where do you introduce this zero? It is normally introduced, if you see the feedback resistance is nothing but R_F, the dominant pole compensation is called lag compensation.

What will you call the zero compensation?
It is the lead compensation. The pole zero compensation is obviously lead lag compensation as called by the other terminology. Therefore how do you introduce a capacitor? If you put a capacitor across R_E then it will result in lag compensation. There will be a lag between the fed back voltage and the output voltage. If you want this to lead slightly what will you do? You will introduce a capacitor across R_F. This is something which you have been calling as speed-up capacitor in the case of digital circuits. This will link the high frequency component very quickly with the feedback terminal. Therefore this is lead lag compensation. This is going to result in a pole. Now what is the pole? A simple way of finding out this pole is to find out what is the effective resistance across the capacitor that will gain.

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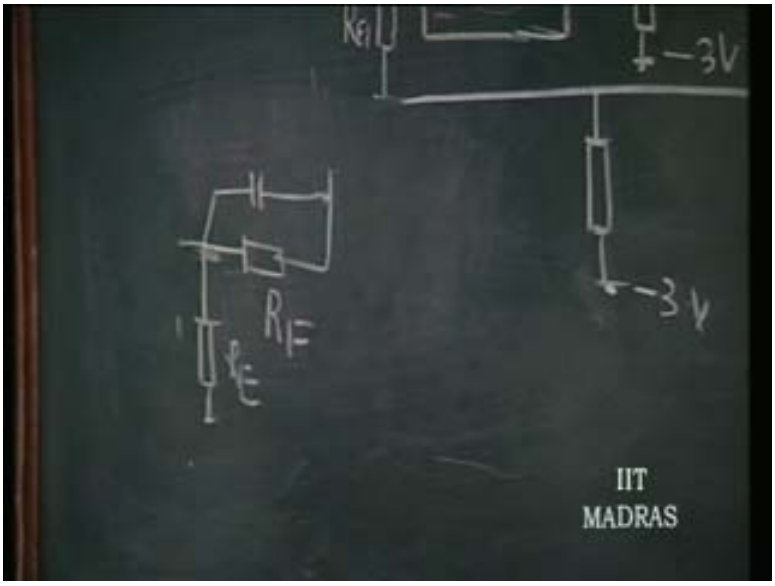

If you consider that this is driven by a voltage source the pole of that configuration can be simply found out by finding out the effective resistance across the capacitor. If this is C_F then it is C_F into R_F parallel R_E where will be the 0 located? It is also very clearly visible. It is the resistance that is directly across C_F that is R_F, R_F parallel C_F so you can locate the 0 at 1 by R_F parallel C_F, R_F parallel C_F is the time constant and cancel out one of the three poles. In the resulting configuration now we will have an additional pole coming into picture having a time constant which is C_F into R_F parallel R_{E1}.

Now R_F parallel R_{E1} can be made a low resistance, this is a load time constant and this can be located far away from the region of interest. If this facility is not so easy you can actually split R_F into R_{F1} and R_{F2}. R_{F1} plus R_{F2} being the actual R_F needed for the low frequency gain and R_{F1} is the one that you should locate the 0 at the appropriate point. This is what is provided externally by you and the [i……] [21:30] will not give this capacitor or even suggest it.

So what you normally do is you just put the value of capacitor that is needed to prevent oscillation. So, one way of doing it practically is, simply observe the output see whether it is going to oscillations to all conditions of supply voltage and temperature. If it is going into oscillation then increase the value of capacitor so that it is eliminated. Just put a little bit more than what is needed. This is a practical way of stabilizing this wide band amplifier and also obtaining the maximum possible bandwidth for your usage. This is the compensation normally adopted for this kind of configuration. The IC might give you trouble. The previous ICs we discussed about would never give you any trouble but we have to live with a low value of loop gain and consequently and somehow it is going to become sensitive to supply voltage and temperature variation.

We had just seen how h feedback circuit starting from fundamentals could be converted into useful IC with biasing etc is taken care of very well. Therefore the configuration we

have synthesized transforms itself into a very useful integrated circuit component wherein externally we might have to do some amount of fiddling with it in order to make it work for the optimum bandwidth. This is likely to be the tone set in hereafter because we are going to use two or three stages and complicate our life further. Therefore practical design of these circuits becomes pretty complicated.

Now, it does not mean that this kind of circuit can only be used in a differential configuration. If you are bent on it you can also use single supply with no differential configuration if you take [r….] to level shifting etc. This is another IC which is available. You can see that in this particular IC here a single supply is used and the bias voltage stabilization is secured by using three resistors just for biasing instead of the normal single resistor configuration.

You can see that this is another IC which is available which uses no differential configuration but uses level shifting straight away using a zener diode. Earlier this was grounded AC wise but now you are putting a zener diode so the collector potential of this is above the base potential so that is a small amount of reverse bias for this to operate. We might as well add a common collector stage before giving feedback so do not imagine that this is necessary. If you still want lower output impedance you can adopt this kind of a technique and using additional transistor is not going to be a problem in integrated circuit. In fact you can bias this separately by putting another resistance here so that it operates at a higher current.

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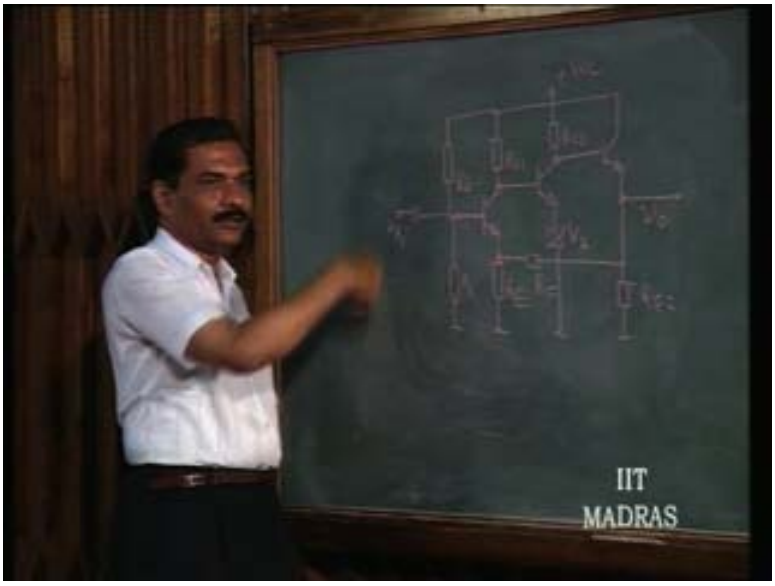

Analyze this and find out the input impedance, output impedance, loop gain assuming finite beta for the transistors. This is exactly similar to this structure but it uses a single supply. Now, what is the dual of this voltage controlled voltage source and current controlled current source?

What should be the kind of feedback we have to apply now?
It is g. So it is very simple to conceive this configuration.

Again we have the two stages cascaded. Now it should be g feedback, it will be shunt at the input and series at the output. You have the same thing R_F R_E but put it this way. This should result in an ideal current controlled current source or the parameter to be used here for analysis is g parameter. And g parameters simply add and the modified parameter is going to be the h parameter. And it is h_{21} which gets stabilized or becomes wide band and all the other h parameters will go towards 0 by the extent of the loop gain so all those things remain the same.

Obviously what will be the gain?
If this is the input current I_i and this is the output current I_0, I_i will now completely flow through R_F and a very little of it will flow through the base. So I_i will flow through this and this will be resulting in a voltage which is I_i into R_F and what will be the voltage across R_E? It is I_i into R_F. Therefore the current is going to be I_i into R_F by R_E flowing in this direction so I_0 is going to be equal to I_i plus I_i plus I_i into R_F by R_E or it is the same thing I_i into 1 plus R_F by R_E which is the same expression we had but the only thing is since we assumed I_0 to be flowing in here then this is going to be negative.

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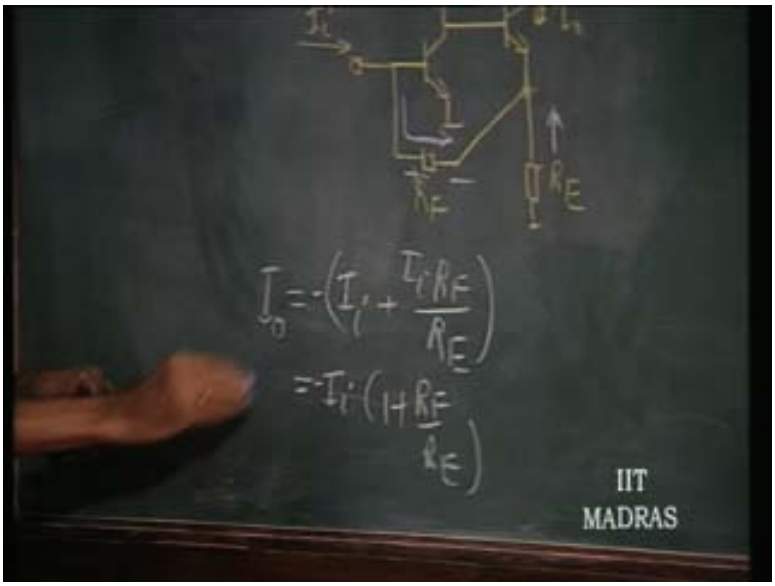

Therefore this is going to be the gain of the stage. It has exactly the identical method of analysis except that the voltage and current changes their role in this case. So 1 plus R_F by R_E is the current gain in this case. The input impedance gets reduced considerably by the extent of the loop gain. The output impedance gets enhanced considerably by the extent of the loop gain and the bandwidth improves by the loop gain. Analyze the circuit using spice as well as normal method of analysis that is g parameters assuming finite betas for the transistor. These two configurations are the cascaded configurations using two transistors.

Can we go to the three transistor configuration?
Now, by this time you must be totally aware of what should be done. It is a routine process now. What are the feedbacks that are valid? It is y and z the valid negative feedback configurations. And h and g will turn themselves into positive feedback configurations. Therefore again the problem of frequency compensation is severe in this case because how many time constants are there on a minimum? There will be four time constants to deal with, it may be of the same order of magnitude. Therefore it will definitely go into oscillation and we might have to take care of frequency compensation of the same type as discussed earlier. That is what is done; it is the ultimate thing that so far nobody has gone for a four stage cascading for wide band configuration.

At three stages they faced enough complications to stop and say they are now satisfied with the loop gain and also consequent desensitization of the amplified parameters with respect to the active device parameters. Therefore this is the point at which the design of IC wide band amplifiers has stopped and that is simply a three stage configuration.

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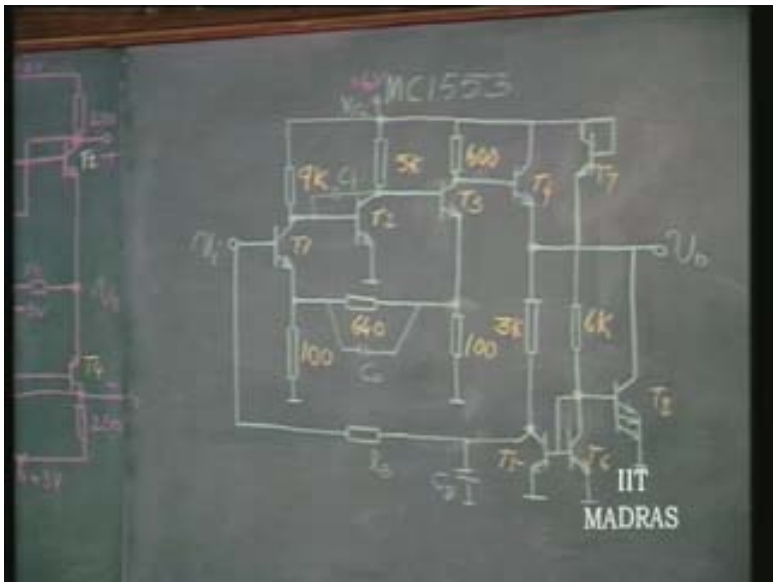

The three stages of cascade:
This discussion is equally well valid whether these are bipolar stages or fet stages.

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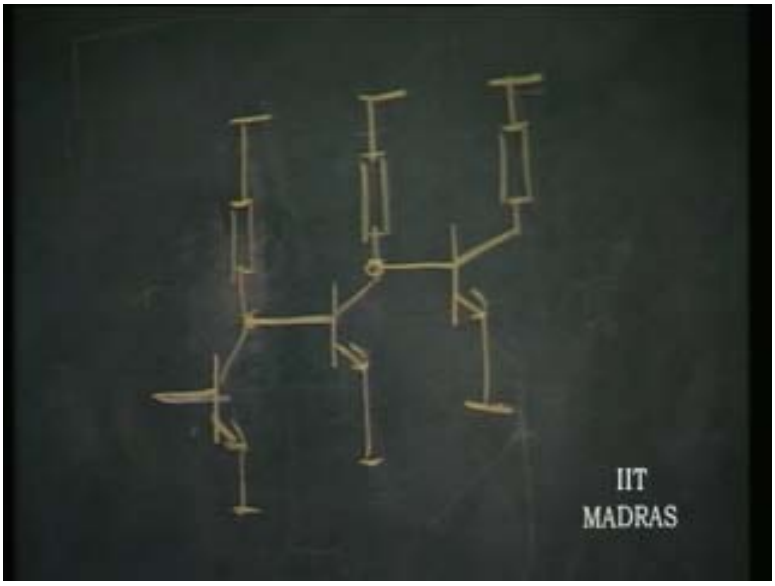

Here, what is adopted is y or z. The y feedback is pretty trivial because the arrangement is pretty simple. It says connect the output to the base through R_F. We can as well say this entire set of three stages can be now replaced by a single transistor and all these analysis. Therefore there is nothing brand new about this, the feedback, technique etc. So, the method of analysis is simple, it says use y parameters. Therefore the resulting configuration is going to turn itself into a current controlled voltage source ccvs an ideal ccvs. The method of analysis is using by y parameters and the modified parameters are the z parameters. The forward transfer parameter of importance is z_{21} and that is nothing but $- R_F$ in this case. So all those methods we have adopted when we discussed single stage structure is valid here also.

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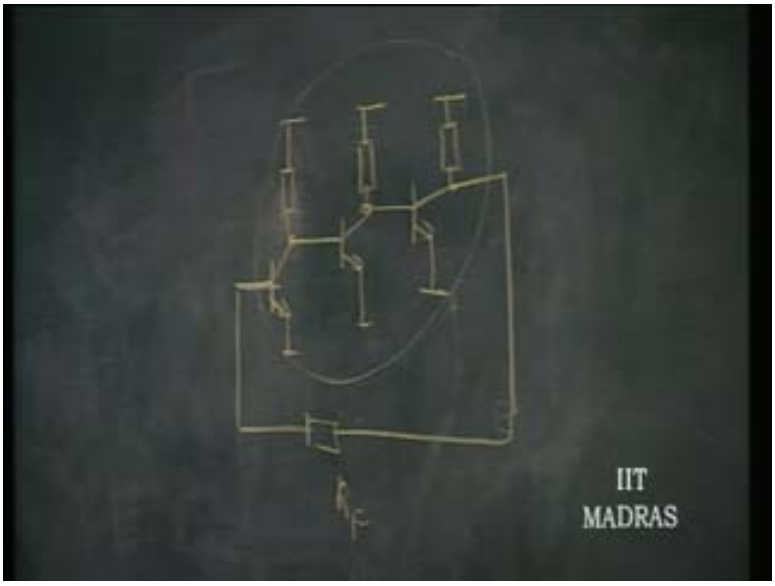

Now let us see the configuration the z feedback which is what is adopted in the ICMC 1553 wide band amplifier stage. So we would like to feed the voltage in series and sense the output current now. So, sensing is done by this resistance and a portion of it is fed back and converted into a voltage and the voltage comes in series. We can call this resistance as R_{E1}, this as R_{E2} and this as R_F. Input is a voltage V_i and output is a current I_0.

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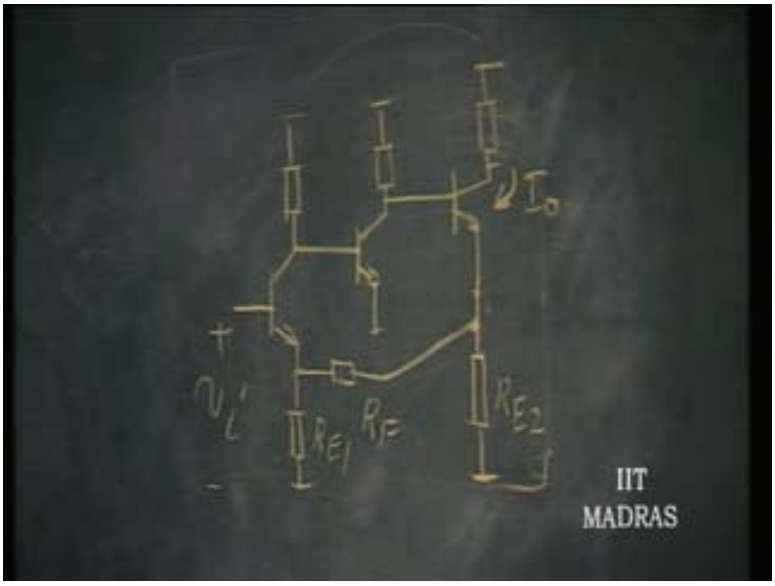

Therefore now we have a voltage controlled current source. Let us quickly do the analysis here to find out the trans-admittance which is the one that is stabilized or wide

banded. Therefore let us evaluate that. V_i comes almost entirely across R_{E1} so it results in a current of V_i by R_E. This current has to move totally through R_F and therefore the drop across this is V_i by R_{E1} into R_F plus V_i is the voltage across this R_{E2} and therefore current through that is divided by R_{E2}. That is, the current through this and current through this is already known V_i by R_{E1}. That is nothing but the total current and that is equal to I_0 or I_0 by V_i is nothing but 1 by R_{E1} plus 1 by R_{E2} plus R_F by R_{E1}. The input impedance is increased and the output impedance is increased by the extent of the loop gain and the forward transfer admittance is stabilized and wide banded. This particular thing is realized in the form of an IC here. Here, this is R_{E1}, this is R_{E2} and this is R_F.

So now you are aware of what this gain or the transfer admittance parameter is for this structure. These are the three transistors which are cascaded together and the output is connected only through a common collector stage which is operating at a pretty high current if you are taking it as a voltage. Strictly speaking this is a current, this current is converted into a voltage by making it come across the 600 Ohms and that voltage comes as such at the output with the load impedance. So this portion of the circuit is for biasing.

Using a single stage you would like to bias this structure, so how do you bias it?
This configuration is left as such because if it gives feedback for AC it will give feedback for DC also and therefore it is biased and is going to be automatically stabilized. As far as this is concerned this is the bias current which is going to be 6V minus 2V gamma by 6k is about 0.8 mA or so is the current flowing in this and that is reflected here as the current. So this current is almost totally reflected here but this current is going to very nearly equal to this current because this is going to deliver only the base current so there is almost no DC drop across this. This resistance is put essentially for isolating the input from the output.

As far as biasing is concerned there is a link of a DC voltage through this but we want to isolate the input and output so this resistance is put and it is bypassed by means of an external capacitor. This resistance is a large external capacitor. This terminal is brought out so that this capacitor can be put externally. So, this particular capacitor is to be put externally for bypassing this resistance.

In the case of an AC picture this is going to be of pretty high resistance so this will go out of picture and this current is essentially the same as this current. Therefore if this is 0.8 mA this is also 0.8 mA and therefore what is the potential at this point?

Let us assume the base to be 0.6 from ground and now what will be the potential of the collector here?
You will have to come back here, there is no potential drop here, there is V gamma here, there is very little drop across 100 ohms because this current is going to be very small, the drops across this is very small so this is roughly going to be 0.6. So we know that this is 0.6 and there is going to be a drop of 3K into 0.8 which is 2.4 and therefore output voltage cohescent value is 3V which is the centre of 0 and 6V so that you can get a fairly good output swing for this particular structure. You can see that this output quiescent is very nearly at 3V by this kind of arrangement here and you can evaluate the other DC

voltages and DC currents. This voltage is 0.6, this is 6 so you can find out the current in this. We also know that this potential is 3 so this is 3.6 so you know the current in this and that has the same current as this therefore you know the drop in this and you know the potential here that helps you to find out the current in this.

In any DC negative feedback structure like this once you know the potential at one point all the other potentials are going to be fixed with reference to that potential because it is a negative feedback. That means the negative feedback configuration has bias points also almost completely stabilized. As far as frequency compensation is concerned you can see the lead compensation here and there is a lack compensation put here, this is going to be resulting in some kind of dominant pole at this particular point so that this lead compensation also can work well. Therefore we have a dominant pole introduced here by introducing additional capacitor here. Again now you have to play with these two capacitors to achieve frequency stability. Therefore, again you see the amount of uncertainty involved.

With this we are putting an end to our discussion negative feedback wide amplifier configurations. There are several other structures which people have thought of. For example, there is a very interesting structure specifically used in a situation where you are interested in matching the input impedance with source impedance and matching the output impedance with the load impedance. In all these wide band structures we discussed so far the input impedance and output impedance will be increased by loop gain and the loop gain is highly sensitive to supply voltage variation and temperature. Suppose we are bothered about gain being stabilized as well as input impedance and output impedance being stabilized in a situation where we require perfect matching what should we do?

What is done in such a situation is a very interesting configuration which is pretty complicated when you try to analyze it but it looks very simple. Let us see that configuration. These are the cascaded structures where I am going to give you g feedback as well as h feedback where both are combined. So this is going to give you h feedback; R_{E1} R_F R_{E2} R_{F1} R_{F2} so R_{C1} R_{C2}. Analyze the circuit using spice. Analyze the circuit first with alpha being assumed to be very close to 1. Find out the input impedance and output impedance and voltage gain and current gain for this.

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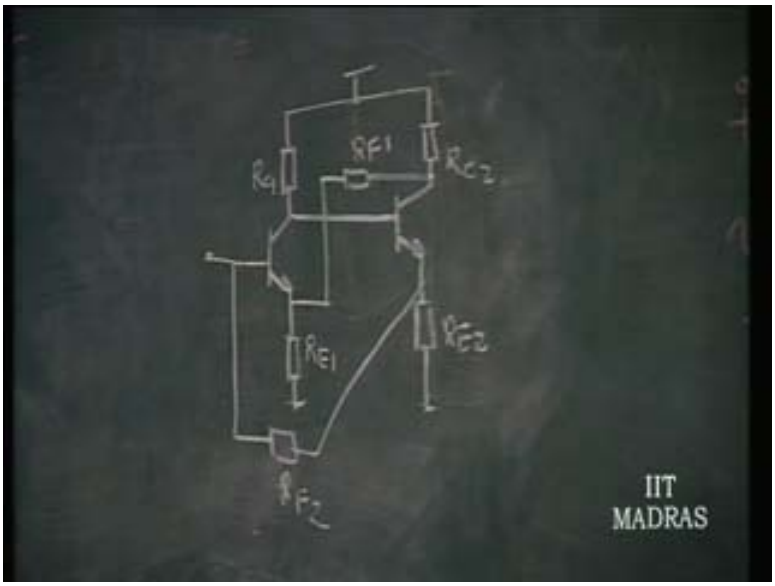

Both voltage gain and current gain are going to be stabilized. Apart from that input impedance and output impedance will be stabilized which can be made your 600 ohms or 50 ohms or whatever it is depending upon the diode you require. Analyze the structure using spice as well as your analytical tools.