Analog ICs
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Lecture - 5
Differential Amplifier
Characteristics and Parameters

In the last class we were discussing about the differential amplifier as a basic building block. We also saw how it can be thought of as being a stage which has been developed as an alternative to discrete circuit common emitter amplifier configuration with all sorts of bypass capacitors and coupling capacitors being removed altogether and being replaced by transistors and it results in a neat configuration which actually has better performance than the discrete common emitter stage in terms of being able to handle larger signal swing for the same percentage distortion and also the same gain as that of the discrete state.

Let us now see how this differential amplifier has certain non idealities associated with it and how the performance of this differential amplifier can be measured in terms of its parameters.

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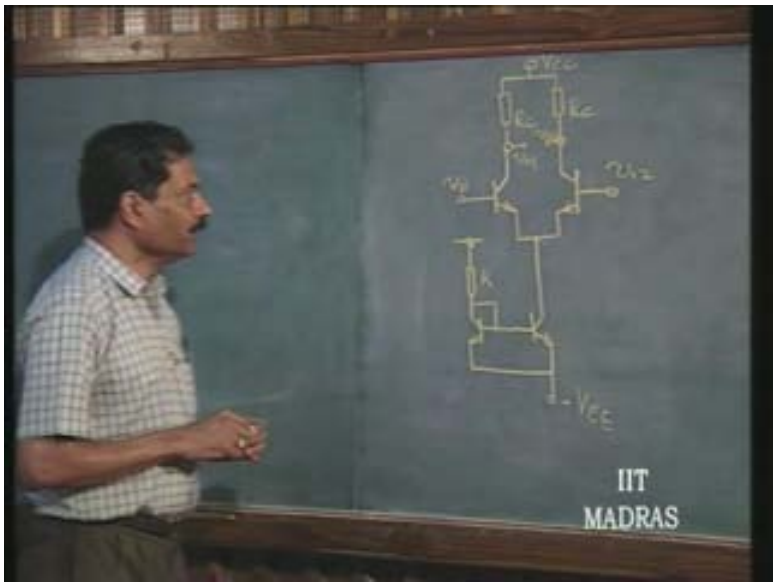

What are the parameters associated with the differential amplifier?

First one we said is the small signal parameter and in this case I have asked you to evaluate the signal level which is required to produce one percent distortion at the output. And we will note that it will be of the order of few vts. So it is dependent upon V_T which is 25 mV. Therefore if the signal level is small where the performance of the differential

amplifier can be approximated as being linear then the input impedance of the differential amplifier for the differential mode signal is going to be 2re into hfe plus 1. And re being equal to $2V_T$ by I_0 by 2 where I_0 is the source current and I_0 by 2 will be the quiescent current to each of the transistors T_1 and T_2. So this is equal to $4V_T$ by I_0 into hfe plus 1, this is one of the design parameters.

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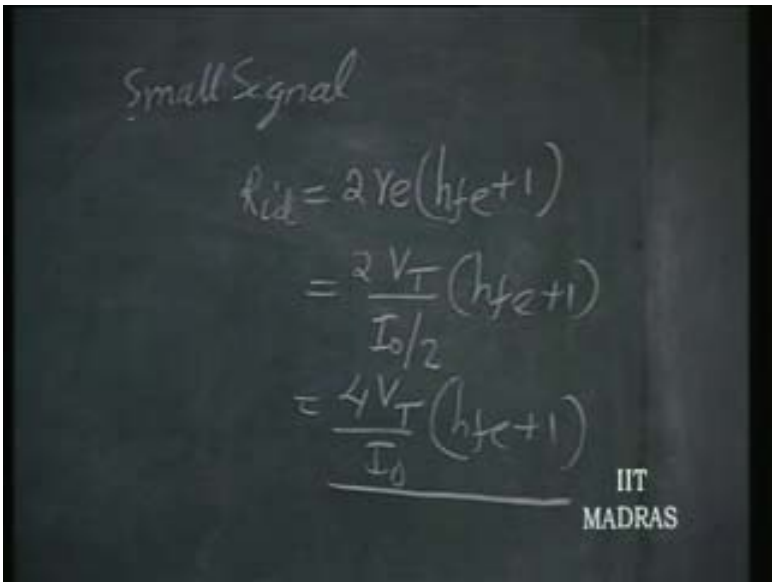

You might be required to design these as an input stage at which point of time you would like to know what the input impedance of this stage is. As I pointed out, the input stage has the primarily responsibility of taking care of input impedance. The priority that should give in terms of parameters of the differential amplifier itself differs depending upon where exactly you are using the differential amplifier. So in this case input impedance is a very important small signal parameter. Then we have the differential mode gain of the stage is equal to gm into R_c. This is the differential mode output to differential mode input which is strictly speaking V_{01} by V_{02} by V_{i1} minus V_{i2} is equal to minus gm into R_c, this is what we have shown last time.

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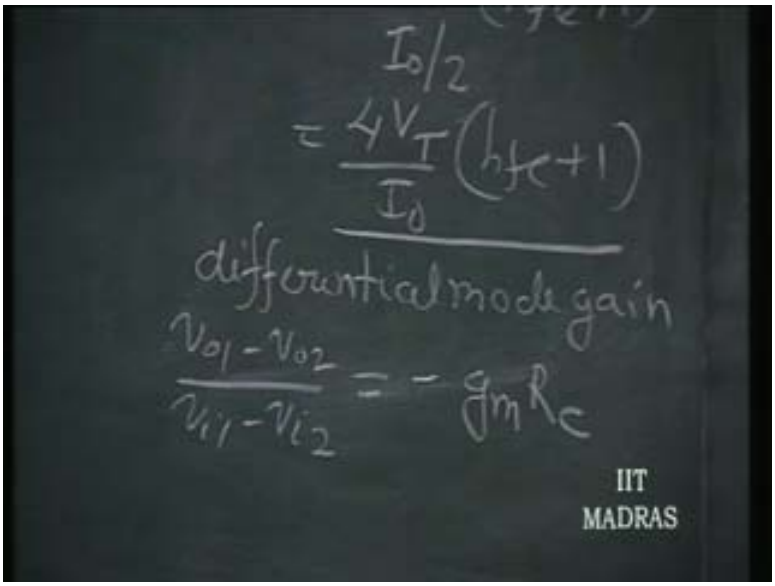

And this is going to be equal to, again gm is the operating current I_0 by 2 by V_T and that into R_c is equal to minus I_0 R_c by $2V_T$. I am writing this in terms of the operating current and other well known parameters so that given the operating current you quickly get a picture of what the input impedance is and what the gain is straight away.

Now we must also know something about the output swing. Suppose it is not used at the input stage of an amplifier it is used as an output stage itself then the output swing becomes important. If it is used as an input stage of an op-amp then input swing and output swing are all going to be very small. It is going to handle signals of the order of micro volts even if the gain is 100 the output swing is going to be of the order of hundreds of micro volts. Therefore please remember that when the differential amplifier is being used as an input stage the output swing is of no consequence.

Subsequently one might for operational reasons even operate the input stage at very near saturation. There are instances where the transistor is on the verge of saturation for certain reasons wherein the swing is very small. It remains in the active region even though it is on the verge of saturation. For the output swing problem as far as the input stage is concerned if of no consequence. But swing problem is a serious thing only when you consider the differential amplifier coming as an output stage. So, in such a situation the output swing is equal to, how much? This also we had evaluated earlier, this I_0R_c comes either through this or through this at which point of time one of the transistors is off that means the swing is plus minus I_0R_C as long as the transistors themselves do not go to saturation. The entire switching occurs due to current being switched from one transistor to another. These are the things we discussed in detail in the previous class.

As long as the transistors are not going to saturation it is independent of supply voltage. The supply voltage question comes into picture only when limitation occurs because the transistors are going to saturation. That is why you can actually design it for a given swing as far as this stage is being used as an output stage.

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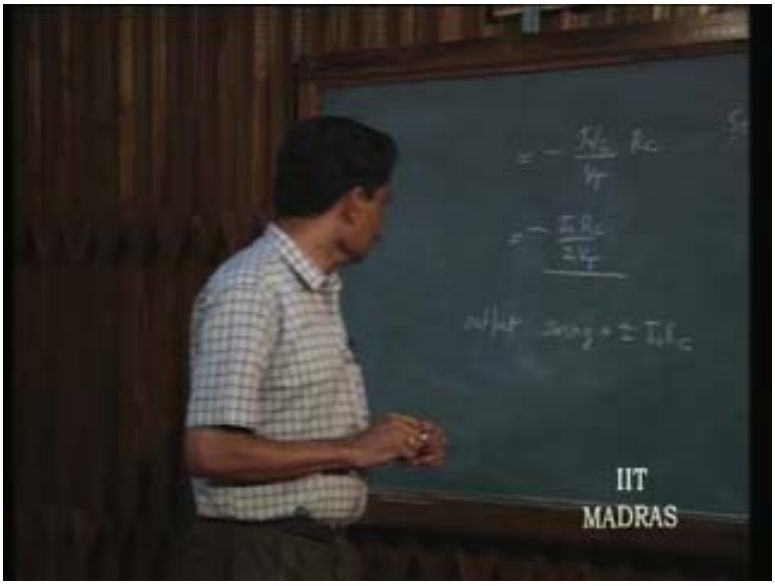

Now let us further discuss about other small signal properties which we have sort of postponed to this class.

This particular thing when it is having no differential mode signal and when it is having only common mode signal both the inputs are connected together to the same voltage. This situation arises in a trouble some manner because if you do not want to bring trouble unnecessarily, when this input stage is being used without feedback you will not unnecessarily cause common mode problem to you. You will always try to eliminate any problem, where will it come without you are asking for it. It is going to be appearing in a negative feedback situation in the worst case of common mode travel that occurs in unity gain mode of operation.

The common mode signal situation, if this is V_i this is going to be V_0 and the entire output voltage is fed back. So what is the common mode voltage of unity gain amplifier? It is V_i itself. And you would like V_i when this is acting as a buffer stage to go as much as V_{cc} itself in any practical situation. That means the input common mode swing capability of an input stage which is being used in an operational amplifier is constraint to operate in this mode as long as you are going to use it as unity gain amplifier, this problem is very serious. If you say that I will never use this amplifier in unity gain mode where it is least seen here where there is no common mode?

Open loop is a situation that there is no feedback. So unnecessarily you are not going to bring in any common mode problem for yourself where there is an application where it automatically comes in but comes in less severely than this. You should know this because in an inverting mode of operation where one end is connected to ground the other end is automatically at virtual ground so the common mode voltage input to the op-amp is 0, very nearly 0. Therefore if you have a common mode problem with any op-amp you should use it only in inverting state.

If you want any op-amp to be chosen for being used as a buffer state then make sure that there is a known common mode problem. If the input stage is designed like the input stage is likely to go to saturation and you are going to use it in this configuration then the problem of latch up is going to occur. It happens when this so called negative feed back itself turns into positive feedback because of the signal and thereafter it refuses to come out of positive feedback situation.

These are clear examples where you as design engineer should know how to design an op-amp given its application, where is it going to be most likely to be used. If it is going to be a general purpose op-amp which is going to be used in any mode then you would design it for the worst case. And the worst case is the maximum negative feedback situation that is called the buffer state.

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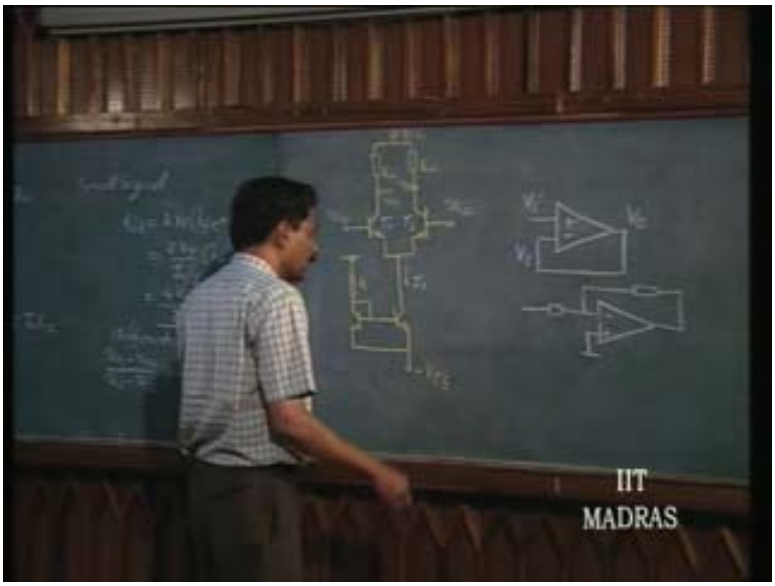

Now, as far as common mode swing is concerned the input common mode swing is an important criteria. The output common mode swing is going to be negligibly small, we are not bothered about that. So, as far as the input common mode swing is concerned it is going to be governed by the amount of DC drop that is occurring in R_c. We will go in for an active device or a current mirror as below because this potential is V_{cc} minus I_0 by $2R_c$ even when the common mode signal is present and it is varying is going to remain at that. Therefore we are driving these transistors to saturation just by common mode signal even though it is not clearly getting affected by the differential mode at that point of time.

Just the common mode signal alone can drive it to saturation and create the problem of latch up. That is why we said you will replace these by active device. This is what we introduced last time as the current mirror that was low.

Today we will see how the swing here goes almost up to V_{cc} minus V gamma on this side and also almost to the negative supply voltage minus V_{EE} plus V gamma plus one more V

gamma and up to that it can swing as far as the input common mode swing capability of the transistor stage is concerned. That means it is almost up to plus V_{cc} on one side and minus V_{EE} on the other side after you replace it by means of a current mirror. Let us see the consequence of this on the gain. The gain we are now going to talk about is again the differential mode gain. Does it get disturbed because of this kind of a load?

Please remember here that this is not the same as two equal resistors. I am putting a current mirror here so the current in this i and the current in this will always remain the same. Even when the signal comes it should not get disturbed. So what happens is, when I apply a differential mode signal to the input this Vid by $2r_e$ is going to be the incremental current in this emitter so the current here is going to be I_0 by 2 plus Vid by $2r_e$ and this current is I_{02} minus Vid by 2.

What will be the current in this? It will be very nearly same except for alpha, alpha times will flow through this. Alpha is very close to 1. So this current is going to be very nearly same as this current. What is this current? It is same as this current. That means we have a current here which is I_0 by 2 minus Vid by 2re and this current is I_0 by 2 because of the current mirror action plus Vid by 2Ve. So what happens now is the current has to come out of the output terminal into the next stage as you want. Why did you use the current source as the load? It was because you wanted the entire output current to signal current to go into the next stage. Therefore it is serving that purpose and what is that current that is being injected out? It is Vid by re.

What has happened? This is with reference to ground. If you now connect a load across this which is R_c the output voltage will be Vid by re into R_c or gm into R_c that means you are taking back the single ended output and you are getting back the differential gain output as the single ended output. This is a method of converting the so called differential output into single ended output. So, using a current mirror has resulted in not only improvement in the common mode swing capability but also has resulted in the differential output getting converted into single ended output. This is an important advantage of using current mirror. That means now the output can be taken with respect to one collector and ground and you will get the same gain as previous gain.

We had noticed how replacing the two resistors by means of a current mirror has resulted in a gain which is the same as that of the earlier differential mode gain but with reference to ground you are now taking the output from one collector. Now please remember that you are connecting the normally the next stage which may be the another differential stage if you are taking it as a differential output you have to connect another differential stage from here so as to exploit the full gain whereas if you had replaced it by means of a current mirror you can take it out of only one collector, and that is the only high impedance point and the other portion which is nothing but the diode is a low impedance point. So the only one high impedance point exists in the case of a current mirror that is the other collector.

As far as the gain itself is concerned it is not infinity. The current source impedance will be coming as the load impedance apart from the input impedance of the next stage.

Actually speaking, in a practical situation the current source impedance will be replacing R_c as well as the input impedance of the next stage, these two will come in parallel. Now, as far as this particular stage is concerned we can replace this portion of the circuit by means of this dynamic impedance. The current source at the dynamic impedance will be Rd. So the AC picture of this stage will look like this, this is grounded, this R_c may be the actual resistance or it could be the output impedance of the current mirror as well as the input impedance of the next stage taken together. So this is the AC picture. Let us consider this stage.

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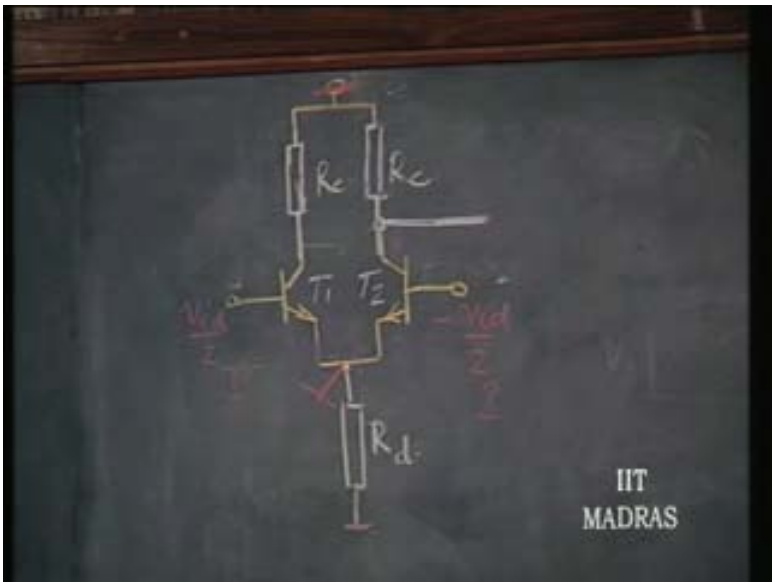

I would want all of you to view the differential amplifier in a slightly different manner.

Now it is the same analysis. When the input here is Vid by 2 and this is minus Vid by 2 the common mode voltage is 0. That means signal applied is only differential mode. This is a perfectly symmetric circuit and therefore the potential at this point which is the common point in this matrix is going to be 0 at all times. So, because of symmetry I can say that this point is going to be at all times at zero potential in which case I can as well say that this is grounded only if it is purely differential and not if it is having common mode as well as differential mode coming in. That means whatever increase in potential arises out of the incremental current injected here will be removed by the current flowing in the opposite direction through the same impedance. So essentially mutual cancellation occurs and therefore potential does not change which means I can ground the incremental picture.

Any differential stage for analysis purpose, for differential mode analysis you can simplify it considerably by simply grounding this point for the differential mode analysis in which case you can see that the gain is going to be R_c by re here and re itself is going to be governed by I_0 by 2. It is R_c by re here and R_c by re here. The phase shift is because of the shifting of this here as we assumed. This will be out of phase with this by 180

degree that is the signal we have seen. This is the analysis that we can adopt for differential mode. Anyway there is nothing new about it.

You have already learnt about the differential mode gain. Now let us see what happens for the common mode. When the signal is only common mode V_c V_{ic}, V_{ic} is still symmetric, what happens? The signal here is going to be very nearly V_{ic} except for a small drop in re. So this potential is going to almost nearly follow this potential of V_{ic}. That means the incremental change here is going to be very nearly equal to V_{ic} by R_d except for the small drop I have ignored through re.

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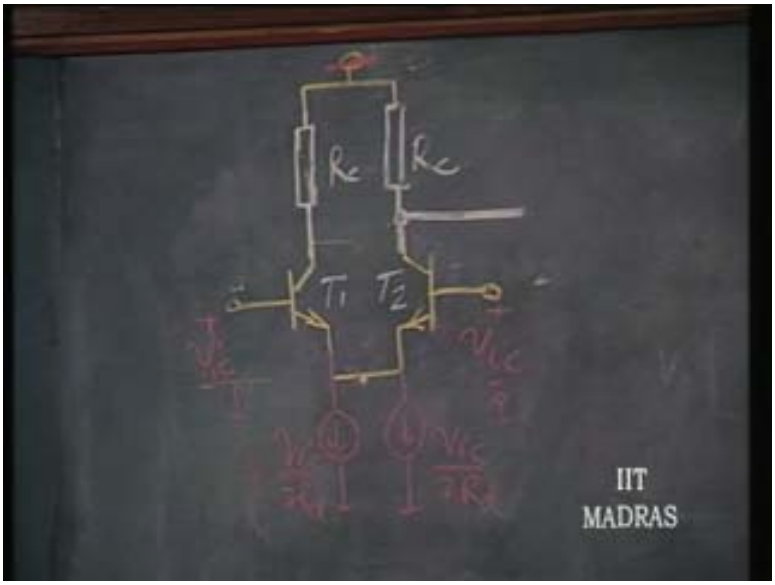

This means I can consider that it is V_{ic} by $2R_d$ and V_{ic} by $2R_d$ two current sources flowing that way summing up to V_{ic} by R_d. That means now you can see which one is V_{ic} by R_d.

Now there is no current going to flow through this link at any time because the potentials will remain the same at all times so I can as well break it open. That means, for the common mode operation I can have the circuits split up as what is V_{ic} by $2R_d$ equivalent to, V_{ic} is the drop across the current source then V_{ic} by $2R_d$ is the current through it, that means it is equivalent to a resistance of $2R_d$ and this also a resistance of $2R_d$.

For common mode signal now let us see what happens. What is the input impedance for common mode? Input impedance is R_2 R_d plus re so $2R_d$ plus re which can be ignored anyway into hfe plus 1. This is also mentioned by the manufacturer. For any differential stage you will also give input impedance for differential mode and input impedance for common mode, this has to be very high. It is very high particularly by using a current source there or sink. We are simulating very high impedance for it. Then what is the gain?

This is the current, now what is the emitter current? It is Vid by $2R_d$ plus re that is the incremental emitter current and what is the incremental output voltage now? It is into R_c so the equation is Vid R_c by $2R_d$ plus r_e. So that single ended common mode gain is going to be nothing but R_c by $2R_d$. So this is nothing but the common mode output voltage. So, common mode gain is going to be equal to R_c by $2R_d$.

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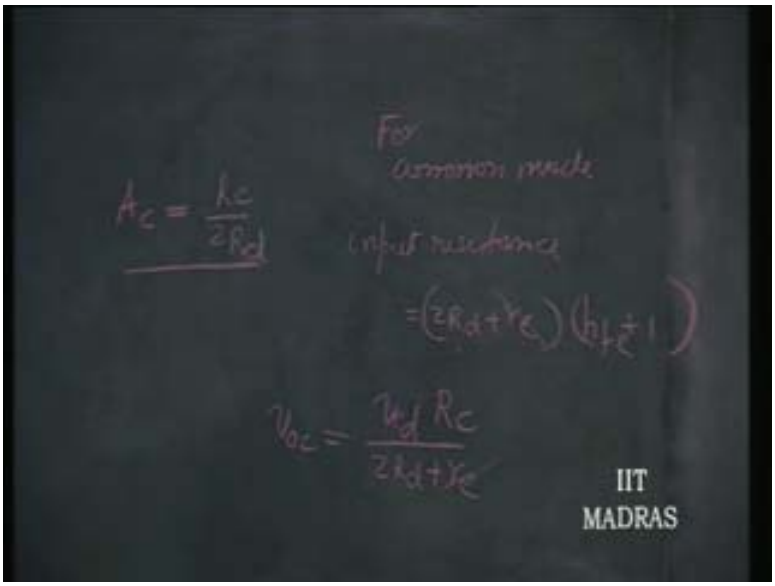

Now, if you take the differential output this output voltage will be in phase with this output voltage for common mode signal so the differential output will be still zero. But for a measure of common mode output voltage therefore it is advisable to use single ended output in the case of a differential amplifier. So, if these output themselves are very small, if Voc itself is very small compared to the differential output due to differential mode signal then making this equal and getting it cancelled is an easier fact. So a measure of how good the differential amplifier is will be determined by finding out the ratio between what the differential mode gain and the common mode gain for single ended output. The entire differential mode of operation has come about not due to output at all but only due to input arrangement of having a current source here which is responsible for the differential mode.

How you are connecting, what at the output is of no consequence. The rejection property for the differential amplifier has come about because of using a current source at the input point of the stage because you can see that both common mode gain as well as differential mode gain will be dependent upon, what is differential mode gain? It is R_c by 2re so it will get cancelled. If you take the common mode rejection ratio it is nothing but Ad by Ac and it is independent of what I am connecting in the collector because the rejection property is due to the current sink that I am feeding in the common point of emitters. So R_c R_c gets cancelled, it is purely a property which is dependent upon R_d and re. So it is R_d by re and what is re again, it is R_d by V_T by I_0 by 2. Now we have

quantified every one of the small signal parameters associated with the differential amplifier in terms of the load resistances as well as operating current including its frame.

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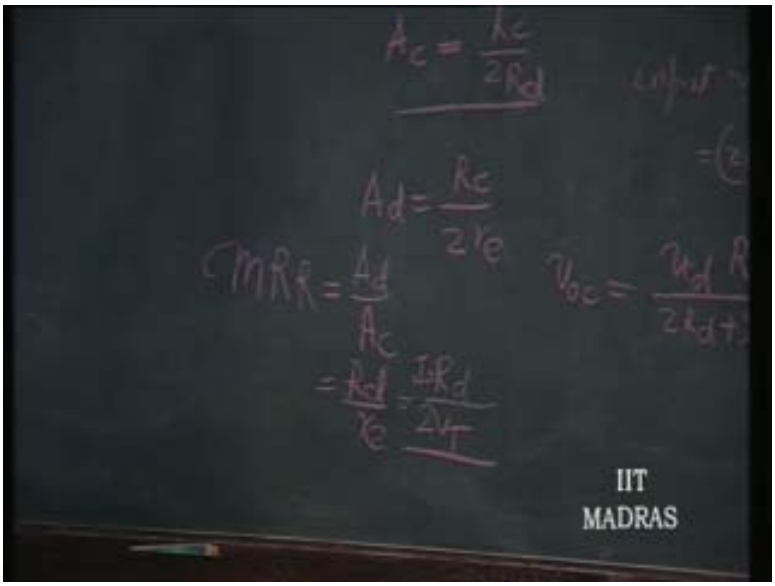

Now you can design depending upon where it is going to be used, is it going to be used as input stage of an op-amp or is it going to be used in a video amplifier where the stage itself has the responsibility of input and output. Then the output swing is also going to count. The signal may have been already amplified sufficiently large. So, the differential amplifier may be used as a power driver stage. Therefore depending upon that you have to decide what is the parameter that should become important.

Obviously in the input stage the important parameters are input impedance that is differential mode, input impedance common mode and that itself will take care of common mode rejection ratio. If you take care of input impedance that itself will take care of common mode rejection ratio and gain is of no consequence. You can forget about it because CMRR is independent of what you are connecting at load. This is what you should consider when it is being used as an input stage. As far as the last signal property is concerned, once again common mode swing at the input and differential mode swing at the output is nothing but I_0 into R_c and the relationship between V_{id} and V_{0d} which is nothing but tan hyperbolic function. These are the things you have to remember in the case of any differential amplifier. The same thing is applicable when the differential amplifier is MOS based or JFET based except that the relationship is not hyperbolic it is square law if you use a resistive load. But again if you use a MOSFET itself as the load then again it becomes linear over a certain range.

Try the same kind of analysis for MOSFET differential amplifier using resistance as the load and see what kind of relationship occurs between output V_{0d} and input V_{id}. Rest of the discussions regarding common mode rejection ratio etc remain the same. So far we were discussing about small signal properties as well as large signal properties of the

basic differential amplifier. Now we will go to the secondary property of the differential amplifier which is also important when we use this in particularly low frequency or DC amplifier stages in the so called video amplifier stages itself.

What we are now going to discuss will be primarily to do with output offset voltages. In any amplifier the output is a function of input. That is generally the property of any amplifier, it is some general function. We would like this function to be a factor independent of V_i which is a voltage called the offset voltage. So, in any amplifier in whatever form of biasing you use it will have this kind of property which is function of V_i and the factor independent of V_i is always called the offset voltage plus A times V_i, linear dependency and non vi square factor, vi cube factor and all these.

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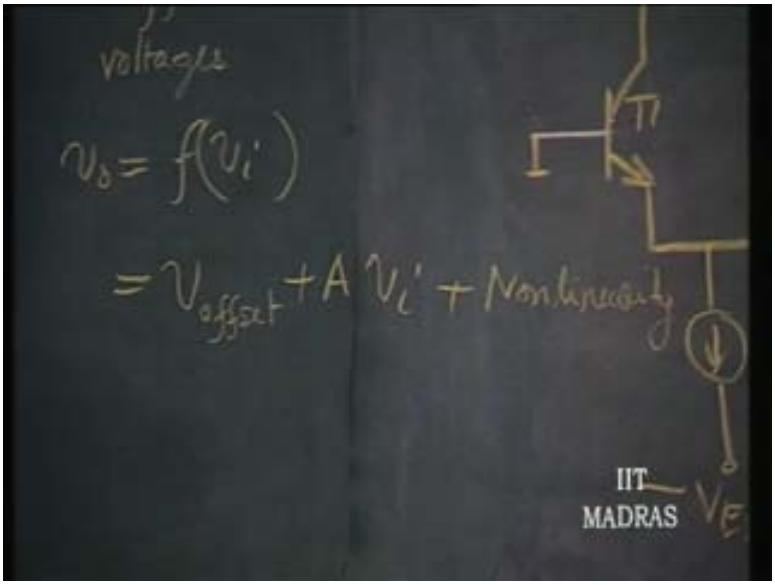

These are non linear, the output due to non linearity, V_i square V_i cube etc. So we are biasing the op-amp for the differential amplifier in such a manner that these terms are made very small for a given value, that is why biasing becomes important. Apart from that we would like to make the offset also go to 0 because the ΔV_0 by Δ time is going to be ΔV offset by Δt obviously it will also depend upon ΔV_i by Δt etc. This has been made 0. We are discussing the situation where these two exist. In such a situation ΔV_0 by Δt is called the drift.

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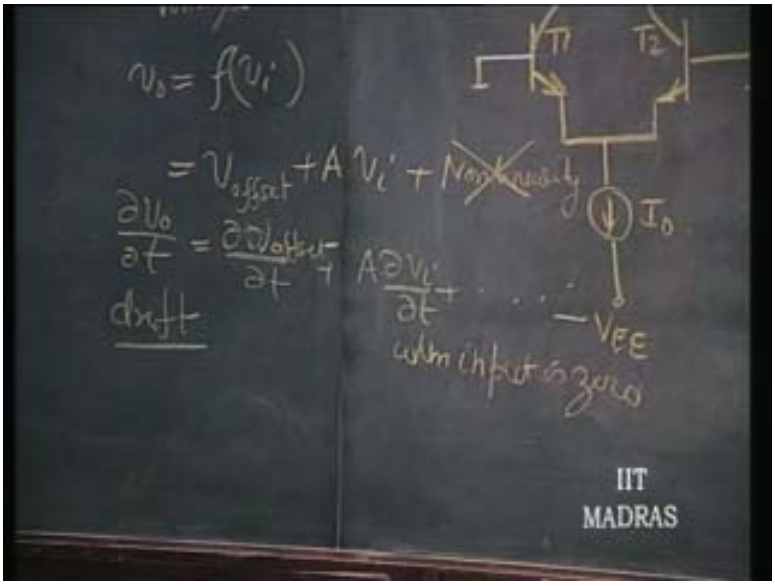

Even if when input is 0 the output drifts because V offset is changing with respect to time and that itself is going to get mixed up because we cannot make a distinction between this which is changing with respect to time which we want to sense and this, these are mixed up. This is the case if we are not able to isolate this. Drift is a very low frequency phenomenon. Therefore, if our signal itself is a low frequency thing we are unable to separate this. If the signal is a high frequency signal then we can separate out the drift component by using a decoupling capacitor

But when the signal is low frequency particularly in the case of video amplifier or bio medical amplifiers there it becomes important that I should make this offset as small as possible. That is the reason offset is made, what is causing you trouble is not the offset itself. What is causing you trouble is the dependence of offset voltage on temperature, time. It depends upon temperature it depends upon operating voltage etcetera and therefore with respect to time it keeps drifting and that is causing a problem. So this has to be eliminated particularly in situations where you are designing high gain amplifiers. This might drift the output quiescent point to such an extent that the operating point goes to non linear regions and the linearity itself or the gain itself gets reduced, this also is a danger. Therefore offset has to be reduced considerably.

So how do we therefore measure this offset? How to therefore come out with the design parameter so that we can say this differential amplifier or the op-amp is better than another differential amplifier? That measure is another important parameter associated with op amps or differential amplifier. So we will come out with what is called as input offset because input offset is the one which is causing major problem because input offset voltage is going to be amplified by the entire gain and is going to appear as output offset. Therefore the danger is the input offset itself. If the input offset is in common mode then it is automatically rejected, that is the purpose of using differential amplifier.

Can it become differential mode?
It is not in our hand. Therefore if it is becomes differential then the danger exists. Now you have understood that input offset can result due to the difference in V_T voltages, what is this?
If the input is 0 these V_{bs} are the same. If these V_{bs} are the same what will be the emitter current here? It is I_{E1} and I_{E2}.

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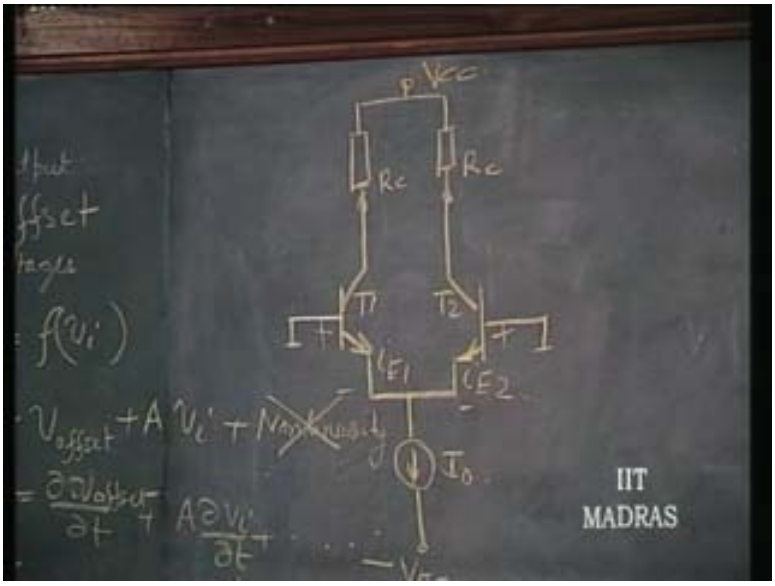

I_{E1} is equal to I_{E0} exponent V_{BE} by V_T. And I_{E2} is going to be equal to I_{E0} exponent V_{BE} by V_T these are going to be same. So, even if V_{BE} changes with respect to temperature this will remain the same and that is of no problem. This is what is called common mode problem. V_{BE} changes with respect to temperature but these currents will remain the same, now the value is going to be I_0 by 2 because I_{E1} is equal to I_{E2} and it is going to be equal to I_0 by 2 by Kirchoff's law and therefore output offset is going to be 0. But when will output offset come into the picture? It is when I_{E1} is different from I_{E2} and that can only arise when I_{E01} is different from I_{E02} that the two transistors are not exactly matched. If the two transistors are not exactly matched I_{E1} and I_{E2} for the same V_{BEs} will be different.

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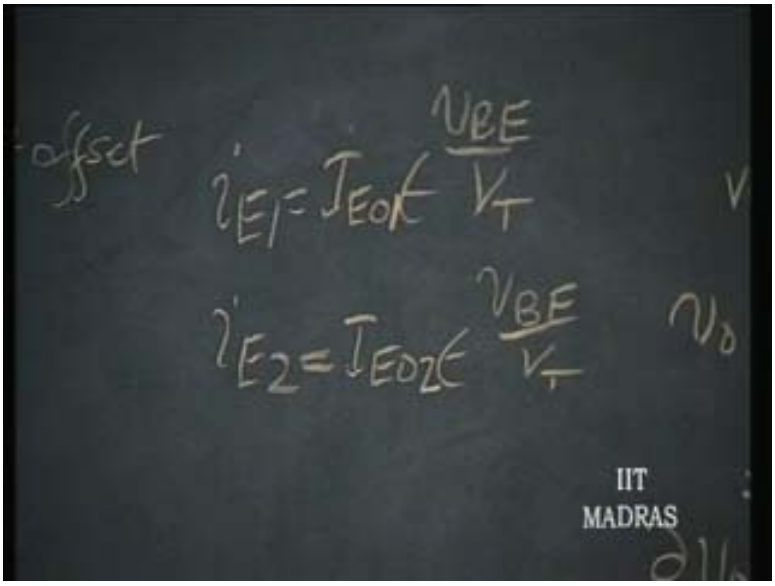

Then there is going to be an output offset voltage because of this. So what is it that causes the output offset voltage? It is the difference in the two transistors and that is resulting in equivalent differential mode signal. Let us see what that differential mode signal is. Input offset therefore is defined as that voltage I have to apply at the input in order to make I_{E1} is equal to I_{E2}. The input offset therefore is that voltage that I have to apply at the input to cause I_{E1} to be equal to I_{E2} that will be then equal to I_0 by 2.

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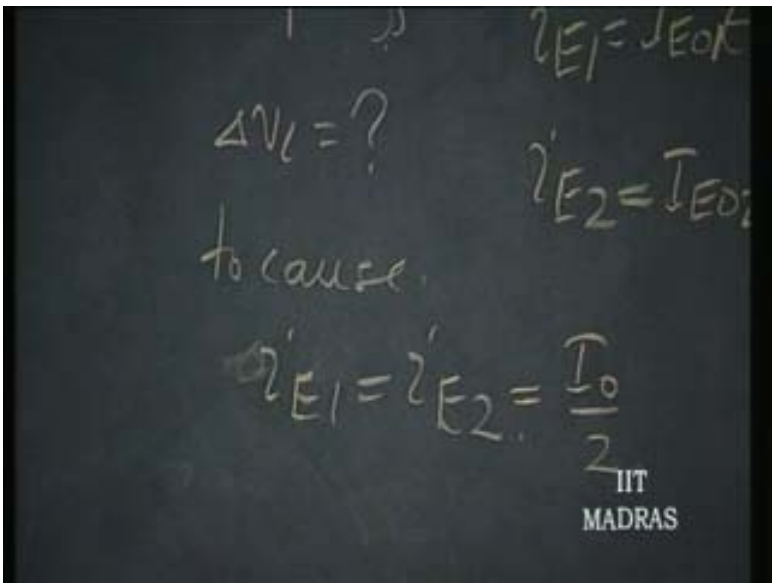

What is the input voltage? I have to apply ΔV_{BE} ΔV_i at the input. In order to cause I_{E1} is equal to I_{E2} artificially and that is what is called as input offset, how do you know that?

You can now find out if I_{E1} is equal to I_{E2} I have made then that is equal to I_0 by 2 then I take the ratio of this and what you get? V_{BE1} has got to be different from V_{BE2} that means V_{BE1} minus V_{BE2} is going to be ΔV_i in that loop, ΔV_i is nothing but V_{BE1} minus V_{BE2} and that is nothing but, take the ratio V_T log I_{E02} by I_{E01}.

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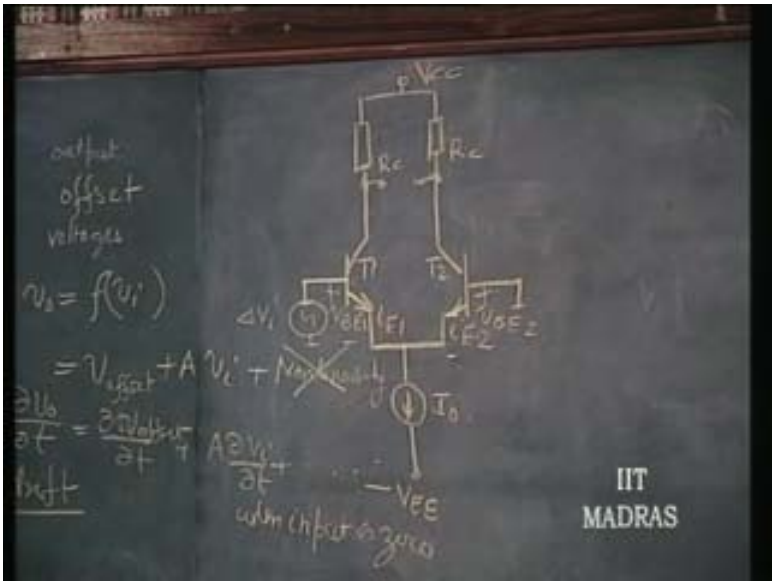

Take the ratio here, the currents are equal so this becomes one I_{E02} by I_{E01} is equal to exponent V_{BE1} minus V_{BE2} by V_T and so it is V_T log. Therefore, by the manufacturer this is defined as the input offset because only manufacturer has to tell you what it is. It depends upon the transistor mismatch. Typically for the technology that exists today for the bipolar transistor this is ranging between 1 to 2 mV. So this is coming because I_{E02} is not exactly equal to I_{E01}. This is not very nearly equal to 1 and that is why this logarithmic factor is going to be a small factor and V_T itself is 25 mV. So some factor of about one tenth will come out of it and therefore you get 1 to 2 mV as the natural uncertainty about this.

If we use one pair this is the input offset. If you use two pairs each of the pairs will result in 1 to 2 mV of uncertainty. So uncertainty will keep on multiplying with the number of pairs. So please remember this, in your design for whatever reason you increase more pairs, darling pairs or Darlington pairs, why do you use Darlington pairs? It is because you want to improve the input impedance of the input stage then you might go for Darlington pairs. So, when the input impedance is increased automatically you are sacrificing input offset. This is the practical situation that exists.

In the case of a MOSFET for example, differential amplifier what is the uncertainty due to?

Here V_{BE} is of the order of 0.6 or so and it is 0.6 for the same current that means 0.6 here and 0.6 here, it is uncertainty in 0.5 to 0.6 whereas in the case of a MOSFET it may be

some 1 to 2V so the uncertainty and magnitude also increases, it in fact increases by an order of magnitude. It will be of the order of 10 to 20 mV that is uncertainty in VGS. For obtaining the same current the uncertainty in VGS is going to be one order of magnitude higher than in the case of a bipolar transistor that is for the MOSFET.

So, please remember, if it is input offset that is the choice for the input stage then MOSFETs are out of question as input stage and you would rather prefer bipolar stage. But MOSFET has given you the highest input impedance that can be given. So always remember that input impedance if you are concerned about you have to sacrifice input offset, this is the primary idea behind selecting input stage. If you want low input offset go for low input impedance, you cannot hype it. This is what is called as input offset.

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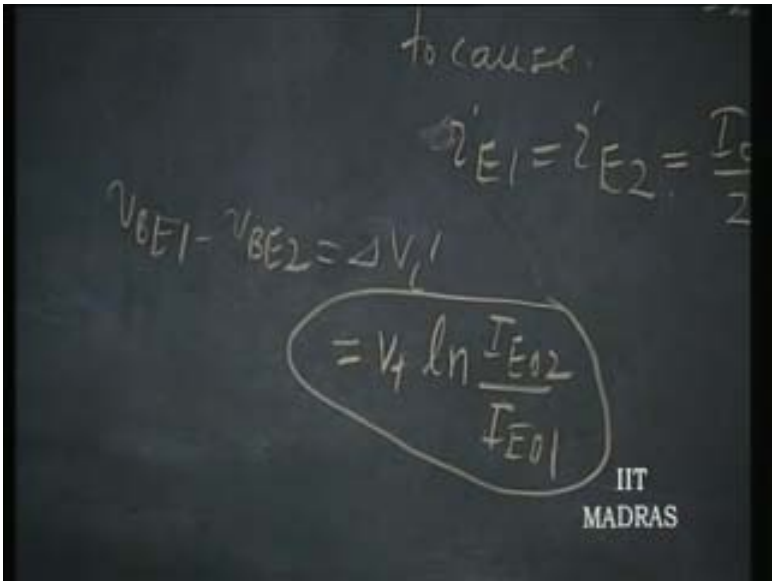

Apart from that input offset we have other offset problems also, why? This particular stage may not be just grounded, you are connecting an input source here. When the signal of the source itself is 0 that impedance R_S is always coming into picture. Since there is a base current flowing in this which is I_{B1} this base current I_{B1} into R_S itself will act as an offset voltage, this is called bias current offset. That is coming into picture only you are having source which is having high source impedance connected to the input.

One way to tackle that easily is to connect another R_S that solves your problem partially because unfortunately even if the transistors are very well matched the betas need not be exactly same and i_{B1} and i_{B2} may be different. So even if you put equal resistors there may be therefore a resultant offset voltage which is due to i_{B1} minus i_{B2} being not equal to 0 for the same emitter current. This is defined as bias current offset. This again is not present in the case of MOSFET. Hence, in the bipolar stage you have apart from ΔV_{BE} offset you have bias current offset also. This has worst case situations which means you have to add these voltages always.

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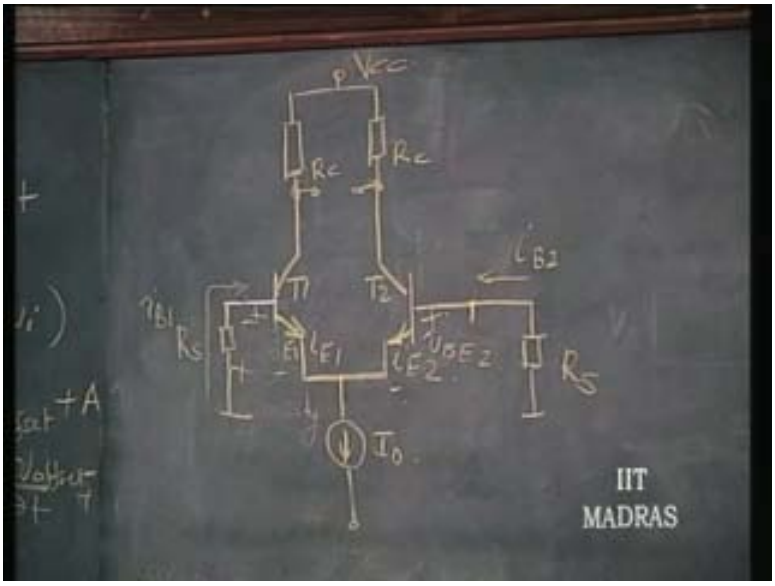

So, one way to tackle this in a very crude manner is always connect from the input to ground or virtual ground an effective DC resistance which is equal to the source resistance if it is not a feedback stage otherwise the principle is from, plus and minus both terminals to ground, you must connect equal valued DC resistances for bias current offset. These have to be done particularly for low frequency design where the drift is a major problem.

If it is a DC it is not a problem. This is going to turn itself in to a drift problem because beta is heavily dependent upon temperature. Therefore that in turn changes with temperature and that in turn causes problem for us to isolate it from the signal. Actually if it is a DC [no voice] then there is ….problem for us. You know completely about the signal. What is noise is time varying signal.

So we will stop here for today and discuss more about application oriented differential amplifiers in the next class. That is, how designs have to be slightly different when we design this differential amplifier for high frequency amplification, frequency application etc.