Analog ICs
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Lecture - 04
Differential Amplifier

In the last class, we discussed about differential amplifier as a basic building block as to how it can be thought of being evolved from the basic common emitter amplifier. And we saw that we are able to get rid of the large valued bypass capacitor which otherwise would have become necessary to bypass the DC current source and also the need for the coupling capacitor to the input by using dual supplies.

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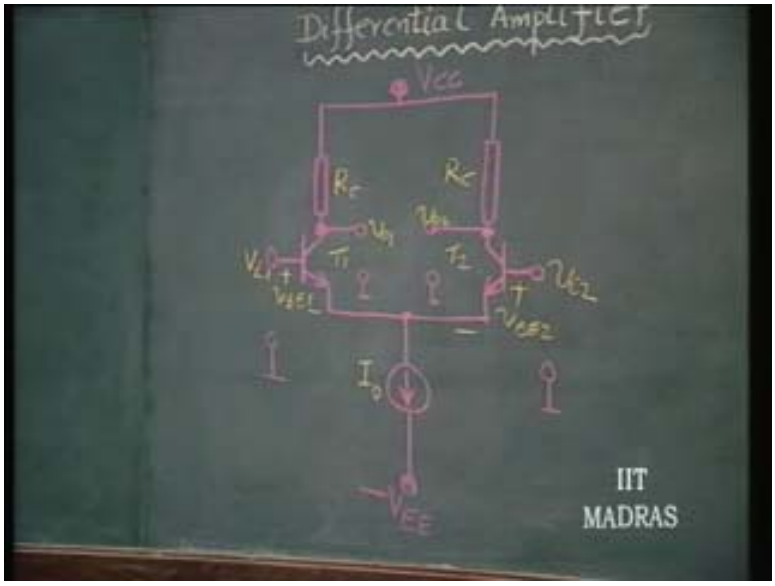

Today we will learn more about the differential amplifier as such. V_{i1} and V_{i2} are the inputs to the differential amplifier and V_{01} and V_{02} are single-ended outputs of the differential amplifier. We have seen that this input is getting distributed as V_{BE1} and V_{BE} if we name these transistors as T_1 and T_2. So, we can say that V_{i1} minus V_{i2} is the differential input V_i differential.

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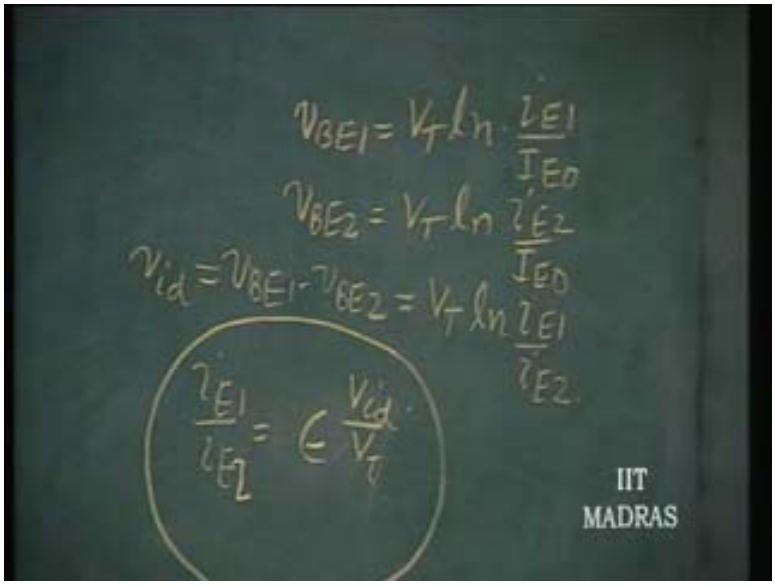

This is also equal to V_{BE1} minus V_{BE2} going through the loop. So V_{BE1} minus V_{BE2} which we have already established is nothing but V_{BE1} is equal to V_T log. Let us call this current as I_{E1} and this as I_{E2} is nothing but V_T log I_{E1} by I_{E0}, and V_{BE2} is nothing but V_T log I_{E2} by I_{E0}. So this relationship which is V_{BE1} minus V_{BE2} is nothing but V_T log I_{E2} by I_{E2}. This is nothing but Vid or this can be expressed as i_{E2} by i_{E2} current ratio is equal to one of the most important relationships in integrated circuits.

The ratio of the two currents, i_{E2} and i_{E2} is equal to V_T log that is exponential Vid by V_i. This is a very important relationship. Please remember that in any transistor configuration, if you are talking of a differential input voltage which is just the difference of the base to emitter voltages that is always equal to the ratio of the currents. They need not be connected as differential configuration. If we just take two transistors arbitrarily and take the difference of these two voltages it will be the ratio of the emitter current. This relationship is what we are going to use in obtaining the output versus the input characteristic of the differential amplifier.

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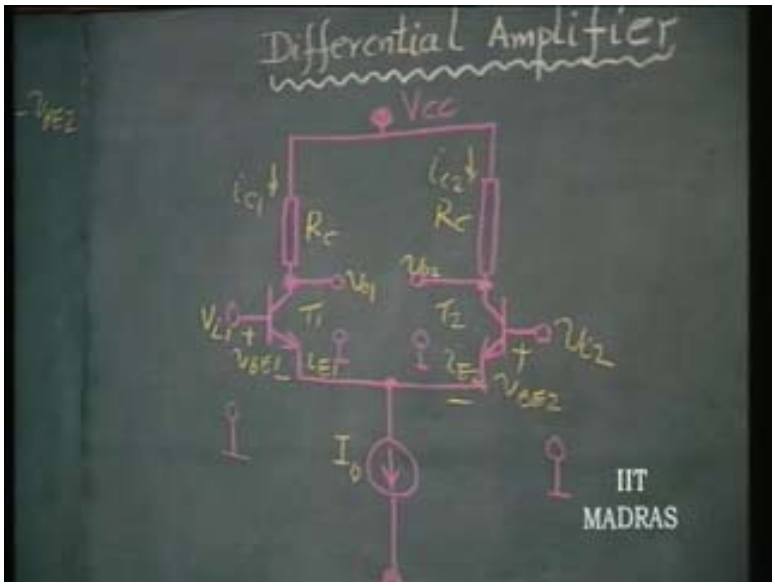

We know that the collector current here is ic_1, and the collector current here is ic_2 at any instant of time. What is it? i_{c1} by i_{C2} is equal to i_{E1} by i_{E2} because I_{c1} by i_{C2} is nothing but alpha(i_{E1}) and i_{C2} is nothing but alpha(i_{E2}).

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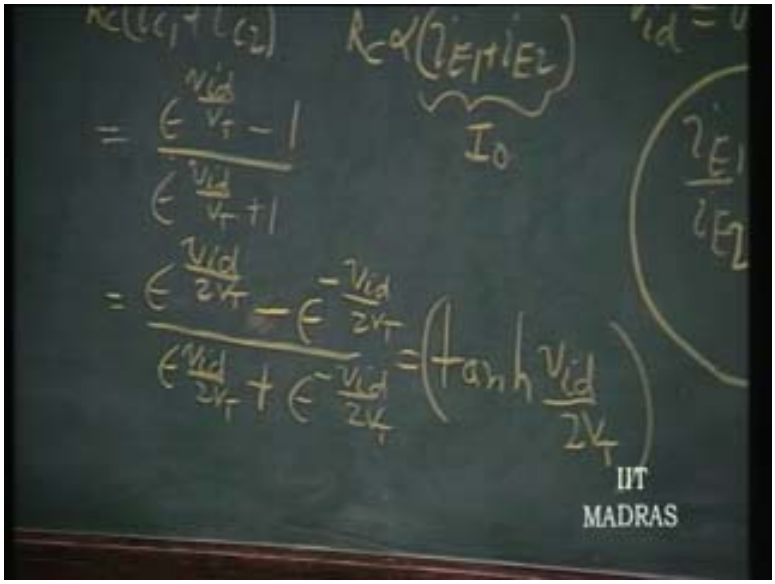

Therefore alpha gets cancelled. So this is nothing but again exponent Vid by V_T. So, from this relationship, we can get I_{c1} minus I_{c2} by I_{c1} plus I_{c2} is same as exponent Vid by V_T minus 1 by exponent Vid by V_T plus 1 from the ratio relationship.

And what is it that we get? I_{c1} minus I_{c2}. Here we can see that V_{cc} minus I_{c1} R_c is nothing but V_{01}. So V_{cc} minus Ic_1 R_c is this voltage. And this is V_{cc} minus I_{c2} R_c. Therefore, we have V_{01} minus V_{02}, which is differential output voltage being equal to V_{01} minus V_{02} is nothing but I_{c2} minus I_{c1} into R_c. So this is nothing but this you multiply by R_c, this also you can multiply by R_c so Ic_1 minus I_{c2} into R_c is nothing but V_{02} minus V_{01}. That is the differential output voltage. The differential output voltage is V_{02} minus V_{01} by R_c into I_{c1} plus Ic_2 is same as alpha times i_{E1} plus i_{E2}.

So alpha times i_{E1} plus i_{E2} is nothing but I_0 this entire thing. So what you get here, exponent x plus 1 and exponent x minus 1 is also equal to exponent Vid by $2V_T$ plus minus exponent minus Vid by $2V_T$ by exponent Vid by $2V_T$ plus exponent which is a well known tan hyperbolic Vid or we can now put down the input by output relationship as V_{02} minus V_{01} is equal to V_0 output differential which is equal to alpha R_c into I_0 multiplied by tan hyperbolic Vid by $2V_T$. This is an important output versus input characteristic of the differential amplifier in bipolar transistor.

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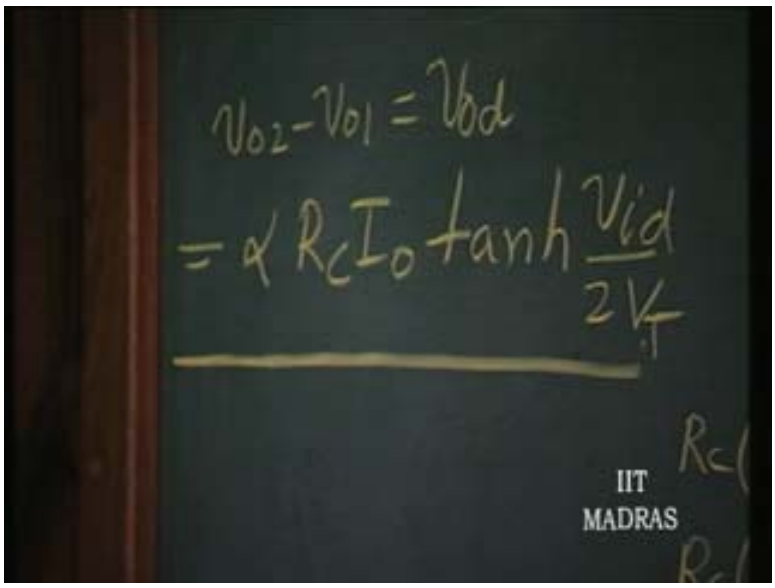

This nonlinearity is quite useful. This is what is called saturating nonlinearity. The differential amplifier has two limits within which this output can swing, and the upper two limits are primarily going to be governed by the transistor amplifier going to saturation. The transistors need not go to saturation. Now we have to see how this happens. What is it that happens where the limiting nonlinearity is due to saturation, the output gets saturated. This is an important criterion which we have to see. So let us depict this pictorially; this relationship V_{0d} versus Vid I would like to plot, how it will look like.

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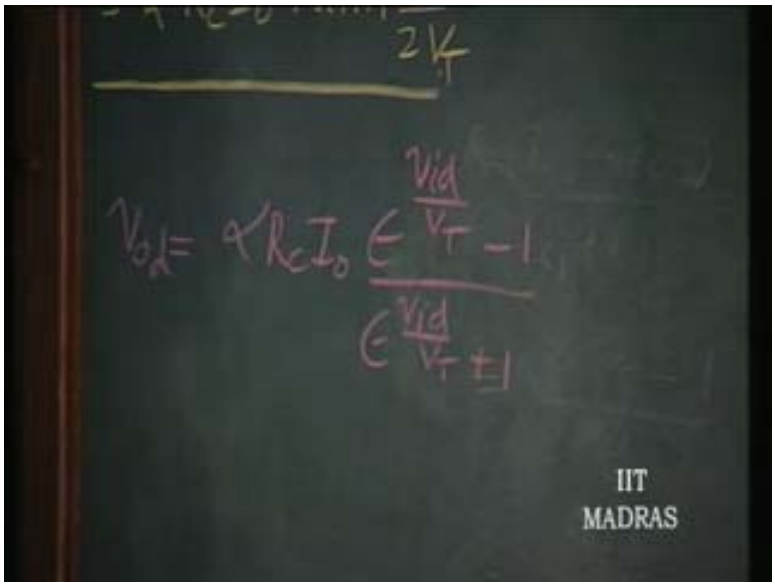

Let me write it again; exponent Vid by V_T minus 1 exponent Vid by V_T plus 1. So when Vid is negative this quantity is going to go towards 0 and this also is going towards 0. That means this whole thing is minus 1. So this factor is minus 1. That means output voltage is going to be minus alpha $R_c I_0$. When Vid is negative, now v_0d has been put as v_{02} minus v_{01} so that means we are putting this as positive and this as negative. So it is starting with this minus alpha $R_c I_0$. It is starting with that and then will go on becoming linear, as Vid becomes very large this quantity is huge compared to 1, this also is huge compared to 1 so this quantity goes towards 1 that means V_0d goes towards alpha $R_c I_0$. This is something that changes the value of the transfer function basically from plus to minus, plus 1 to minus 1. This is the saturating nonlinearity that is nothing but the tan hyperbolic curve.

And as you see, it is linear around Vid is equal to 0. So once again, what is this expansion in terms of Vid by $2V_T$ tan hyperbolic expansion? Tan x tan hyperbolic x. This expression alpha Rc I_0 tan hyperbolic Vid by $2V_T$ can be shown to be equal to expanding tan x as x minus x power 3 by 3. That is, alpha Rc I_0 into x is Vid by $2V_T$ minus x power 3 which is (Vid by $2V_T$) to the power 3 by 3. The other higher-order terms power 5 etc I ignore so the next higher order term is the cubic.

Indicating clearly that if I have Vid as Vp sine omega t for example, a sine wave input, there will be only third harmonic or all harmonics existing in this. That is easy to grasp because this particular nonlinearity is hyperbolic tan whereas in a common emitter amplifier it is simply exponential and therefore it will have x power 2 by 2 factorial x3 by 3 factorial and so on. So the second harmonic, third harmonic all these factors also come into picture. As far as this structure is

concerned inherently it is having less distortion than the common emitter amplifier.

In place of common emitter amplifier therefore we must necessarily use a differential amplifier if it is the IC. There is no need to therefore ever use common emitter amplifier as an amplifier at all in any of the designs. Therefore this particular output alpha R_c I_0 into Vid by $2V_T$ is the basic wanted amplified output wherein this factor can be easily identified as alpha R_c I_0 by $2V_T$ is nothing but gm into R_c. So alpha I_0 by $2V_T$ is the gm of the differential amplifier and that into R_c is already known to be the small signal gain of the amplifier.

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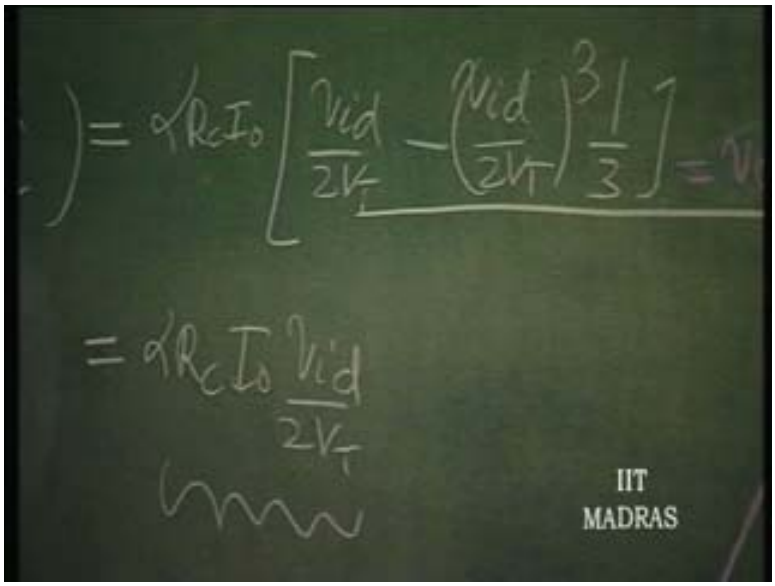

So this is gm into R_c into Vid minus alpha R_cI_0 divided by, now, 8 into 3 is equal to 24 V_T power 3 Vid to the power 3. This is going to contribute to third harmonic distortion.

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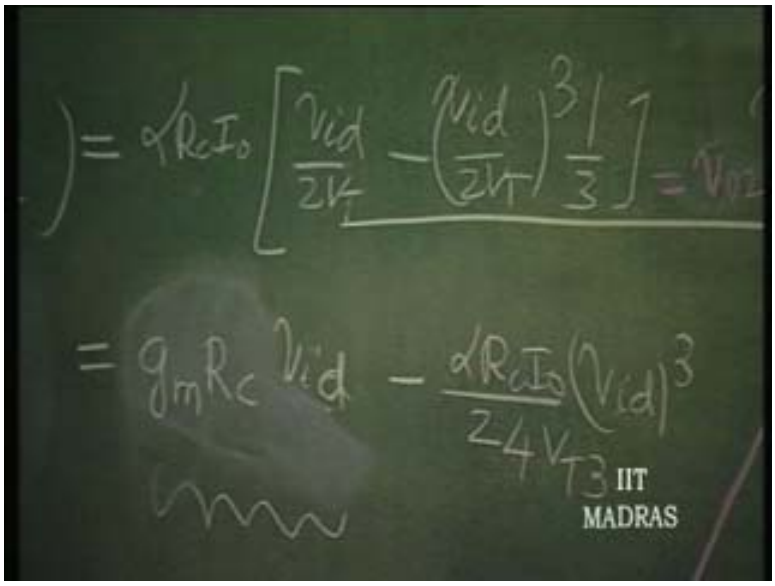

Therefore, if Vid is equal to Vp sine omega t we would like to know how much percentage distortion occurs in this. That can be easily evaluated by this, gm into R_c is the gain of the amplifier for the low-valued signal and this into Vp sine omega t is the output due to fundamental and that alpha I_0R_c by $2V_T$ again, this is again gm into R_c, so we will take that gm into Rc, alpha R_cI_0 by $2V_T$ has been taken so we have $12V_T$ square and this is Vp cube sine cube omega t which is nothing but 3 sine omega t minus sine 3 omega t4 by $4V_T$ into Vp cube.

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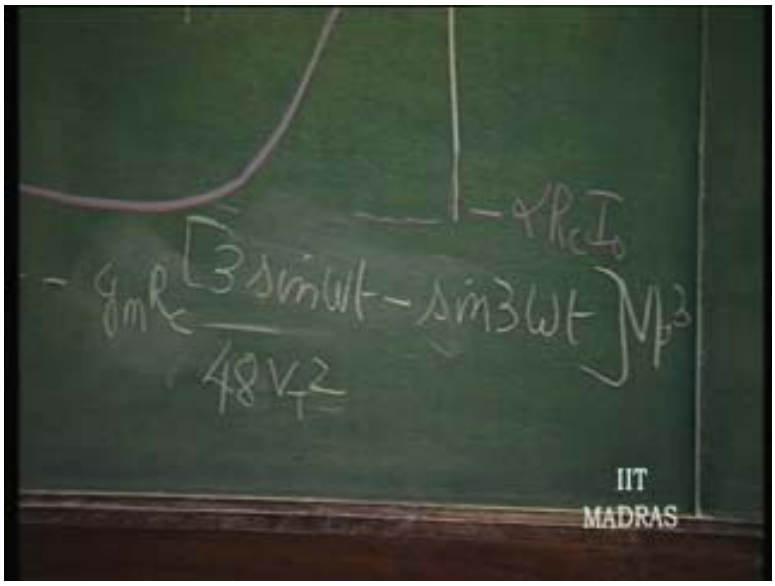

So we can see here that as far as the third harmonic is concerned it is multiplied by the same gain gm into R_c, as that of the fundamental. Apart from that there is a factor here which is coming.

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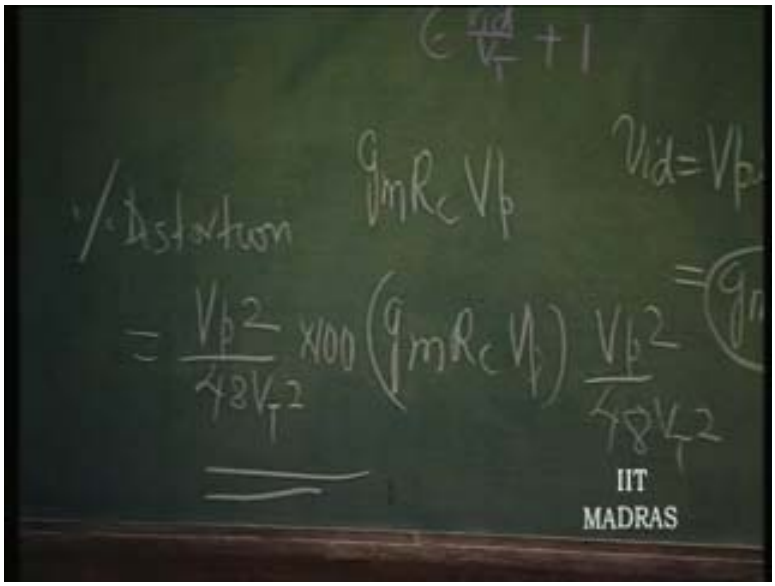

This is gm into R_c into Vp is the peak amplitude of the fundamental as against that we have the harmonic gm into R_c into Vp into Vp square by $48V_T$ square as the additional factor coming into this picture. So, if I specify now that the distortion of this signal should be restricted to 1% then you can take this as the ratio of the third harmonic to fundamental. So percentage distortion is going to be ratio of this divided by this, which means Vp square by 48, V_T square into 100.

So if I say that this should be restricted to 1% then you can find out what the value of Vp should be in terms of V_T.

You will definitely know that this distortion you may need to restrict to the specific value of 1%. The signal that you get as Vp is going to you much higher than the corresponding amount of signal for the same amount of distortion in common emitter amplifier because of the fact that, in the common emitter amplifier it is exponential nonlinearity that comes into picture. When the signal is 0 the currents will be equally divided, I_0 by 2 and I_0 by 2 so I_0 by 2 is the operating current, and therefore, this differential amplifier has the same small signal gain as that of the common emitter amplifier.

Now, what is this saturation that are curves?
The current initially is, when these two are connected together to ground the input voltage is 0 and the currents will be I_0 by 2 and I_0 by 2 that is the cohescent state where the output voltage here will be V_{cc} minus I_0 by 2 into R_c and V_{cc} minus I_0 by 2 into R_c so the differential output voltage is 0, therefore for the input 0 output is 0. Now, when the signal here increases in relation to that the current here is going to increase because we know i_{E1} by i_{E2} is nothing but exponent Vid by V_T.

So, when Vid increases the current here increases and the current here will decrease because i_{E1} plus i_{E2} is a constant I_0. So ultimately the current in this will become totally equal to I_0 and this will be 0 at which point of time it has reached one limit of saturation. What is it? The output voltage here is going to be V_{cc} minus I_0R_c and here it will be V_{cc} and therefore it has reached V_{cc} minus V_{cc} minus I_0R_c that is I_0R_c. That is what we are seeing there.

On the other hand, when this voltage increases and this voltage decreases exponent Vid by V_T goes towards 0, or the ratio of this current to this current increases enormously i_{E2} becomes larger than i_{E1} and ultimately, i_{E2} is equal to I_0, and this becomes equal to this. This is an important method of switching called current switching or this is called current mode logic or it is also called emitter coupled logic.

So the same building block is also generating a family of logic circuits which are called emitter coupled logic which are the fastest logic families known. Why is it fastest? It is because none of the transistors themselves go to saturation state. So the switching occurs merely by the current getting switched by the voltage from one transistor to the other. So, this way we are preventing the transistor from going deep into saturation and therefore this is a current mode logic which is the constant.

So we can see that as far as the logic level swing is concerned it is also governed totally by I_0 and R_c. As long as the transistors do not go to saturation as per the requirement the swing is independent of the supply voltage etc and it is equal to I_0 into R_c on either side of the operating point; plus I_0R_c and minus I_0R_c. So if you

say I would like to design in a differential amplifier working on a load of one kilo ohm operating at a I_0 of 1 mA and straight away I know what the voltage swing is, 1 kilo ohm and 1 mA 1V peak to peak is the possible swing of the differential amplifier as long as the transistor do not go to saturation which is still the requirement. Based on this you can design a differential amplifier for the required swing, output swing.

This differential amplifier is basically used as an emitter coupled logic in logic families or also in analog circuits it is used as an input stage and it has major responsibilities as an input stage. You should have high input impedance, if it is a voltage controlled device it should have high input impedance and another important factor is high common mode rejection ratio.

What is common mode operation?
We are now discussing about the common mode operation where suppose v_{i1} is equal to v_{i2} is equal to v_i common mode that means there is no differential signal. The differential signal is nothing but v_{i1} minus v_{i2}, v_{i1} is equal to v_{i2} and it is a common voltage vic. So this is connected to the same voltage as this, then what happens, as far as this circuit is concerned this particular voltage will follow this in this manner and this vic and v gamma will appear here, this is a current source and it will not have a current change. That means there is no increase in current of these two stages. That means output will remain at V_{cc} minus I_0 by $2R_c$ and this also is going to remain at V_{cc} minus I_0 by 2. This is an important factor that you should note.

When these two voltages are maintaining the same nothing should happen in the ideal differential amplifier. It is ideal because we are putting an ideal current source. The voltage here follows this in the following manner that it will be vic minus v gamma here and therefore this is seeing an ideal current source so there is no change in current occurs obviously and therefore there is no change in voltage here and this remains constant at V_{cc} minus I_0 by 2.

But then this voltage can vary, it may be a signal which has the common mode voltage component. So this can increase or decrease but nothing happens to this, this remains constant at a dc value of V_{cc} minus…. So what happens is when this voltage keeps on increasing the reverse bias voltage of this will keep on decreasing. A point will reach when collector potential becomes same as base potential. There after if you increase this the transistor will go to saturation. That means the common mode voltage has this effect on the differential amplifier.

It can drive the transistors unnecessarily to saturation. When the common mode voltage increases this way this transistor may be driven to saturation. If it is driven to saturation what happens is the output is going to be linked to the input. That means the phase difference that existed earlier between the output and the input is lost. The output will follow the input. If that happens and if this is an input stage of an operational amplifier and something like that then if one phase

difference is lost then if that op-amp is connected in a negative feedback mode now when the phase difference is lost it is going to be connected in positive feedback mode. This is what is called latch up.

This problem is called latching up because just nothing has been done but only the signal has increased at a particular signal level and suddenly the op-amp turns itself into positive feedback mode and once it turns itself into positive feedback mode the output will be going to the highest value and thereafter it is not able to come down even if the input is decreased so it just gets caught. It remains there until you again switch off the whole thing, bring it back to the original side and then increase input signal. So this kind of latch up problem is a very serious problem in op-amp design in the first few generations of op-amp design.

What happens actually is, this effective polarity difference is due to a single stage amplifier. So this we are connecting it to another stage which will also have a phase difference and the ultimate output is going to be a single ended output. So, from that output to the input if you have some kind of feedback now that negative feedback is going to turn itself into positive feedback. So when you give negative feedback you might connect the output through some resistor to this input so this also has gone to saturation. That means this phase shift is also responsible for converting it into positive feedback.

It is the overall feedback which turns itself into positive feedback and therefore this latch up problem has to be avoided in this as far as possible. What is it due to?
It is simply because the transistors are going to saturation. What is it?
It is primarily due to, I have to have an R_c and I have to have I_0 by R_c by 2. We had earlier seen that the signal output swing depends upon I_0 into R_c. If I want large signal swing obviously I must have a considerable value of I_0R_c. Also we have seen that the gain of the amplifier is dependent upon I_0 into R_c. So if I want large gain I_0R_c is going to be huge so there is some problem now. If I want a good differential amplifier, I am now caught up with this situation that it will have poor common mode swing capability.

This is the differential configuration. Even if it is differential output the same effect is going to be there. So, if one phase shift is lost the feedback will turn itself into positive feedback due to signal amplitude. This can happen in any amplifier where the amplifier is driven to saturation, any amplifier stage where you have such a stage of amplifier where one such stage goes into saturation. This is not a necessary event happening only in a stage like this. It can happen in any amplifier.

It can happen in situations where one device is connected to another device and there is a feedback. So even there if one device goes into saturation then it becomes positive. That is why this latch up problem is also there in digital circuits and not just in analog circuits. So this latch up problem therefore has to be tackled. How do you tackle?

This whole problem is that, if you put a collector to base diode what will happen is it will be going to the border of saturation and you are not preventing it from going into the saturation, it just going into the border of saturation. Therefore you are just limiting the signal level of operation but that is nothing.

I want the signal to swing pretty high or I want the gain to be pretty high, so what should we do?
The problem here is just this. This voltage is far different from this supply voltage. Strictly the common mode voltage should be as much as the supply voltage. Can you have that?
You have to replace R_c by a dynamic resistance and not a resistance which has the same, that is dc drop will be higher when the ac drop is higher or when you want the ac drop to be higher dc drop also has to be higher. But we want a situation where the dc drop has to be very low but the ac resistance should be very large. That is nothing but a current source. So why not replace these Rcs' by means of current sources.

Therefore if you replace these Rcs' by means of current sources then we can see that the current source can have a dc drop of v gamma and still remaining current source. That means this common mode voltage can go as much as V_{cc} minus v gamma. Therefore this is the design operation in the case of third generation op-amp.

All the previous generation op-amps second and first generation op-amps used to resistive configurations like this landed themselves in serious problems of latch up. The user was not able to understand why it is misbehaving when the signal level is getting increased. This was a nuisance and therefore in order to not prevent this they put dynamic resistance here.

How do you replace this?
You replace this by means of current sources. Already, operating current is determined by this I_0 by 2, I_0 by 2 here. The current swing determines the operating current here which means this cannot be independent current sources. This should be independent upon this current. They should be just drawing the current as to whatever is coming through it. That means obviously these currents have to be made current mirrors.

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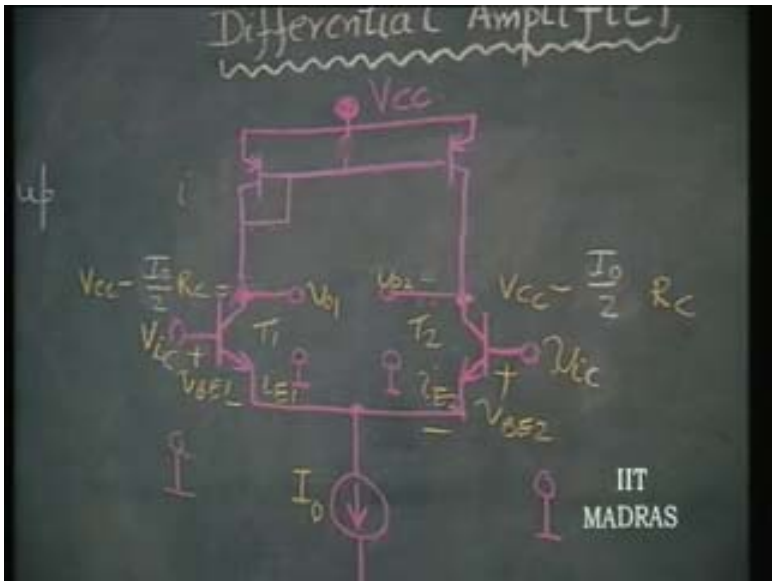

So, if this is I_0 by 2 this will be I_0 by 2. Now, when the signal is not appearing because of putting current mirror here I am making these dependent current sources. So whatever is flowing here will is also flow here. So now you can see how current mirror which was earlier used only for biasing applications becomes a very useful component to simulate a large resistance, not only that but cause is small dc drop in trying to simulate a large resistance. So what is the large resistance that is simulated? It is nothing but 1 by hoe which is resistance of the order of hundreds of kilo ohm to mega ohm.

And if you had to put such resistance and operate at 1 mA current you might have to operate with the V_{cc} of 1 mA across hundred kilo ohm, hundreds of volts whereas no such requirement here. Not only that we have the common mode voltage now, it can swing up to V_{cc} minus v gamma without any problem.

Normally output voltage cannot swing as much as V_{cc} itself and therefore there is no eventuality of any latch up problem at all because of this arrangement. This is some point which time and again people fail to understand because a given amplifier stage goes to saturation or latch up situation because of signal level. That is tackled by this. Now we have got rid of the resistance which we anyway did not want in an integrated circuit. So we have got rid of that resistance and the differential amplifier is made up of nothing but transistors.

This also is going to be a transistor current source. So you can replace this also by a transistor, and current mirror here for causing the bias and what is the I_0 value now? We have the V_{EE} minus v gamma by R, so the current source current is going to be V_{EE} minus V_{BE} by R.

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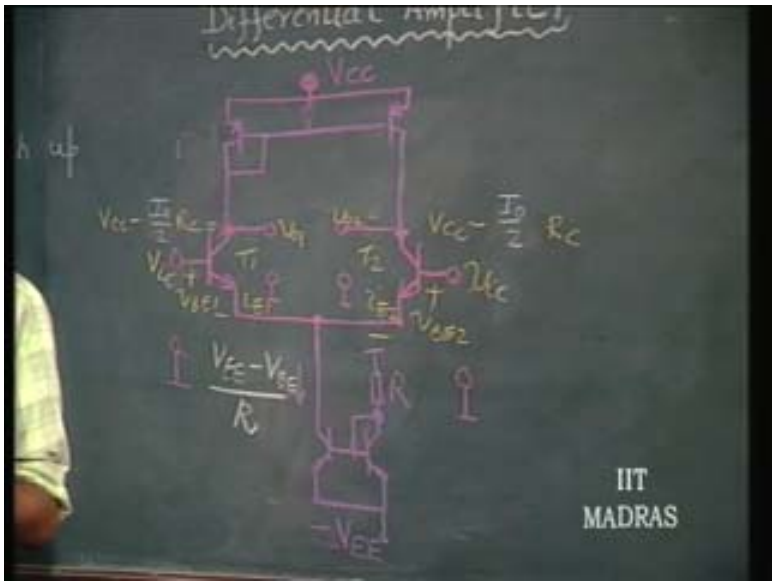

Therefore now in the entire configuration that can be very usefully used as an input stage for any device op-amp or comparator or anything has only transistors. And what is the ability of the input common mode swing here? The stage remains undisturbed even when V_{ic} goes up to V_{cc} minus v gamma on this side and up to what value on the other side?

It can keep on going down no problem, this will be following this as V_{ic} minus Vgamma and this will be going on decreasing and when this potential becomes equal to minus V_{EE} plus v gamma this transistor will go to saturation. That means it can go as much as minus V_{EE} down, no problem. That means common mode swing can happily go from one supply voltage up to the other supply voltage without disturbing the input circuit. This is an important achievement in the later generation op-amp designs that is to make the input stage handle high common mode swing as much as the supply.

We have now seen how this input stage of an op-amp gets developed, how the load resistance gets replaced by means of a current mirror, how the biasing is also done by current mirror. In the next class we will discuss about what are the non idealities, how the common mode voltage also is going to disturb the output because of the non ideal current sources that we are using and how common mode rejection ratio is not the ideal value of infinity but something finite but that can we made very high etc.

As far the differential signal is concerned the gain is gm into R_c same as the common emitter amplifier but the input impedance is now $2R_E$ into hfe plus 1 because you have two RE resistance coming here and you are looking at the base so hfe plus 1 or beta plus 1 is the input impedance of this stage. So the input impedance differential mode is $2R_E$ into beta plus 1. Once again you can see what is re two times, RE is equal to V_T by I_0 by 2 (beta plus 1) or this is equal to $4V_T$ by I_0 (beta plus 1).

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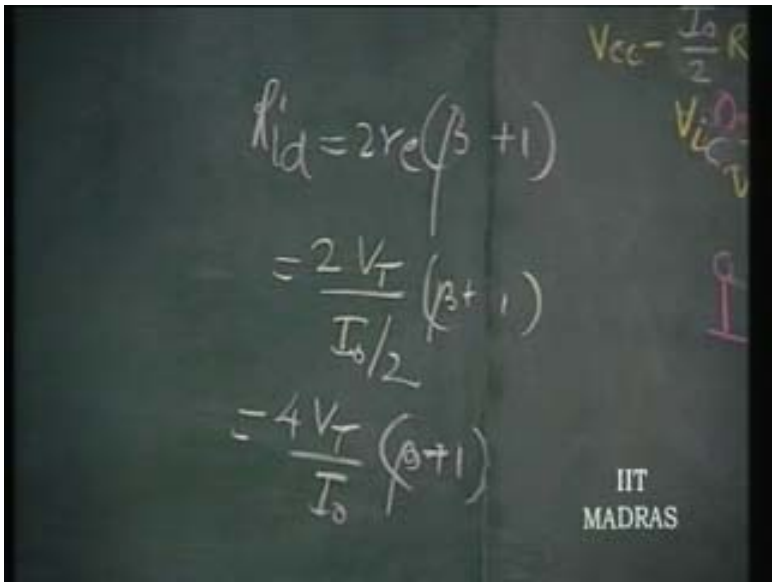

That means another design parameter for the input stage I_0 fixes up the gain, higher the I_0 higher is the gain. But lower the I_0 higher is the input impedance is a problem. That is, if you want the input impedance to be high you have to lower the I_0. So you cannot have the responsibility of both input impedance and gain given to the input stage. It is like the watchman.

Watchman is a gate keeper who is facing the outside world so lots of people are coming, we do not know what kind of people are coming and trying to get into the house. So the major responsibility is there as for the watchman is concerned to identify the character and see whether they are people who can be allowed inside. Inside, the hosts are there and they are entertaining the people who come in. So once they are admitted by the watchman the entertainment is given without any partiality. So the input stage, the hosts have certain responsibility of entertaining that is the major responsibility let us see. But the input stage, the watchman should not start entertaining the guests that will be a danger. If you want the watchman also to entertain the guests then he will not discharge his original responsibility properly. That is why as for the input stage is concerned the more important thing is input impedance and common mode swing not the gain. So we will try to sacrifice gain as far as input stage is concerned. So the same stage can be designed for different requirements.

The next stage may be again a differential amplifier but when it is next stage then it does not have the responsibility of input impedance and common mode swing. At that point of time we can worry about maximizing the gain for that stage and therefore we should not load the input stage too much in terms of responsibilities. So we will continue further in the next class.