Analog ICs
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Lecture - 28
Current Mode ICs

Today we will talk about another important topic in the so called analog circuits. This is normally known to control engineers as sampled data systems. It was control engineers who brought this first into the whole electrical engineering topic itself. But later on it was exploited by people who were designing filters looking for a solution for monolithic filters, continuous time filters. And people were not happy opting digital filters in place of the usual active RC filters for monolithic applications. The continuous time filter as we discussed was one such solution which was proposed long ago. But simultaneously what was proposed as a solution to the problem of realization of effective RC filters in monolithic form was nothing but the switched capacitor filter. Therefore we will discuss switched capacitor filter as well as switched current networks.

There is some kind of similarity in the analysis and utility of the systems. Let us first consider what was wrong with our active RC filter. We already discussed about this and brought out one type of solution in terms of master slave concept which resulted in what is called continuous time filters. Now simultaneously another solution was proposed and the solution was just this, what was your problem? Given this integrator as a building block for filters we saw that integrators could be the building blocks for most of the filters, for most of the analog signal processing operation.

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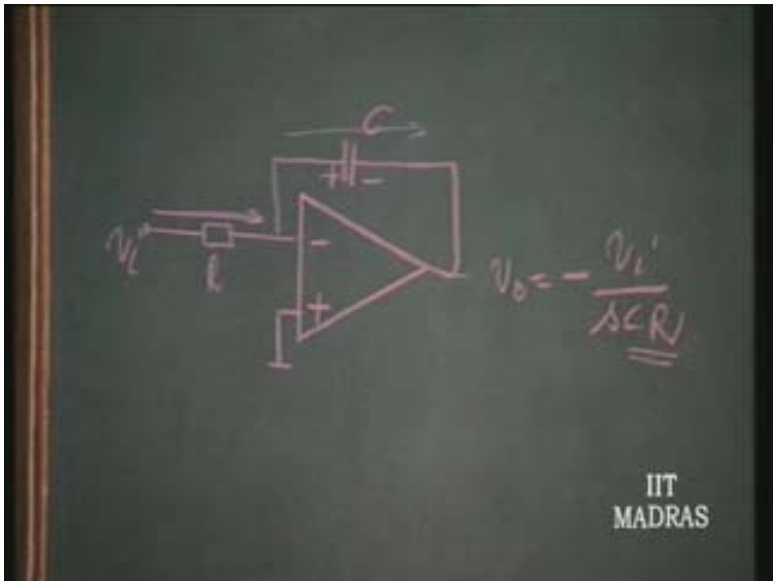

In such situations we had this problem; V_i was generating a current which was V_i/R which was getting pumped into this capacitor and this capacitor was integrating that

current so output was integral of 1/C integral of V_i/R_{dt} with the negative sign because this was charging the capacitor this way. This was essentially V_0 which is minus V_i/sCR. And in this we saw that this time constant was very crucial. The capacitors were having a tolerance of about 10 to 20% and resistance was having a tolerance of about 30 to 40% when CR was having very poor tolerance of the order of 40 to 60% which was absolutely useless for most of the precision designs. And then we came up with some solution of master slave that is one solution possible.

The other solution is this, what is it that this current is doing?
This current is charging the capacitor to a certain value. Let us do this in a very systematic manner using a carrier here in the sense (Refer Slide Time: 00:08:13) this is now going to be discussed in terms of charge transfer from one capacitor to the other. Ultimately this is going to be charged to a certain voltage. Let us assume that there is going to be a capacitor now which is going to be switched here in one space of our clock.

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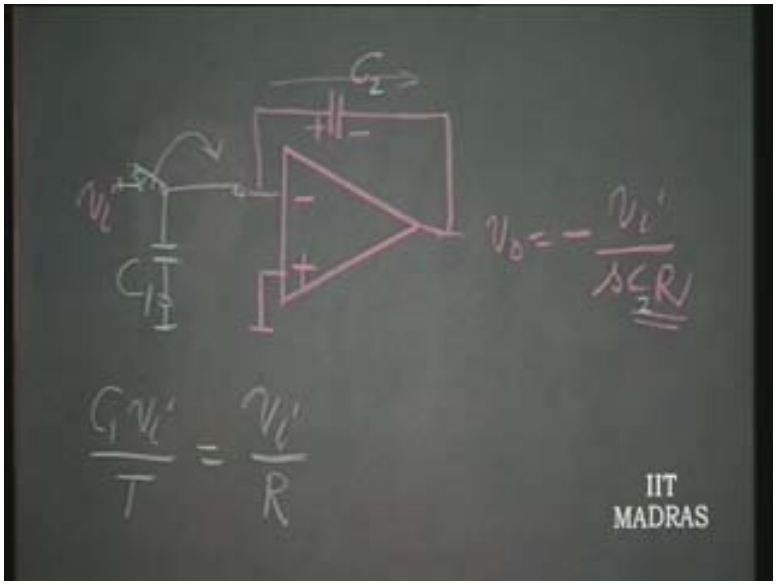

We have the clock period in which in one face of the clock this is going to connected to V_i. Let us say this is C_1 this is C_2 so one face of the clock is going to be connected here. The charge acquired by the capacitor is C_1 into V_i whatever instant you are connecting it here corresponding to that assuming that the input voltage is not going to vary much there it is held at that point so C_1 into V_i is the charge acquired by the capacitor.

This is now going to be switched over to this, so what happens?
In the other face of the clock this entire charge is going to be transferred to this capacitor by the op amp because this voltage has to be made 0. That means the next instant of the clock the entire voltage V_i which has come across C_1 has a charge C_1 into V_i which is going to be transferred to the other capacitor. Therefore the charge transferred in the whole process is C_1 into V_i and the equivalent current is charge transfer per unit time so it is the clock period T.

Charge transferred per unit time is the equivalent current which was otherwise going to be done by a resistance which is noting but V_i/R. This C_1 into V_i is the charge which has been transferred during the clock period of duration T. So the equivalent current is charge div$_i$ded by duration which is V_i/R or the simulated resistance R using a switched capacitor concept is equal to T/C_1.

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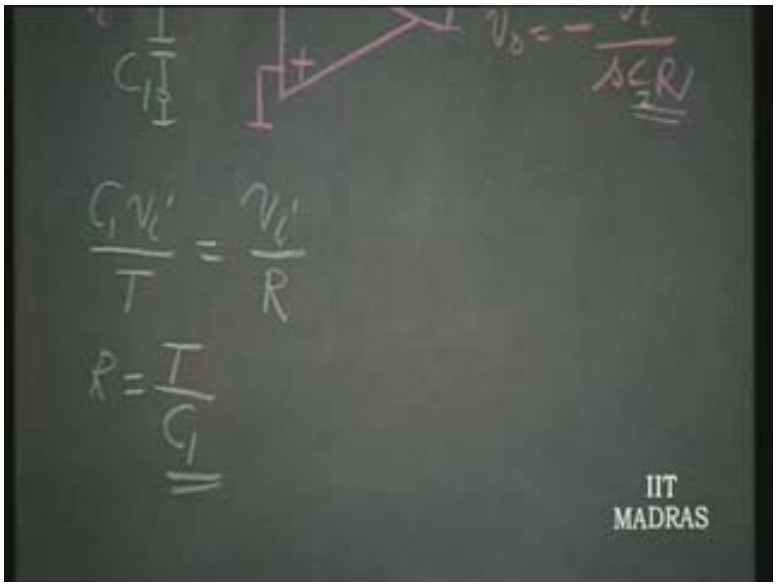

So by this act of first extracting a certain charge and transferring it the switched capacitor is behaving like an equivalent resistance R is equal to T/C, what is the assumption?
The assumption is, during this transfer V_i is remaining constant. That means the switching frequency should be very high so that I can assume that the highest frequency contained in V_i looks as though it is very constant when it is switched at this high frequency. As long as the switching frequency the clock frequency is very high compared to the highest frequency contained in V_i then this assumption is perfectly valid. Therefore if you now see the integrator the integrator time constant which was C_2 into R is now going to be replaced by T/C_1 so C_2 into R is nothing but T/C_1 which is very important. You can use any number of integrators of this type in your system for building filters or any network.

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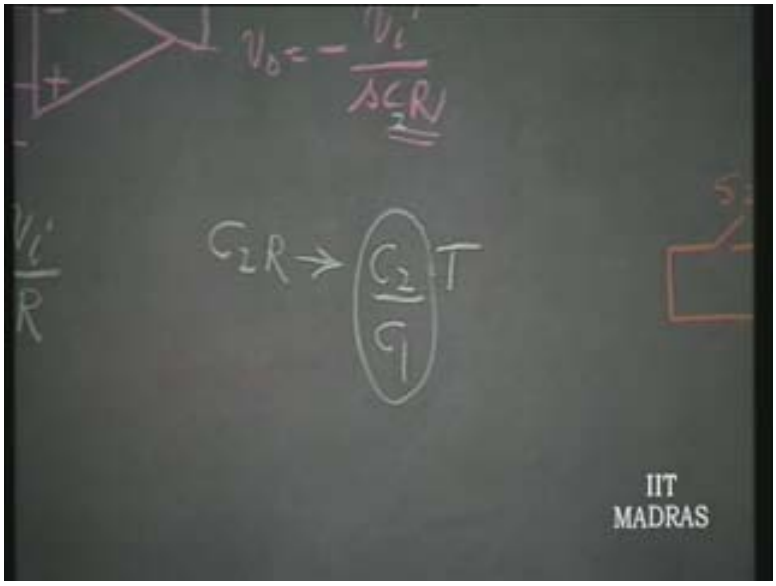

The integrator time constant is going to be a ratio of capacitors into the clock frequency. And the ratio of the capacitor has an accuracy which is one order of magnitude better than the absolute value. That means it can be kept to an accuracy of 1 to 2% and even slightly better than that and clock frequency is constant. Not only that, this can be made programmable by varying the clock frequency. So the RC time constant can be programmed by you. Therefore this exhibits exactly similar features that master slave concept exhibited.

Remember that there also we had ratio of capacitors coming into picture and the master input clock frequency or signal frequency was also coming into picture. But at the expense of switching here there is no such switching that was required in the master slave concept that is why it is called continuous time filter. Here it is called switched capacitor network or switched capacitor filter if you use such blocks in realizing the conventional filter.

For example, the KHN filter contains or the universal active filter we discussed earlier contains two such integrators. You can have two such integrators being replaced by this switched capacitor scheme and you will get a switched capacitor network which is something that can be fabricated in monolithic form with reasonable performance which is acceptable. And these switched capacitor networks are also coming into practice as VLSI circuits for doing complex filtering.

For example, higher order filtering, Chebyshev, Butterworth, elliptic filters of 12th order etc have been made in the form of VLSI circuits. The requirement will be the op amp with good frequency response and capacitors and it does not use any resistors and switches. These are the essential features of these switched capacitor network. Once you accept switching and the switches then I can perform certain gimmicks.

For example, in a KHN network you needed one integrator and the second integrator and a third inverter, to build what is called the resonator block you needed an inverter. What it means is, you can use one integrator which is inverting and another integrator which is non-inverting.

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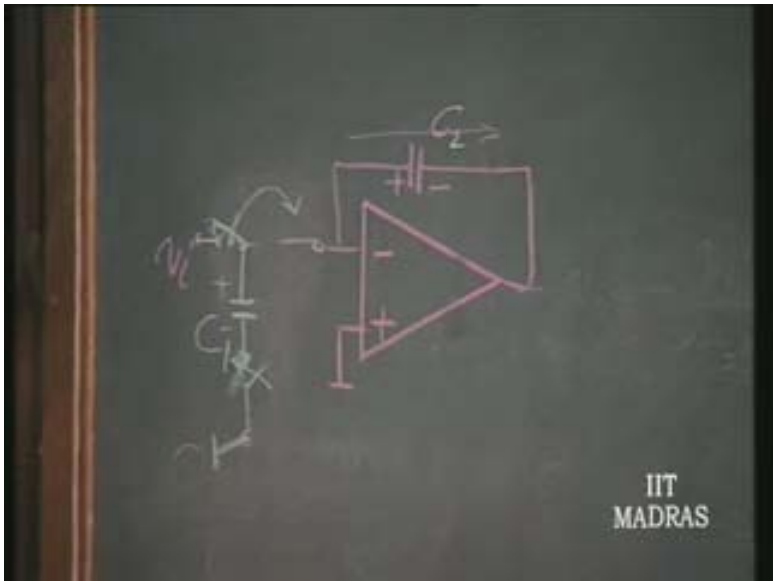

So how to make a non-inverting integrator without using another op amp which will do inversion?
That can be done if you decide to use another switch here. For example, let us say you accept the input this way and then connect the capacitor in the next phase in an inverted fashion. So, instead of constantly connecting one end of the capacitor to ground here also you will put a switch while accepting the input you will connect the input this way so V_i is taken this way. Now, while connecting it to this op amp you will just invert this that means this will be connected to this. And in the next case this will be connected to this and this will be connected to the ground.

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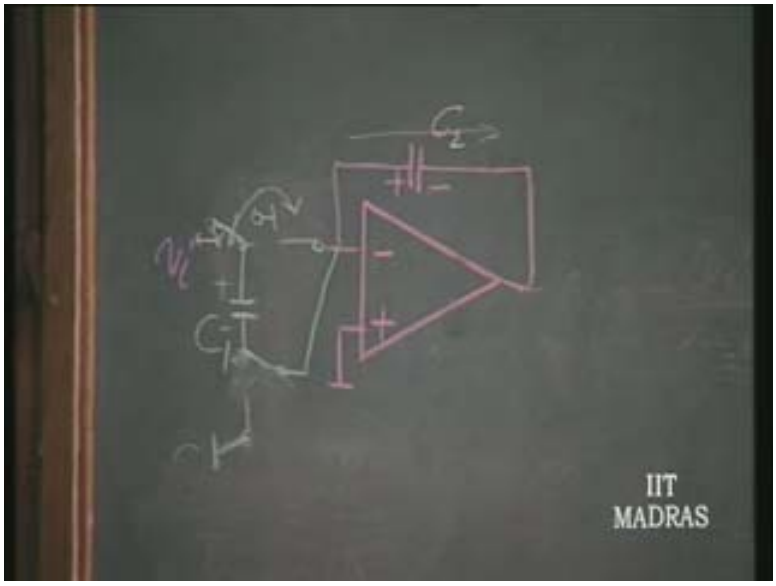

Therefore this is going to be connected to this side and that is connected to the ground in the next face of the clock. This is one face of the clock the second face and the first face would have been connected to ground and this would have been connected to V_i. That means we can get rid of the need for integrator all together that inverter so it becomes a two op amps circuit. Now, in case you have to do amplification and you do not want to use resistors, you can obtain these integrators easily by replacing one of the resistors by switched capacitor.

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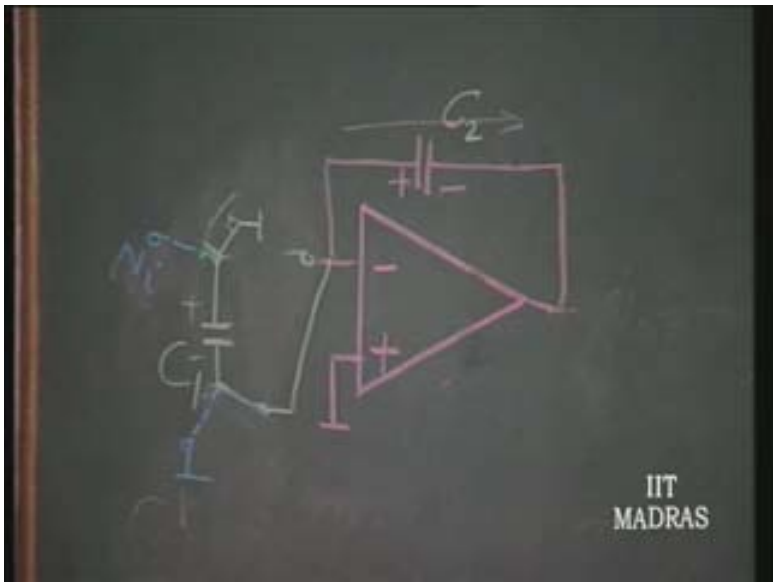

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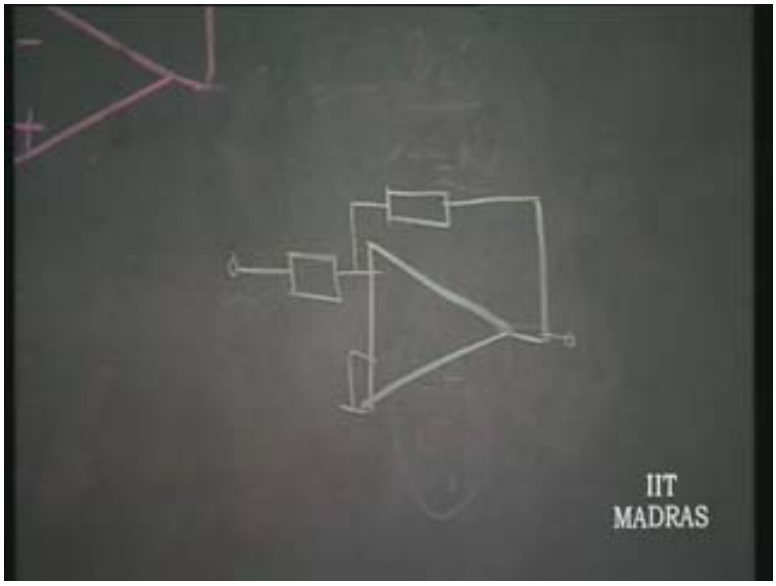

Now, if you had to do amplification here then equivalently you can replace both these resistors by switched capacitors and you can get the amplification factor as a ratio of capacitors. You need not necessarily do it in this case of a KHN network for inversion but if incase you want to independently do the process of amplification without using resistors then each of these resistors could be replaced by switched capacitors.

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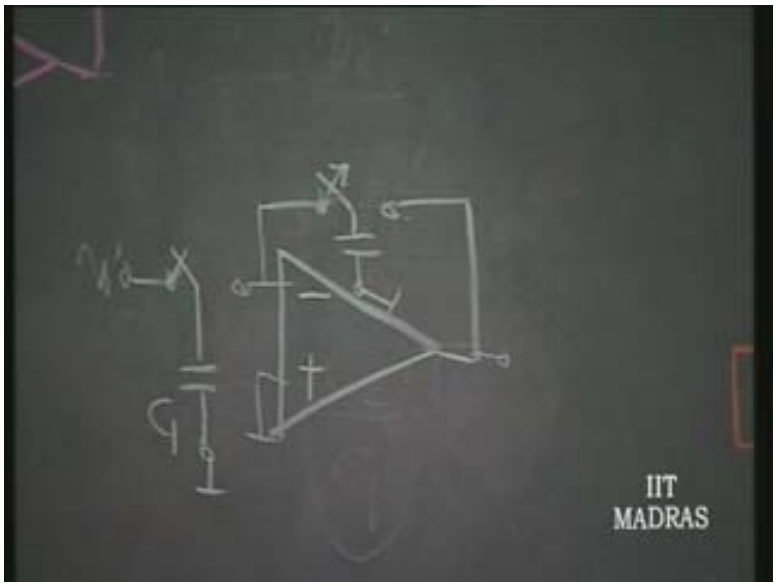

Thereby here this is receiving the charge and when this is receiv$_i$ng the charge this could be connected to the output here. And when this is delivering the charge this could be connected here and it could receive the output and then again transfer the charge. Now

this kind of scheme requires switches. And all these switches themselves will have capacitors and these capacitors will try to retain some of the charge and cause problem.

So how to resort to switching in such a manner that the capacitors of the switches themselves do not retain the charge within themselves thereby causing error in charge transfer. That kind of scheme can be developed by using more number of switches. The idea is, the charging and discharging should be taking place in such a manner that the switches invariably come across low impedance sources so that the retention of charges across these inter electrode capacitors does not take place. Let us therefore see the scheme of switching where the stray capacitor effect is minimized. You introduce switches in the following manner just for an act which can be done by using just two switches but having this disadvantage of stray capacitor effect causing an error can be got rid of by using four switches instead of two switches.

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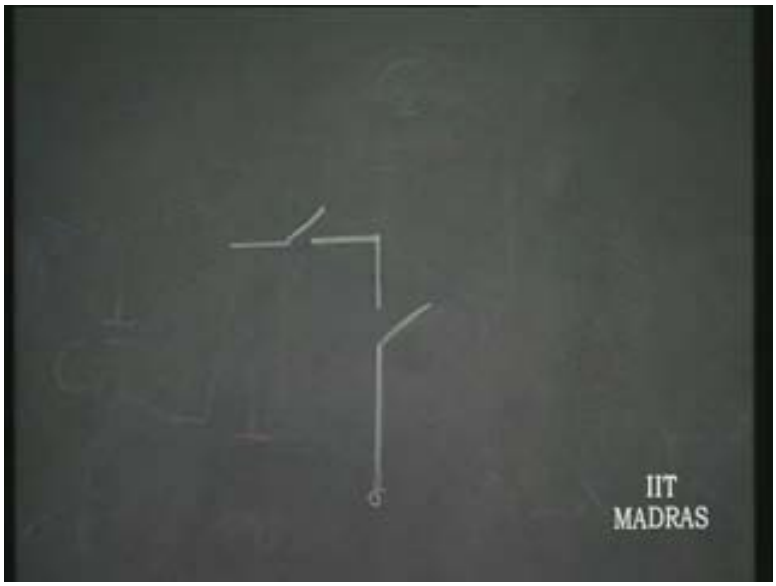

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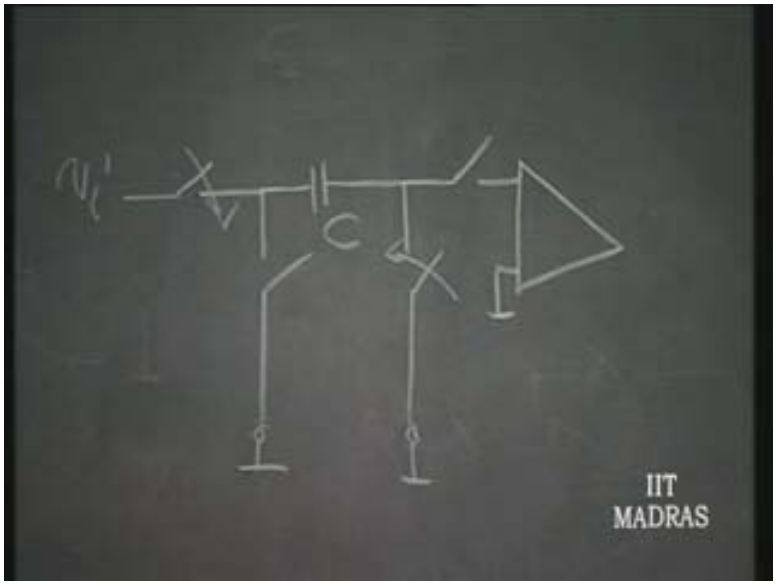

Let us say this is V_i and I want to connect this capacitor to V_i so I connect this and connect this in the first phase, these two are open, so what happens?
The capacitor is going to acquire a charge corresponding to C into V_i. In the next phase I will open these and close these.

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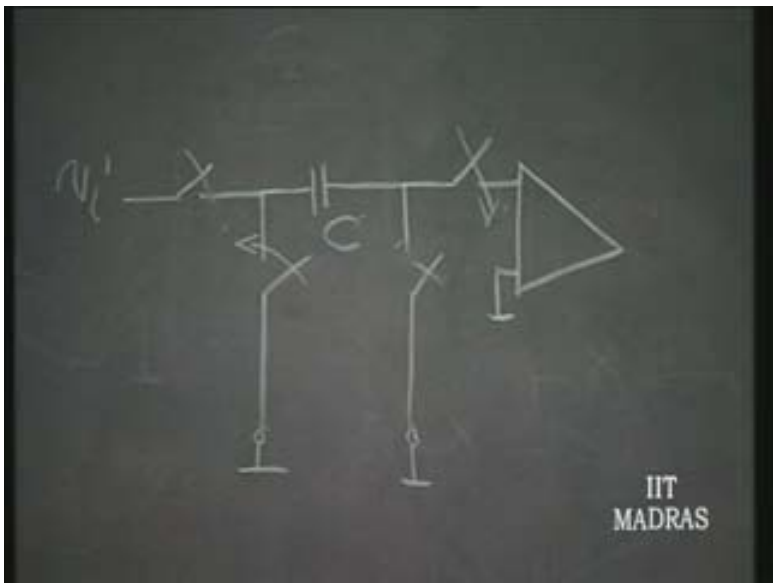

So what happens is, now inversion is also achieved simultaneously, the voltage across the capacitor originally gets charged here and gets connected in the other way in this case, so you can connect it on to the next input this way. And now if you see the capacitor is this. Whenever the stray capacitor comes into picture they come only across voltage source or

virtual ground. The arrangement is such that when the switch is open it is seeing either virtual ground potential or signal voltage which is the source. Thereby we do not have this disadvantage of stray capacitor taking away some part of the signal. And always this kind of switching is adopted in the switched capacitor network in order to get over this problem of strains. Apart from that the basic principle is very simple. All active RC filters for that matter can be converted into switched capacitor equivalent simply by replacing the resistor by the equivalent switched capacitor.

Therefore, formulating the switched capacitor network is not at all a difficult proposition. So, the disadvantage of this however is that because of switching the output is going to con comprise of simply charged packets coming at various class intervals. Therefore there will be spikes occurring in the power supply wherever the switching charge transfer is occurring there will be spikes occurring in the power supply and this gets distributed of all over. Therefore it might cause some amount of false triggering in your so called digital circuits. So you have to be very careful in isolating the power supply for this from that of the power supply of digital circuits. Otherwise there will be malfunctioning of the entire system which might comprise of these filters as well as the digital system within the same chip.

It is also necessary that if you want this finally to be shown at the output as a continuous time function obv$_i$ously you have to do some amount of post filtering because it contains large amount of harmonics. Therefore this has to be necessarily subjected to some amount of filtering. This filtering need not be very rigid in its cutoff frequency etc, it can have poor tolerance components still being used. Therefore it can be active RC filter built within the chip as a monolithic filter and in spite its poor performance it can be used for most filtering application. That means still in spite of the fact you are trying to do some amount of sophisticated filtering you need the good old active RC filter to remove the spikes etc riding over the waveform.

Filtering itself is supposed to be a smoothening effect. But in order to do filtering properly you are actually dirtying the whole waveform and also then subjecting it to further filtering. This is a major disadvantage of the scheme and that is why continuous time filters to over this in spite of the fact that lot of work has been done over the last fifteen to twenty years on switched capacitor networks. But most probably I think the ultimate solution for filtering will be only the continuous time filters and the switched capacitor network because of the fact that they need further filtering and are not likely to be used in monolithic VLSI form. They can be used for other applications. The simple system itself is sampled data system and we will see other applications of sampled data system in signal processing and realize its power. Once you can do switching you can wait and think and do whatever you want before you switch, this is a great advantage. You can make use of this advantage in designing lots of circuits.

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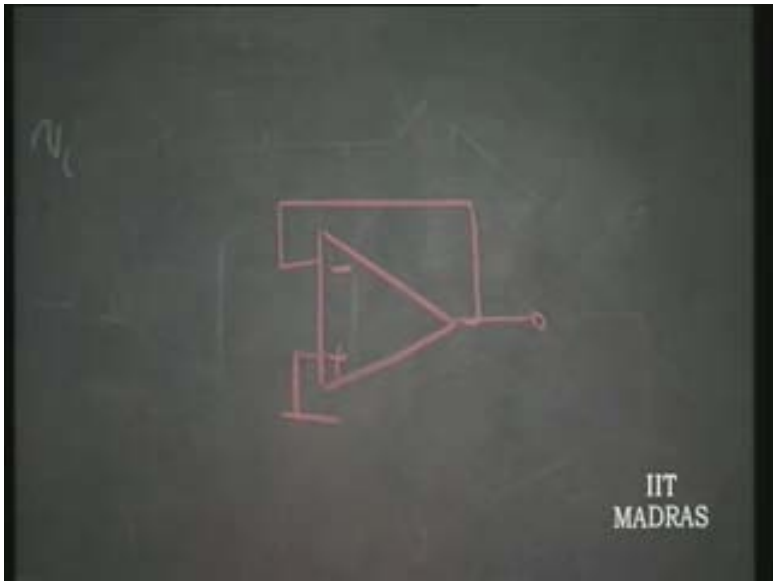

For example, you are using an op amp and you want a low offset, what will be the output voltage here now when input is 0?
It will be nothing but the offset voltage which is typically of the order of 1 to 2 millivolts for 741 like op amp and this will start drifting. Therefore for low frequency application where it is important that this drift should be minimized you would like to compensate for this offset. But we do not know how much this offset voltage is going to be at any given time or temperature so it is a tough job. Now if you say that you are going to work in a sampled data domain the job becomes very simple. What you normally do is, this is the offset voltage so you charge the capacitor using this during one face of the clock. Then thereafter you will open this and connect it to the signal and this one is going to be connected in the next case to this.

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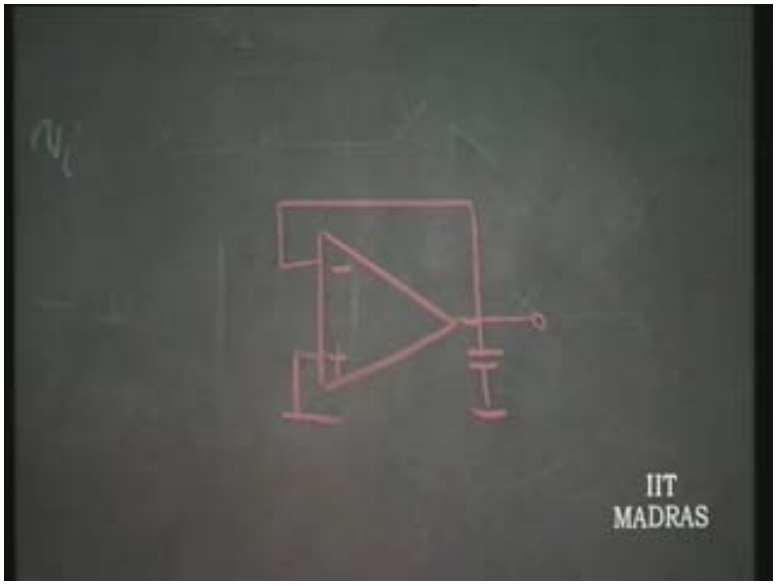

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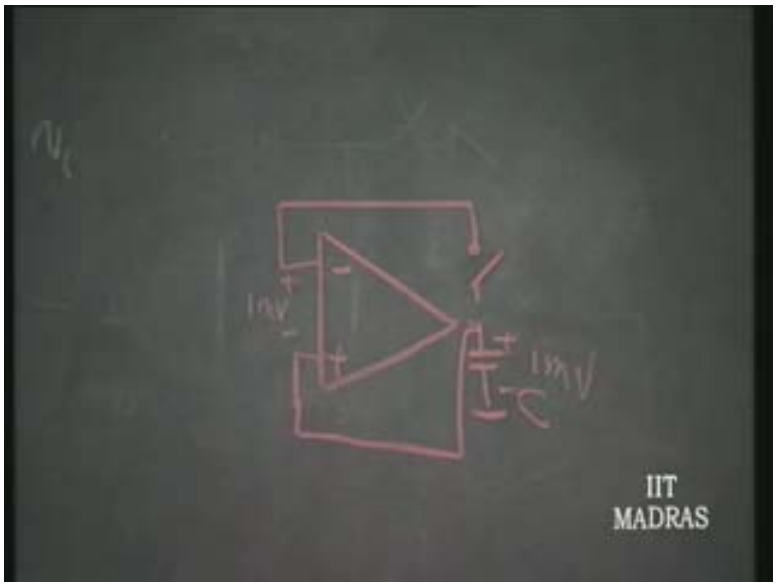

So what happens is, now this is the original offset voltage which has already been sampled here, let us say this is plus minus 1 millivolt so this has been charged to that 1 millivolt. Therefore during the phase of the clock this was connected and this feedback loop was closed. So in the next phase you have open this and this capacitor is now coming at this point here and it has already got that 1 millivolt which we have sampled and you are now connecting the output here and the input.

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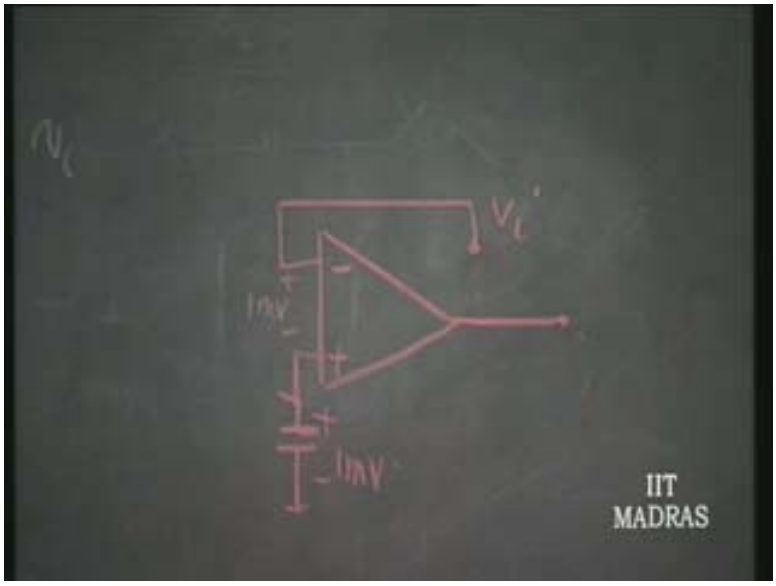

The sampled input is connected here and this can become a very good comparator. Comparator is the one which requires this offset compensation most because we would like to know when exactly 0 crossing occurs for the input voltage. If there is an offset voltage that is going to cause enormous error in detecting the 0 crossing. So you have detected the offset during one phase of the clock and applied it in series with this, and here this has to be applied in the opposite direction so that it is compensated for. Therefore by switching arrangement you can now connect the capacitor in the opposite direction so that it can be compensating for this. Now it will be a true 0 crossing detector.

Let us once again see the various operations. Initially this is closed and the capacitor is charged to the offset voltage. This is, to sense the offset voltage the feedback loop gets closed here.

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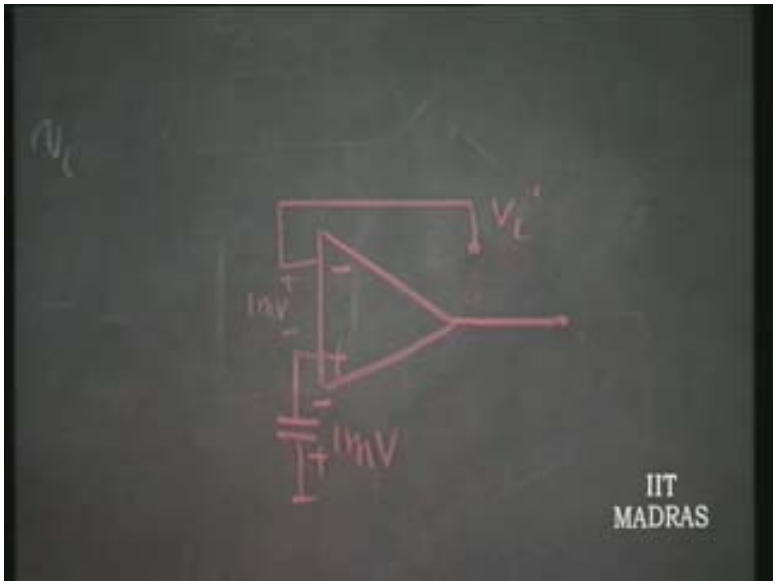

So the capacitor is charged to, if this is plus minus 1 millivolt this is going to be plus 1 millivolt. Now you will open this and open this and apply this and here also you will open this now and apply this to this. So this voltage is applied here and this is the arrangement you can have. The grounding is removed here. Originally this was closed, this was closed, this was closed and this was open. The capacitor gets charged to the offset voltage then this is open, this end gets connected here, this is closed, this is open and this is closed. Hence, the comparator is ready to receive the incoming signal at this clock phase and this you can keep on doing periodically and this is how these sample data systems can be built with facility for compensation in between. You must have heard of this self compensated amplifiers and low drift amplifiers this is the concept that is used.

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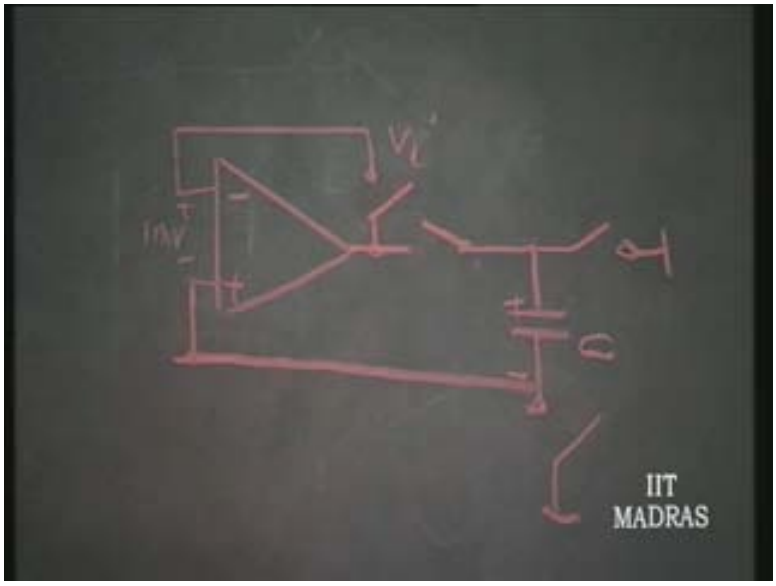

During certain time it will keep on checking its own offset in between and then compensating during the other time when it is receiving the signal. You must have heard of this chopper stabilized amplifier section. The basic principle is only this same thing because once you start chopping you can start compensating in between whenever it is not receiving the signal so you can compensate for drift.

Now we come to a similar concept where we utilize this capacitor which is there in a MOS. We have a gate in a MOS and below this we have the mass capacitor already present. If it is sufficiently large this capacitor can be used for storage. Offer information during one clock phase so why go for extra capacitors, MOS itself contains capacitor at the input. This has been exploited by a very nice principle called current copier.

What is current copier?
We know that the current mirror works under this principle. This is a current mirror, when I is the current here this I gets reflected here because this is connected with gate and drain shorted. That means this FET will adjust its bias voltage in such a manner as to make this current same as I, like the feedback system we discussed earlier. In that processes there is a capacitor here which is getting charged.

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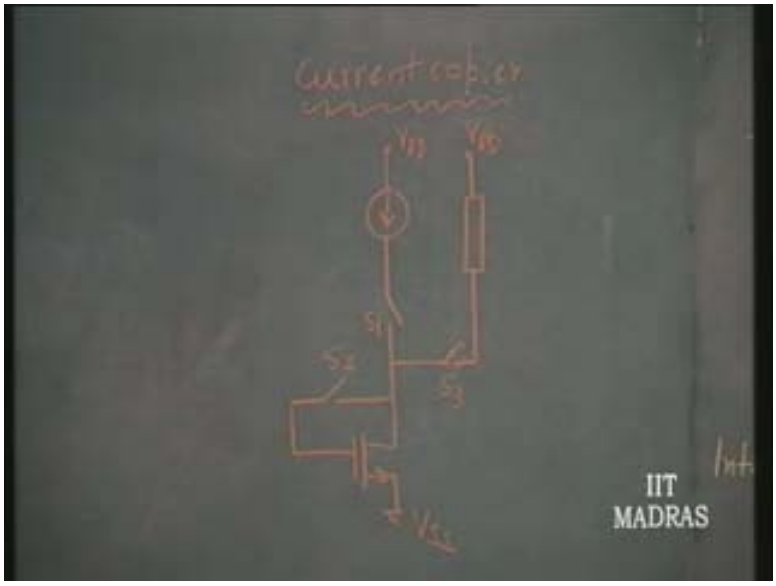

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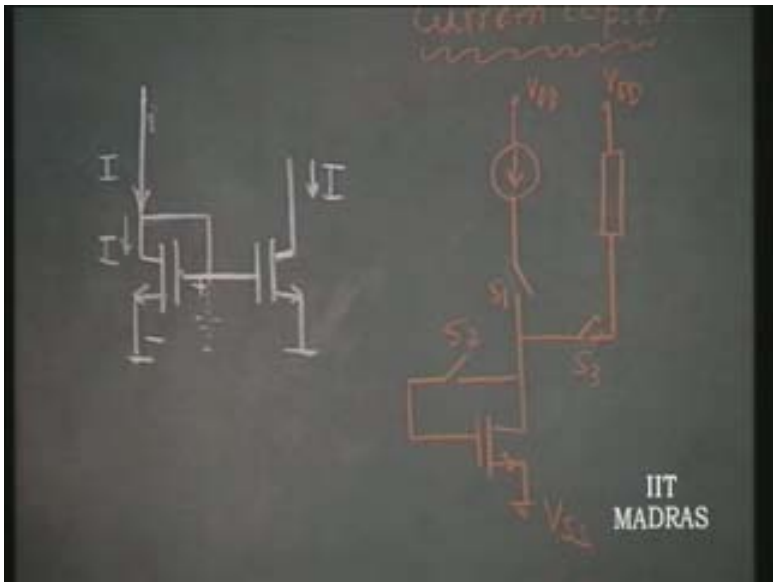

Unnecessarily why should I retain this, continuously in this mode of operation? When this itself can now retain this voltage, if I open it and thereafter make this current keep flowing. In this arrangement for the current to be reflected exactly requires that this FET should be exactly identical to this FET. We can get over this problem by using the same FET in one clock face as a feedback FET and in the other clock face as the current source. That is the basic principle of current copier which simply gets rid of this geometry dependence in current mirrors. It is independent of the geometry, independent of the tolerance of the geometry.

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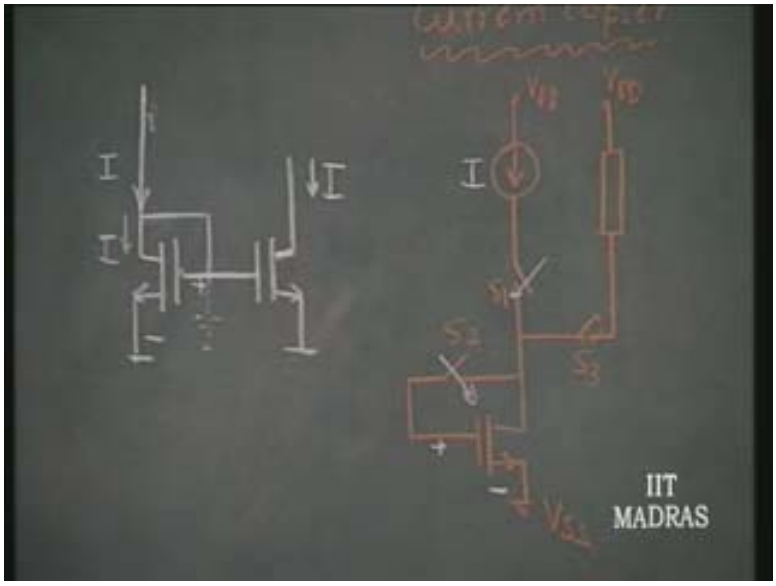

Let us see what has to be done? This is the current I, this current I is going to be pumped into this by using these switches and this switch S_1 is closed and S_2 is closed. S_1 is closed in order to pump this current into the FET connected with gate and drain shorted. That means this gate to source voltage is going to so adjust itself as to permit this current I through it. In the next phase I am going to open this S_2 and this S_1 but close this S_3. This is going to be opened, this is going to be opened but close this S_3 so what happens?
This has already been short to VGS required for sustaining this current I. So when this is open this capacitor will retain that charge and therefore this load will now have a current of I flowing through it as though it is beginning like this circuit here. Therefore current mirror action is exact.

There is some small edge, what is the edge?
Considering the fact that when this current source is connected this capacitor should be fully charged and it should not discharge any amount during this time when I am connecting it here. Once again if the clock frequency is high enough I can achieve this retention of charge. But of course if the clock frequency is too high I might not be able to charge it fully so you have to be very cautious about selecting the clock frequency suitably that this current mirror action is exact. Therefore now this can be used wherever current mirrors are used. Or for that matter this itself can be used, the load can be anything, It can be even a capacitor. If it is a capacitor you are now generating an integrator.

For example, in this face of the clock you can have I_0 flowing through this and in the same phase a signal current being pumped additionally here. And in the next phase you can have I_0 still flowing through it but open the signal current here. Now only the signal current will be pumped into the load because that much information is going to be retained here in VGS which will only pump out the signal current, I_0 is all the time there, I am now connecting a current of i into this signal. So this is going to be charged to that

voltage as to sustain a current of I_0 plus I. Here this is going to be closed at that time, this is open. At the next instant of time I will open this and close this, and what happens here is, the moment I open this, this is still carrying I_0 plus I. Therefore this signal current of I will now start flowing though the load.

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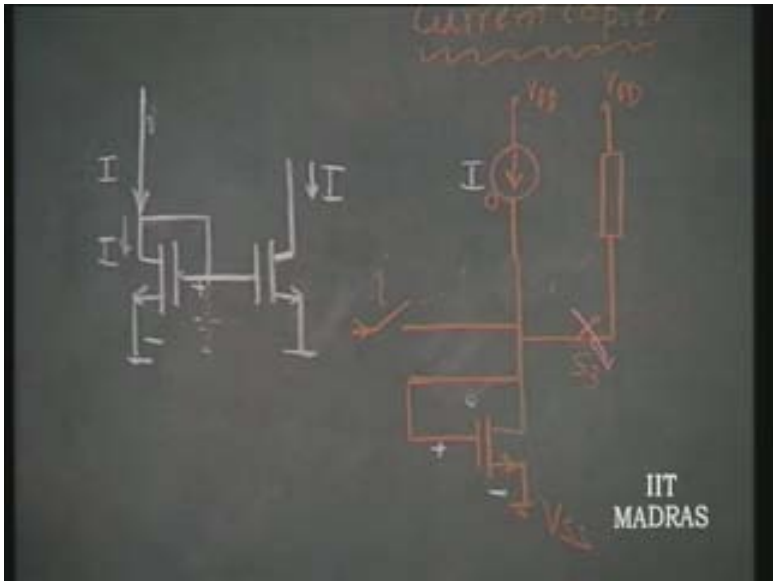

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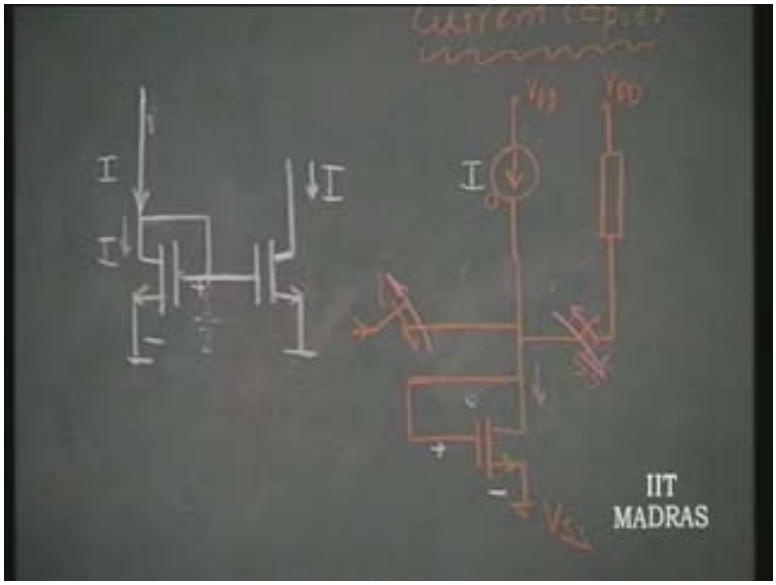

This way I can transfer only the signal current from this to this and this. If it is a capacitor for example it is now going to behave like an integrator where i is getting into the capacitor so you are charging the capacitor by means of a current so it is an integrator. Once you have an integrator you can use integrator blocks to build a filter. So this kind of

signal processing circuit can result in what is called sampled data filter or even this analog filter.

Now, coming to the final topic there are so many other application using this. It can also be used for integer multiplier that is digital to analog converter. You can copy the current many times and add the current. Depending upon your number of switches you can add the current as you do in the case of a D to A converter and for all these you use the same current to copy.

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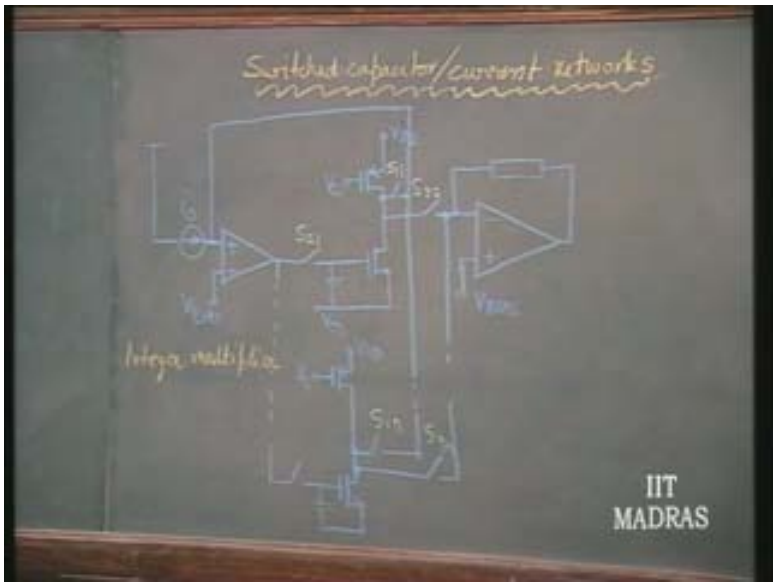

Now you can see an arrangement here. I_0 is the current you would like to copy in the entire current mirror. Let see how it is done. In the first phase this is closed and this is closed. There is a constant current i_0 flowing through this. This is nothing but a FET with a current source biasing just as we had done it there. I have actually put the current source here in terms of a FET. So you have this FET with i_0 originally flowing. Now this is closed, this is closed so this i_0, let us say this is capital I_0, this is signal i_0 so what happens is, this i_0 is going to be added to this along with this and this will be I_0 plus i_0. So, if this is closed the op amp will adjust the bias of this in such a manner that V_{GS} will get adjusted to that value that is required to sustain a current of I_0 plus i_0.

Now the same thing can be done in a sequential manner so that all these things can get the additional signal current of i_0 into that. And then depending upon the number of switches you activate as S_{32} when you close this has to be opened and this is also going to be opened and then the entire current the summation of the current is going to be pumped into the load depending upon the number of switches that are going to be closed. So, depending upon the number of switches that are likely to be closed you can multiply it by any integer. The output can therefore be determined by a multiplication of the same signal current by any integral value. This idea is almost similar to the idea you would

require for obtaining a D to A converter. So you can see that in this particular case these need not be actually having any identical geometry.

Irrespective of the geometries they will get charged to the same signal current and they can deliver the same signal current at the output irrespective of the mismatch. So this matching factor does not come into picture at all in this scheme. So this is an integer multiplier. Similar idea can be used for D to A converter or div$_i$der. Such applications are many in this field of switched current and switched capacitor network. In our resistive weighted resistor scheme you can replace each of those resistors as well as the feedback resistor by switched capacitor then it becomes switched capacitor D to A converter. Therefore this is a very powerful technique of switching. The only disadvantage is that the spikes are going to be generated in the power supply which maybe harmful to the other circuitry devices. But otherwise the flexibility and the possibility in design are many in this particular technique.