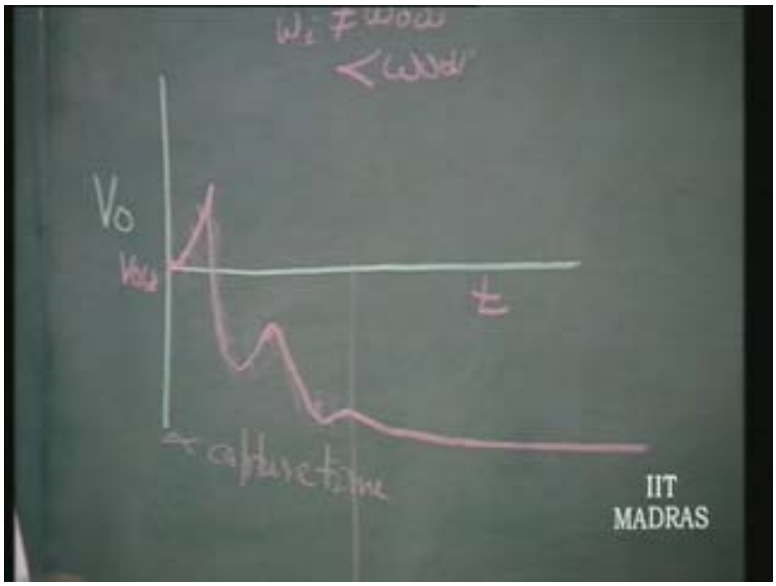
Analog ICs
Prof. K. Radhakrishna Rao
Department of Electrical Engineering
Indian Institute of Technology, Madras
Lecture - 26
Phase Locked Loop (Continued)

So now I would like to explain to you another important phenomenon in Phase Locked Loop that is the process of capture, how does the capture actually takes place. You understood this for understanding something about capture range.

(Refer Slide Time: 00:05:39)



But actually speaking how does the capture transient occur?
Again let us examine V_0 because that is one point which will tell us clearly when steady state reaches. Assuming that originally Phase Locked Loop is having $omega_i$ is equal to $omega_{0Q}$ but now suddenly $omega_i$ changes to some other value.

So what happens?
Obviously V_0 was at V_{0Q} $omega_i$ is equal to $omega_{0Q}$ and suddenly frequency changes from $omega_i$ is equal to $omega_{0Q}$ to some other value either higher or lower. If it is higher the ultimate steady state V_0 should be higher than V_{0Q} we will assume, if it is lower ultimate steady state voltage attained at V_0 should be lower than V_{0Q}. So let us say it is lower, $omega_i$ applied is less then $omega_{0Q}$. Now this is the time access let us say, ultimately the steady state value should become equal to this when $omega_i$ is different from $omega_{0Q}$ but less than $omega_{0Q}$. Then at the instant of this particular thing it was equal to $omega_{0Q}$ and let us say we have produced some kind of sine wave output because all the harmonics are going to be eliminated by the low pass filter that the fundamental component will have and at every instant of time frequency is changing. Therefore it is not a sinusoid but it is something that has narrow form here and a broaden

form here so that in effect has a time average it is producing a DC in this direction. If it is to produce a DC in the other direction it would have been narrow here and getting broaden on this side.

At every instant of time the frequency is changing. So what I am plotting here is supposed to be the filtered output but not sinusoidal. So it is becoming narrow here and broadens at this point so that on an average it is getting a DC on this direction. And in the next instant of time it will be broader than this here and this will be still broader than this and effectively it is producing a DC in this direction. It might take place within few cycles we take few hundreds of such cycles that obviously depends upon the low pass filter capacitor, the averaging capacitor. But this the kind of wave form with what lot of high frequency superimposed over it because that is not going to be totally eliminated but will be attenuated considerably.

So you will see a waveform of this type and this is called the capture time after applying the incoming frequency equal to omega_i which is less than omega_{0Q} it takes certain time for it to capture the incoming frequency that is called the capture time. This is how the output voltage will look like. This is in effect the output when you apply a step frequency in input suddenly the frequency changes and again it is brought back to omega_{0Q} and again this will come back. So you will see that this is the kind of waveform that the FM detector should give as output if it is given an FSK signal because the capture time should be made as small as possible for us to reproduce the square wave. So this is a design criterion for this.

(Refer Slide Time: 00:12:52)

So far we have discussed two of the important applications of the Phase Locked Loop, one is straight away for signal conditioning. Signal conditioning means improving the signal to noise ratio and improving the power level at which the signal gets delivered. Again signal conditioning can also be like this, not necessarily selecting the FM signal

you want and strengthening it. Also sometimes synchronization frequency is not continuously coming wherein television receiver. Horizontal and vertical synchronization pulses are sent not continuously to be reproduced at the receiving end but continuously.

So what you do?
You will have two PLLs functioning one at horizontal synchronization frequency and another at vertical synchronization impulsive frequency getting the composite video at the input so what happens is whenever you have the wanted information of horizontal frequency the output is going to correct itself to the correct DC so that output frequency is same as what is coming during those periods. And that voltage is going to be retained because it is going to be a large capacitor until the next set of information comes in.

So you can extract the synchronization frequency from the composite video using simply a Phase Locked Loop running at the corresponding free running frequency corresponding to the horizontal synchronization pulse or vertical synchronization pulse width frequency. That is also forming part of signal condition or FM detection. FM detection obviously is an FM demodulation or FSK demodulation it does not matter. FSK is nothing but frequency shift keying used for data transmission. FM is a regular what audio signal modulating a carrier. So, for both these purposes it can be very well used. Prior to this all the FM demodulators were having limited dynamic range of operation whereas this particular thing has excellent dynamic range.

Mostly in other FM detectors the FM detection is done by using tuned circuits and locating the carrier of center from the tuned frequency so that it can produce amplitude variation corresponding to the frequency variation. This property was used earlier whereas here in this case we are using a linear VCO. Therefore the dynamic range of the FM detector depends upon the dynamic range and the characteristics of the VCO. So this is an important aspect of PLL as FM detector and most of the present day FM detectors are PLL based.

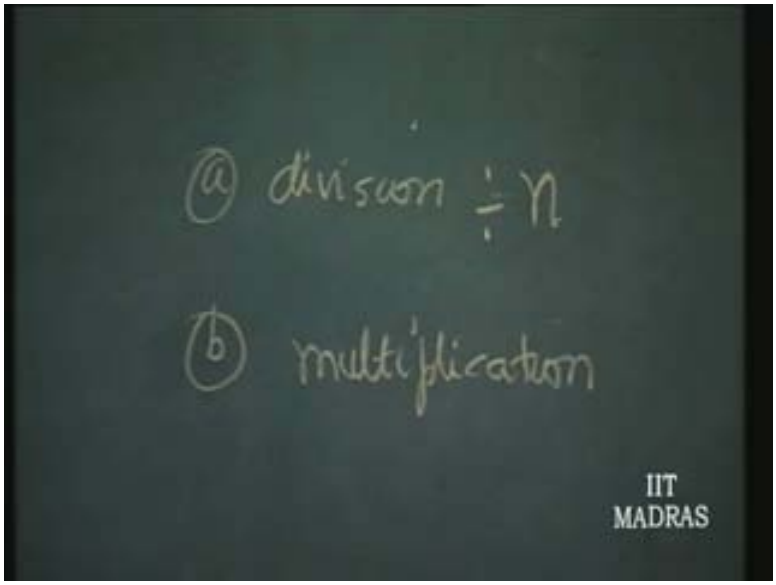
The next important application is called frequency synthesis. This is very important in communication, frequency synthesis particularly for military applications wherein they would like to keep on changing the carrier frequency in a particular sequence known to only them so that the enemy cannot detect your signal so this kind of thing is attempted. Now, if you keep on changing the carrier so often then there should be a perfectly safe way of generating the same stability carriers at the receiving end otherwise there is no use.

This frequency synthesis is an important synthesis technique adopted in communication, what does it involve?
It involves generation of any frequency output with as good as stability as the main source. The main source may come from a crystal. Crystal oscillators are the ones which are primarily used for generating stable frequency output. So, crystal oscillator is the main source to generate the reference frequency and it is so good now-a-days that this design has been so perfected that you can get excellent stability with respect to temperature etc as far as the frequency of oscillation is concerned. Almost everybody has

decided that any accuracy you want in your electronic circuit will depend on a reference and that reference shall always be if possible a frequency reference not a voltage reference, it can even be a time reference. Even a time reference can be derived from a frequency reference. Therefore most of the present day control circuitry used as reference frequency and not the olden day technique of using voltage references.

Crystal oscillator of f reference is coming. How to synthesize the output frequency of any value using a given reference is the purpose behind frequency synthesis. The problem is how to get f_0 of any value giving f reference as the input that is frequency synthesis. Now, one on or two operations needed for this straight away is, one is frequency division. This division is the simplest operation performed. Division by two for example, binary division is done by a multivibrator. So very simply you can division by a factor of two by using digital circuitry there is no problem. Therefore division by any number can be done again by using counters, any integer.

(Refer Slide Time: 00:15:26)

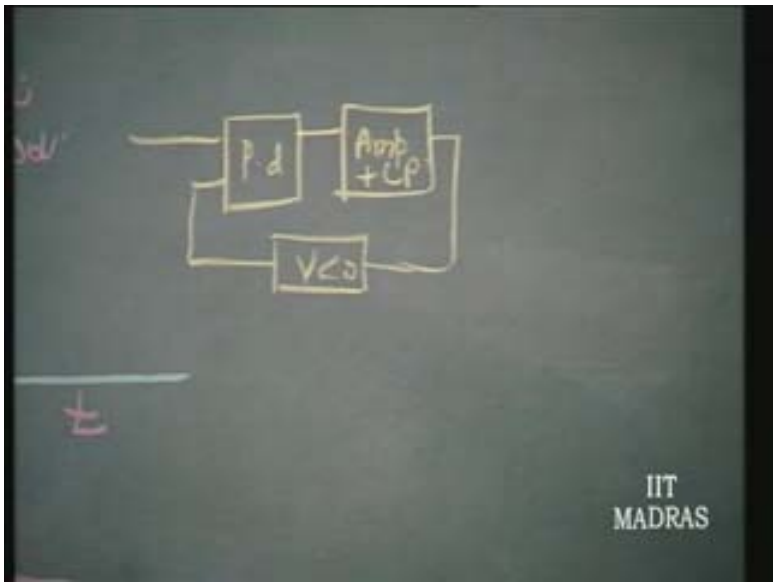


Thus, division by any number n can be done using digital circuitry. That does not solve our problem of frequency synthesis in its entirety so you also have to come up with other methods. Multiplication is pretty complex.

What is the easiest way of multiplying a frequency?
It is any non linearity. That was the age old technique. When microwave engineers were confronted with this problem of frequency synthesis used diode non linearity, diode is a non linear device. Therefore they fed this signal to the diode and output of that had lot of harmonic components and they could filter out the desired frequency component. But this is a very inefficient way of doing it because harmonics will be reducing in amplitude as you try to select higher and higher harmonic components. Therefore now multiplication had to be done in a better manner that is the purpose of the Phase Locked Loop.

A Phase Locked Loop has a phase detector which is nothing but a multiplier and amplifier plus low pass filter and this is the phase detector. Frequency synthesis can be done by what is called harmonic capture.

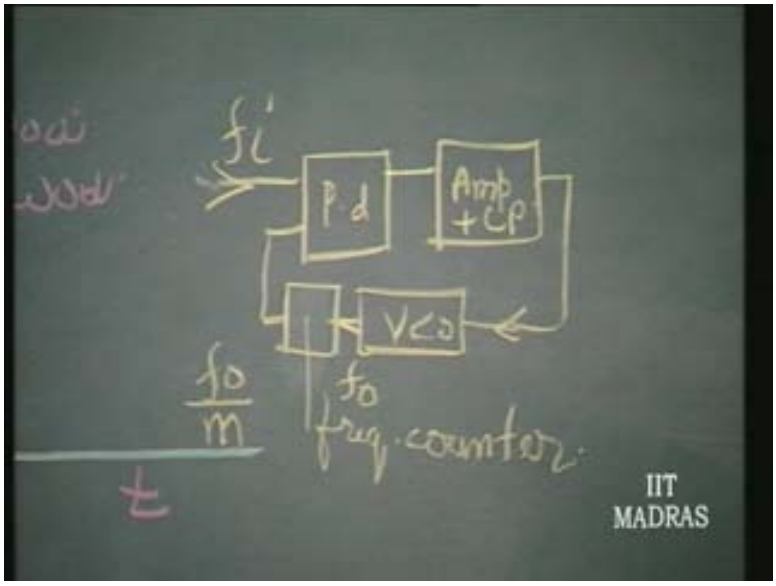
(Refer Slide Time: 00:16:52)



If this is free running at 1MHz and I feed a frequency which is very close to 1MHz then it will capture that and will keep tracking that. But if I feed at this input one third of a mega hertz here it can still capture. In the input you have one third of a mega hertz obviously there will be 1MHz as the third harmonic in it so it can get locked on to the third harmonic component of this signal. So what will be produced at this point is going to be still close to 1MHz. It need not be really one third mega hertz but it can be close to one third mega hertz so if it is close to one third mega hertz this will be close to 1MHz locked on to that. That means now you are selecting the third harmonic as the output. Therefore the multiplication factor is by a factor of 3. It can now vary around one third mega hertz and this will vary around that. This is called harmonic locking. But this is again not very efficient because the phenomenon capture depends upon the strength of the signal. The strength of the harmonic content keeps on decreasing.

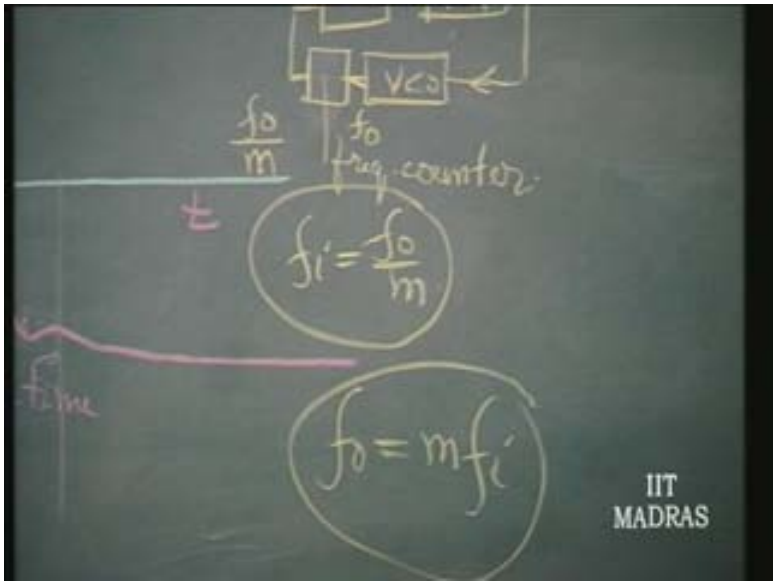
Now the same argent in the other way also is valid. This can be 1MHz but this can be one third mega hertz. That means it is called sub harmonic locking. So I can divide and multiply using this harmonic locking principle by any number. This method is possible but not in vogue, what is in vogue is this.

(Refer Slide Time: 00:19:58)

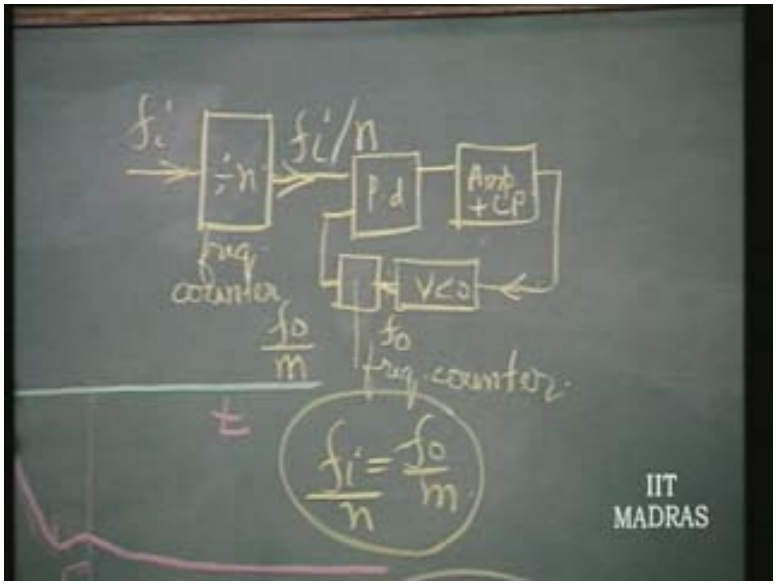


We will design a VCO with a frequency counter, you put a programmable counter. That means this VCO frequency is f_0 and this will be f_0 by n or we will call it m. So this incoming frequency is still f_i. Therefore as far as the Phase Locked Loop is concerned it does not know what you are doing. It thinks that this whole thing is the VCO. It still thinks that this whole thing is the VCO. So it will say f_i is equal to f_0 by m or f_0 is equal to mfi. So you take the output here and you will get frequency multiplication. This is one of the important applications of a Phase Locked Loop multiplying the frequency by any entity. So you said you are going to multiply by any number then let me put another frequency counter here and feed f_i here then this will be f_i by n so this is division by n.

(Refer Slide Time: 00:20:23)

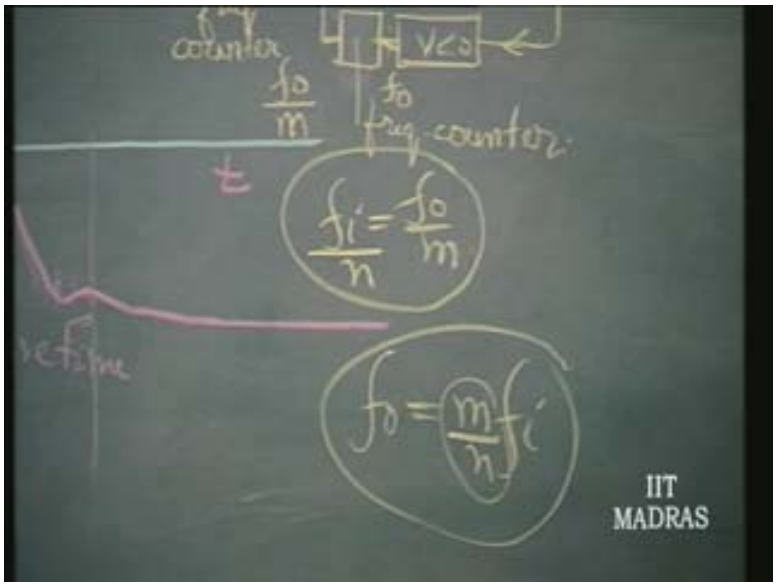


(Refer Slide Time: 00:21:11)



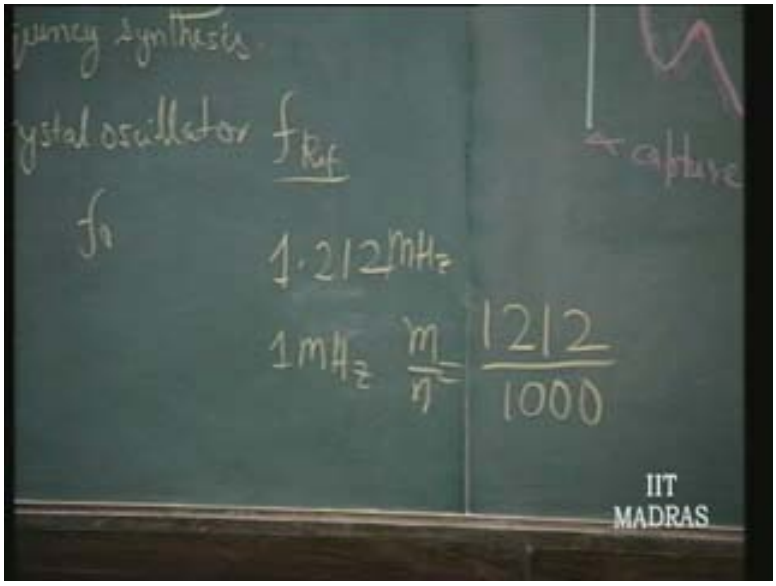
So what happens here is, phi by n is equal to f_0 by m these two frequencies should become one and the same. So f_0 is equal to mfi by n. So by using this combination of two programmable counters I can manage to get any m by n, m and n are integral values.

(Refer Slide Time: 00:21:28)



Now I am doing this because I can synthesize an output which need not be integral multiple of the output input. It can be any number you can just say 1.212MHz I want to generate using 1MHz.

(Refer Slide Time: 00:22:31)

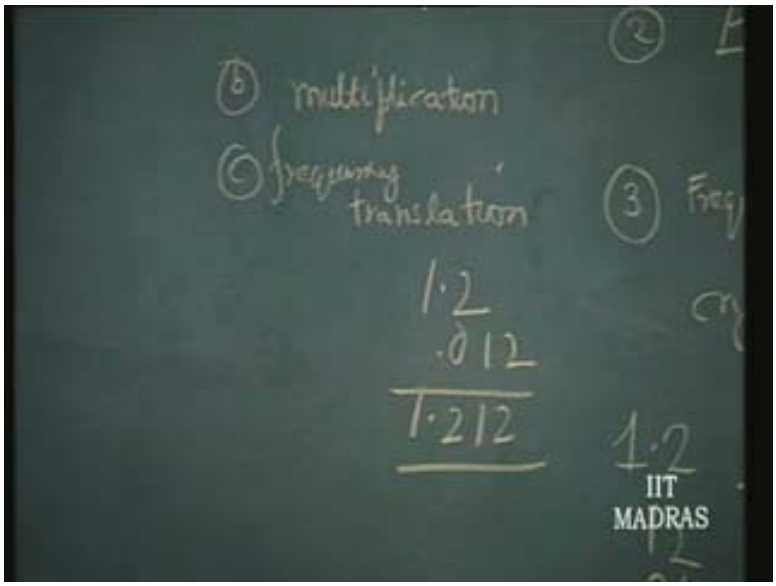


Let us say you want to generate 1.212MHz from an input which is 1MHz, theoretically speaking this can be done accurately by multiplying 1212 by 1000. This is not an easy job, divide by 1000 here and divided by 1212 these two counters are needed. This kind of building counter is not very efficient but theoretically it can be done. Then what else you need for frequency synthesis. If you say theoretically it can be done practically what is the problem. Practically bringing this kind of counter itself is not a normal effect. So how do we generate this kind of technique? I can generate this kind of thing, for example very easily by getting 1.2, how do I get 1.2? Multiply by 12 and divide by 10.

(Refer Slide Time: 00:24:21)

Divide by ten counters are available, divide by twelve counters can be designed easily so you can get 1.2. Then I can get 0.12 because decade counters are readily available. Then I can get 0.012 then I have to add 1.2 to 0.012 and I can get 1.212. This is the most efficient and practical scheme of synthesis. I simply use commonly available decade counters as far as possible and the only deviation I am doing is I am designing a divide by twelve counters in addition which is also possible. Then I go on using decade counters alone and obtain all these. Therefore now I can get any frequency to any accuracy by using this technique of addition or subtraction that is called frequency translation.

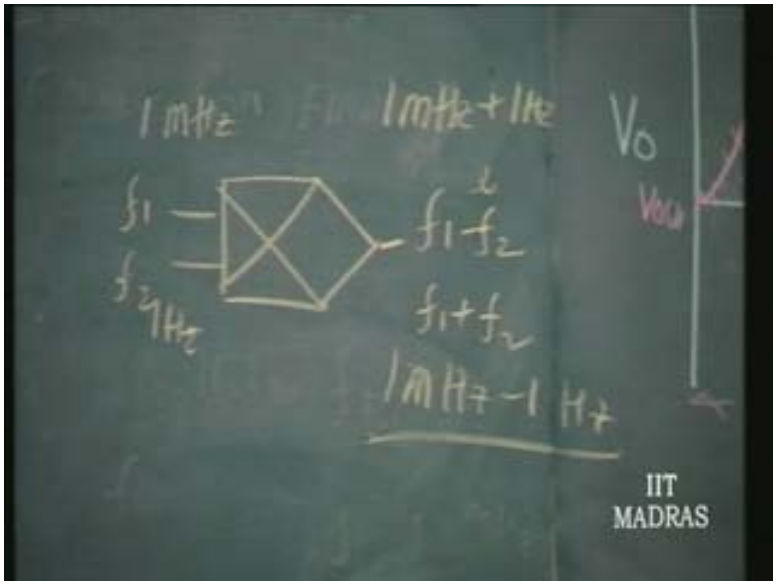
(Refer Slide Time: 00:24:45)



So if you couple on to this scheme of multiplication and division frequency translation scheme then it becomes a very powerful frequency synthesis procedure.

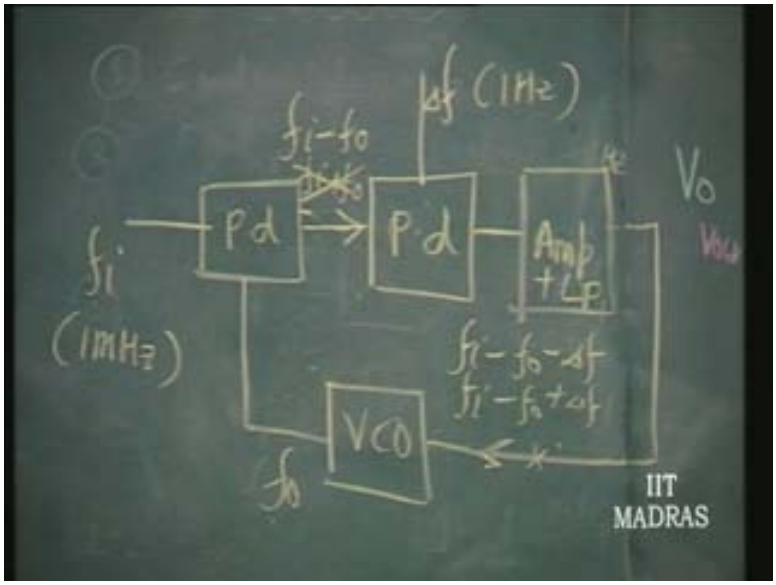
Now how do I do frequency translation?
I simply multiply. So if I use a multiplier f_1 f_2 here you will get f_1 minus f_2 and f_1 plus f_2. What I want is f_1 plus f_2 or f_1 minus f_2 and now we are talking of f_1 is of the order of mega hertz and f_2 being of the order of maybe kilo hertz or hertz. If I want 9.999MHz then imagine you doing multiplication of 1MHz with maybe 1.00 0 01MHz then you have to select the corresponding frequency. That is, you are doing 1MHz with 1Hz then you get 1MHz plus 1Hz, 1MHz minus Hz and you want this component. This is not a practical joke here that you are now thinking was separating out these which is not possible.

(Refer Slide Time: 00:26:32)



Therefore what you must do is, put this in a Phase Locked Loop that is what is called frequency translation effect. You have to use a multiplier but multiplier must be part of the loop. Let us see how it is done.

(Refer Slide Time: 00:29:10)



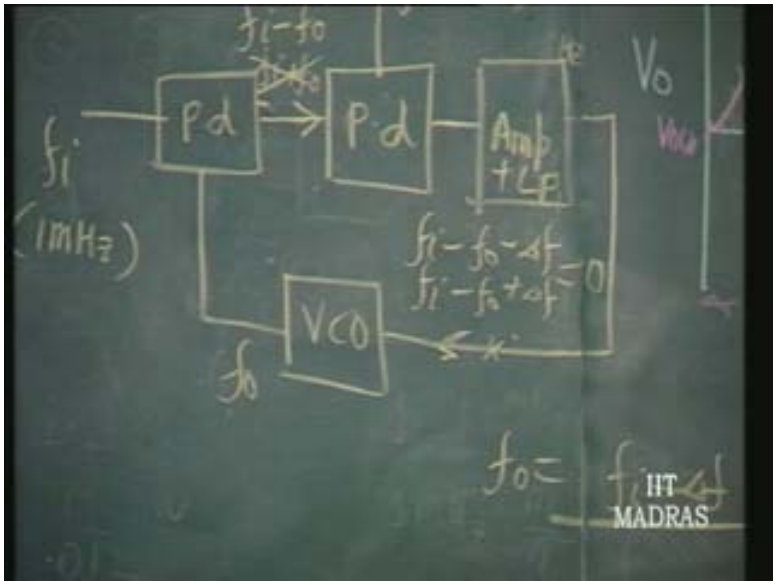
This is fi, this is delta f, let us say, this is 1Hz and this is 1MHz now what happens here? Just for information sake I will keep track of this 1MHz and this is the 1Hz, this is the same multiplier and now I am putting it inside the loop.

What is the basic principle?

This should become a DC that is the basic principle. So this frequency will be uniquely 1 because there is a low pass filter here and if this becomes a DC this should become a single frequency f_0 it cannot be two frequencies. If this is f_0 this is going to be f_i minus f_0 and this is f_i plus f_0. Obviously f_i plus f_0 is going to get eliminated because that is a very high frequency because f_0 is going to be very close to f_i but f_i minus f_0 is a low frequency.

Assuming that it is only one frequency which is the lower frequency that is f_0 is less then f_i this is possible otherwise what is coming here is f_0 minus f_i and not f_i minus f_0. If this is f_i minus f_0 what will be the component here? It will be f_i minus f_0 minus delta f f_i minus f_0 plus delta f. Out of this again if f_0 is less then f_i then this component can be the DC component. This is going to be a higher frequency component.

(Refer Slide Time: 00:29:44)



If f_0 is less than f_i this component can be equal to 0 or f_0 is going to be f_i minus delta f. This is the output we are going to have and you can select the thing. Now how are you sure that it is f_i minus delta f that is going to be output and not f_i plus delta f?
That depends upon the free running frequency of the VCO. If it is closer to f_i minus delta f it will be f_i minus delta f and if it is closer to f_i plus delta f it will be f_i plus delta f. If it is in between you cannot be too sure what is the one that it is going to captured. But this is going to be the frequency selective time.