Analog ICs
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Lecture - 24
Phase Locked Loop

So, in the last class we learnt something about how to do self tuning in a filter. We learnt the control circuitry, how a phase detector can find out the phase difference between the input and one of the outputs namely low pass or high pass outputs and get the average information regarding the phase and compare it with a reference in the comparator output which is used to control the master and this will make the filter get tuned to the incoming frequency. Now this concept has been exploited in what is called as monolithic filters. Currently it is called continuous time filter. We will see why this is going to be called continuous time filter instead of the presently called monolithic filter.

The history of filtering:
Filtering is the most common signal processing activity in electrical engineering. And 80 to 90% of linear signal processing activity is just filtering. There are other non-linear signal process activities. Rest of these linear activities is just amplification. So if you leave out amplification and filtering there is nothing left out in analog signal processing. In the olden days filtering was done by passive LC filters primarily because they are Loss Less Components LLC and there is no problem of stability etc which would normally occur in the case of an active circuit component and there is no need for power supplies are some of the reasons for these becoming the basic components for building any higher order filter.

In fact in the olden days almost all types of filters were designed for very high orders and the tabulations are already there. So this design is already there in a normalized form. Anybody can look at the table and design the filter as per their requirement by just looking at the normalized values. So the filter design was a very simple effect in LC filters for example the frequency was always equal to 1 by 2pi root LC

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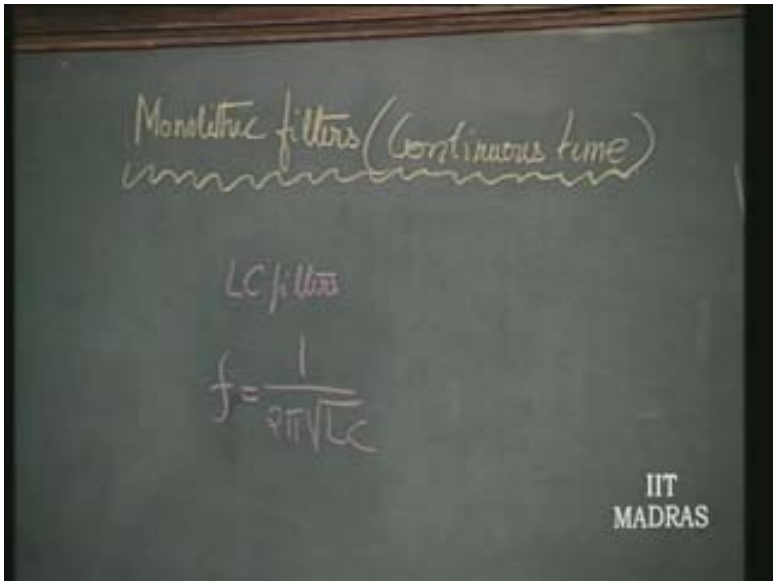

It might be just 1 by 2pi root LC or 1 by 2pi $L_1 L_2 C_1 C_2$ to the power of 1 by 4 and so on depending upon the order of the block, the pole frequencies etc will be determined in the following fashion. Obviously the sensitivity of L and C to f is determined from this, it is 1 by 2 minus 1 by 2 because this square root is coming here. And L and C were very accurately fabricated, one could therefore fix the tolerance of this f very accurately with this passive LC filters. But for low frequency applications we found that these L and Cs used to become very high because of low frequency therefore L and C values will have to be large and the size has to increase and therefore the size was a problem with passive LC filters.

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When people wanted to go to micro miniaturization and monolithic filters there was no way of fabricating L, L was not available. So the question was how to do the filtering? Then we came up with an idea called active RC filters. This was around 1970s when the op amp had become available the transistors were also very much in usage and people were fabricating some small scale integrated circuits at that time, differential amplifier and op amp etc and using these small scale integrated circuits one could get rid of L by simulating L or think of the whole process of filtering as a problem to be solved wherein you are using op amp in combination with R and C in order to simulate the filter in its entirety.

The filter design is a question of solving differential equations or integral equations. Therefore using what it is called as an integrator block one could therefore solve any filter problem using merely active RC components. But however the disadvantage of this is that active devices are proven to stability problems, the op amp etc has frequency limitation. R and C's are to be accurately designed. That was not a problem in discrete circuit design using active components along with R and C discrete components, the thin film thick film components etc where you could build fairly good active RC filters. These replace most of the LC filters when these integrated circuits were made available.

The stability problem was there, the size was much reduced. But still this has not solved the problem of making the entirety monolithic because in the monolithic filter R was not satisfactory because it had very poor tolerance of the order of 30 to 40%, C was also having poor tolerance about 30 to 40%. Therefore effective tolerance of frequency in this case was 1 by 2 piR_C was unacceptably large because this is 30 to 40%, this is 30 to 40% and effectively the frequency was deviating by 60 to 80% from what you wanted. This was not acceptable because of poor tolerance.

Not only that the Rs and Cs had poor temperature coefficient, large temperature coefficient. So this was not acceptable for any design of a decent filter in monolithic form. And at that time a solution was proposed as to using the active device in a monolithic block itself as an integrator. It has its parasitic capacitor or small capacitor which can be used for fixing the time constant. And then obviously you had a problem because it is parasitic or it is characteristic to that particular device, how you can get rid of poor tolerance in large temperature coefficient? There the idea of master slave concept was proposed.

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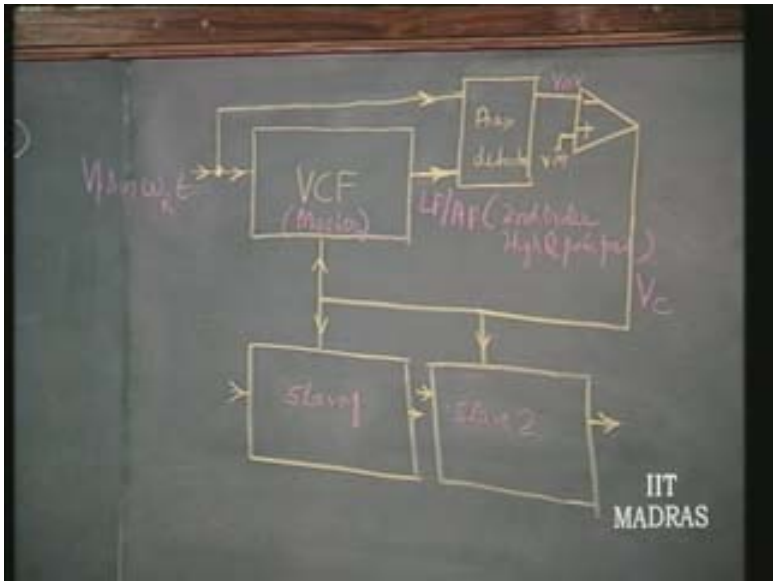

The master slave concept is exactly similar to our concept of current mirror wherein we used inside of voltage controlled filter a diode a transistor as a diode in the negative feedback configuration to make it accept a collector current of whatever that you are fixing and develop a voltage to sustain that current and there after use this voltage in order to bias all the other base to emitter junctions so as to sustain the same current in all the transistors. The same principle in a sort of little bit complicated way is going to be used here to get over the major problem of poor tolerance and large temperature coefficient.

The assumption is, in a fabrication of a monolithic component all the components have same temperature coefficient and same absolute value. If all components have same absolute value under the same condition of operation and same temperature coefficient then let us assume that we have designed a voltage controlled filter block using the same blocks the KHN filter block wherein the resistors are replaced by FETs. So, the control voltage for the FET is going here and the input and the low pass or high pass output is taken and you use a phase detector to get the V average corresponding to the base and compare it V reference and control this.

Now if this works satisfactorily we have shown in the last class that this will be automatically tuned to the incoming frequency which is omega reference. So this control voltage will at all times adjust its value at all temperatures under all operating conditions it will adjust itself such that this particular thing band pass filter or the pole frequency of this filter the low pass or high pass is automatically tuned. That means for this we know that omega r master is equal to 1 by r_{ds} of the FET into C master.

So r_{ds} of the FET into C master. for these slaves we have omega slave 1 is equal to 1 by if you say that similar FET is used for the control applying similar control voltage to the gate our same control voltage to the gate then r_{ds} will be the same in all. So r_{ds} by C slave

and omega$_{s2}$ is going to 1 by r_{ds} into C_{s2} so on and so forth. You can connect any number of such components like this without any limit. That means all these salves get the same control voltage that the master gets.

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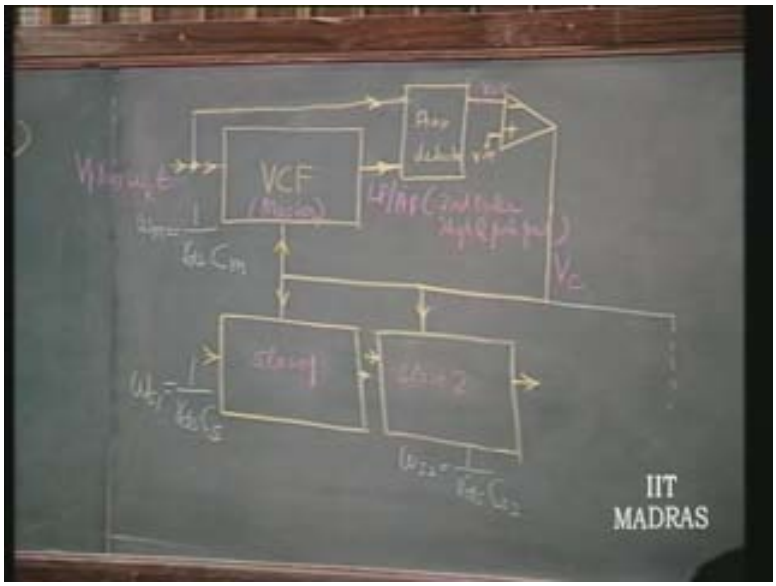

Now it is established that omega m is same as omega R by the feedback loop at all times.

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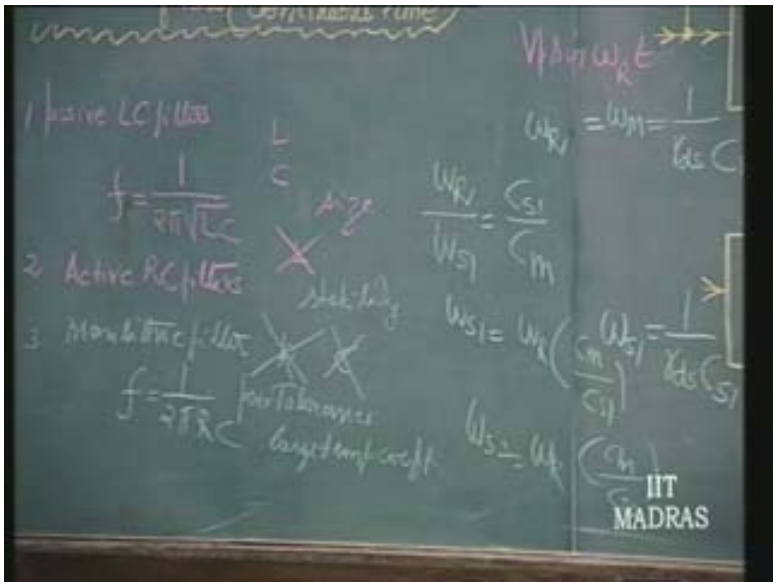

Now let us take the ratio omega R by omega s_1 is equal to C_s by C_{s1} by C_m or omega$_{s1}$ is equal to omega$_R$ into C_m by C_{s1} omega$_{s2}$ is equal to omega$_R$ into C_m by C_{s2} this was established very clearly. Therefore now it is a constant reference frequency which can be

made as a table as you please into ratio of capacitors belonging to the same block. Therefore these ratios will track very well as far as the absolute value of the ratio is concerned and temperature coefficient is concerned. Therefore this is fairly accurately fixed. Therefore you are capable of now fixing independently the pole frequencies of all these filters which you can now connect in any manner you like, the input and output are free.

So you can connect these filters in any manner you like to formulate a complex higher order filter block, any nth order filter you can well using cascading of these slaves. Then all these filters will now have a normalizing frequency omega which is under your control. That means you can make these filters become programmable by simply changing omega R they will retain their characteristics.

Suppose you have designed these filters so that these filters are showing you 10th order Butterworth characteristic that is designed based on what is the Q of this block what is the home frequency etc. As I change omega_R it will remain 10th order Butterworth at all times but its cutoff frequency can be continuously varied. So this is the advantage of this kind of filter design so this has been now adopted by monolithic filter designers as one of the techniques in realizing analog VLSI filters.

Now the only limitation that comes about is because of the fact that you are using a FET here whose dynamic range where it is operating as a linear resistor is quiet small which only means that the dynamic range for which this filter block can be used is quiet small. You can come up with techniques of making the dynamic range larger and that will be another research contribution here in this concept of continuous time filter block. So these filters are now-a-days implemented, for example, in television receiver this was implemented on an experimental basis by Philips long ago around 1980s.

This idea was proposed around 1976 or so and around 1980 or so Philips at UK built an IC it was not op amp filter but it was a gyrated type of filter were inductors were simulated it does not make any difference where how you realize this filter. There was a master filter design and then the slaves were designed. The advantage of this kind of filtering in this television block was you had a synchronizing frequency coming from the transmitted information and this synchronization frequency could be used as the reference frequency to tune all the filters the video filter, the audio filter everything was tuned by a master which was getting its input as the synchronization frequency. And that way it was tracking whatever was happening with at the transmitting end.

There were large number of such filter blocks needed in a television receiver and that is when it was used for the first time as an application. Now of course it is being abundantly used universally in all analog signal processing blocks. This whole idea of master and slave was evolved at IIT Madras as an undergraduate project around 1976 and this was published in proceedings IEEE of the same year.

Now we will discuss about a concept which is again frequency locking similar to what we discussed earlier. But this is called Phase Locked Loop popularly known as PLL. The

PLL concept was in existence for a long time lying dormant somewhere. A few people who knew about PLL were only microwave engineers and there are only a very few of them in the world today. Therefore only those people needed this concept because it was very difficult for them to get stable frequency output and they had to take recourse to what is called, from low frequency stable output they had to multiply it to higher levels. This kind of frequency synthesis was quiet [e…] for microwaves and for microwave itself considerable advancement took place during Second World War the whole concept of radar and microwave sort of advancement to place then and people were using this concept of Phase Locked Loop during that time for obtaining stable frequency output. But very few people understood the whole concept.

Surprisingly it was proposed only for a radio receiver it was not proposed for any radar or frequency synthesis. Somebody wanted ideas for a cheap radio receiver. Lots of ideas came, one such idea not very simple of course it was very complex at that time but a novel idea was phase locked loop. The person who had proposed it even though he brilliant was disappointed because it was thrown off and the idea that was taken up was what is currently called as superheterodyne receivers' key which was the simplest and the cheapest. And this Phase Locked Loop was just kept everywhere.

Then when monolithic integrated circuits were coming into the market around 1970s again those very few analog circuit people were looking for some component which otherwise would not have become acceptable because of its need for usage of large number of active devices but can be used in a communication application. So such a device that was brought out was the Phase Locked Loop. Of course again if you make these multinationals take up any responsibility of fabricating anything the first thing they would do is popularize the IC

Again applications of Phase Locked Loop were asked for and a large number of such novel applications were put together in the form of a manual and given free of charge to everybody to learn the use of this component then thereafter it became very popular. That is the history of Phase Locked Loop. Therefore let us see what Phase Locked Loop is. Conceptually it is totally different from all those concepts we have been learning so far in control. Actually it is also a control circuit that has the basic building blocks. You have obviously a phase detector.

How a phase detector can be designed as a monolithic block?
It is nothing but an XOR gate emitter couple logic. It has two inputs obviously; the phase detector is nothing but a multiplier in combination with a low pass filter.

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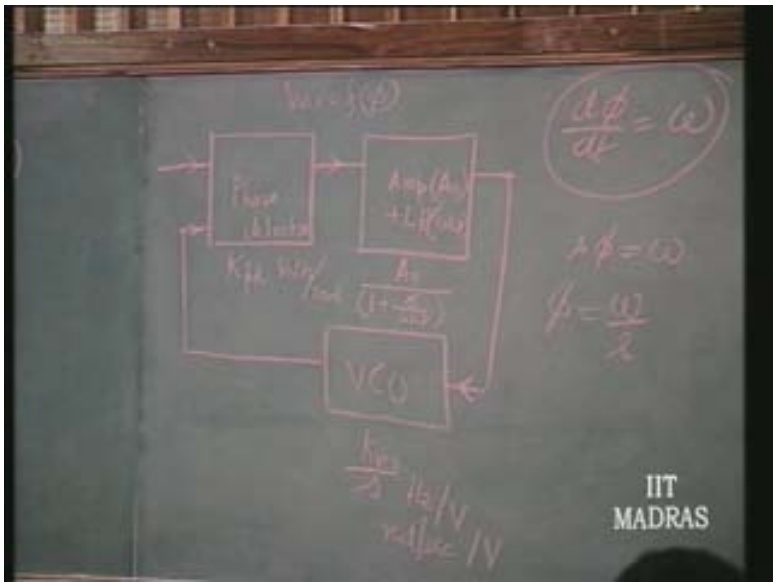

The low pass filter is nothing special. I am going to use an amplifier here to improve the loop gain of this loop because if it is a control loop always you have to improve the loop gain. Therefore obviously we have to put an amplifier plus low pass filter. So the low pass filter needed to average out the multiplied component is put along with the amplifier, it is just an arrangement. And then you get the amplified average output and this has to be converted back to phase information. This information which is a voltage has to be converted to phase. As a first step we convert it into a frequency because we know that frequency and phase are linearly related, d_{phi} by d_t is nothing but omega.

Rate of change of phase is nothing but frequency so it is linearly related. Therefore I put a voltage to phase converter or voltage to frequency converter which is nothing but a VCO. We already studied as to how VCOs can be built using an integrator and a Schmitt trigger. Therefore we know all the basic building blocks that can formulate what is called as a phase locked loop. Now, if such a loop is built we have to understand how this now functions in locking on to the incoming phase.

Let us assume that the input is coming here and the phase detector is giving an output corresponding to the phase. So the phase detector has what is called as phase detector sensitivity which we defined as equal to K_{pd}. We already defined this for the phase detector we built. It will be so many volts per degree radians of the phase. It is so many volts DC by degree radians which is the phase detector sensitivity K_{pd}.

What is the V average output?
V average is going to be a function of the phase. So phase detector sensitivity is nothing but delta V average by delta phi for any given circuit. And as far as amplifier is concerned its sensitivity is defined as nothing but A_0 gain. As far as the low pass filter is concerned, we will take the simplest low pass filter that is the first order low pass filter

then you have the low pass filter cutoff frequency we will call it as $omega_{LP}$ which means this A is going to be A_0 by 1 plus s by $omega_{LP}$, that is the sensitivity of this. Then we are getting this DC where this DC is converted it to frequency here. That means DC to frequency converter or it is nothing but K_{VCO} which also we defined as so many hertz per volts or so many radians per second per volt.

If it is omega output it is radians per second per volt or hertz per volt. So here it is volts per radians and here it is a ratio. We assume that this is linear and if it is non linear we will assume this as a small signal characteristic, we assume it to be linear characteristic of each of the blocks. This is a Phase Locked Loop, it is the phase so from here to here the frequency is automatically getting converted to phase because this is a phase detector it is going to respond to change of frequency or change of phase which is nothing but frequency.

Hence, strictly speaking if it is to be converted as phase, what should happen? What is the relationship between omega and phi in terms of Laplace? It is s into fi is equal to omega or if it is phase it is omega by s. Therefore, if it is phase that you have to put you have to put here this as K_{VCO} by s. That means here this is going to respond to the phase at this point and not frequency. So the response for this is going to be like this, the input is a DC which is varying corresponding to the phase you are changing here so that corresponds to K_{VCO} by s which means it is radians per volt.

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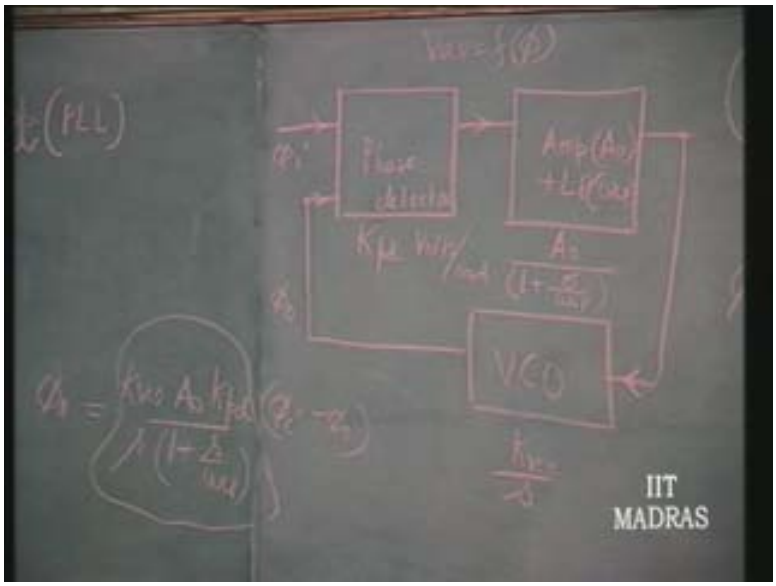

Now we have understood that this is the incoming phase and this is the output phase. If this is phi and this is phi_0 this is with reference to some common reference whatever it be. What is it going to respond is phi_i minus phi_0 phase difference and output of that is going to be K_{pd} times this and that DC is going to be multiplied by A_0 by 1 plus s by $omega_{LP}$. It is not a DC it is a low frequency component. The average is not necessarily a DC if it is time varying therefore phi and ph_0 are time varying so the average need not necessarily

be a DC it may be a low frequency component therefore this it the attenuation or amplification factor of that. This average component is going to be multiplied by K_{VCO} by s and you get phi_o here.

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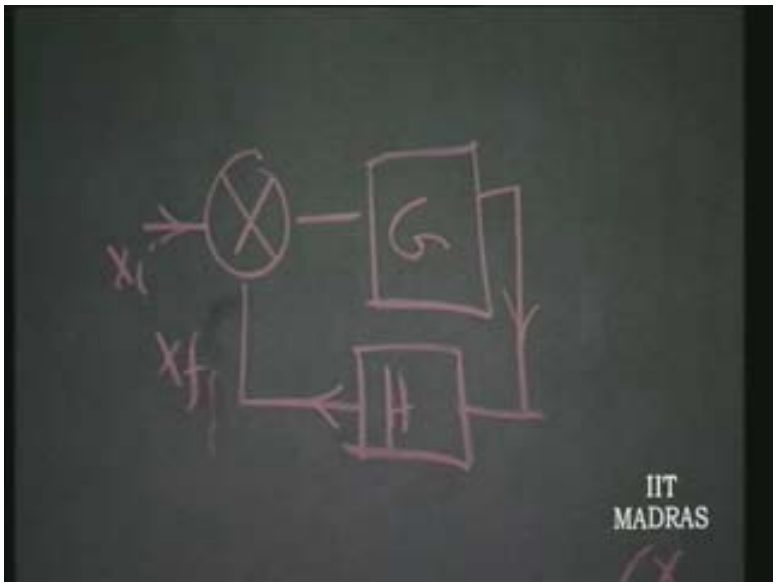

Therefore you can consider this as nothing but, for a feedback amplifier stage what is this going to be?

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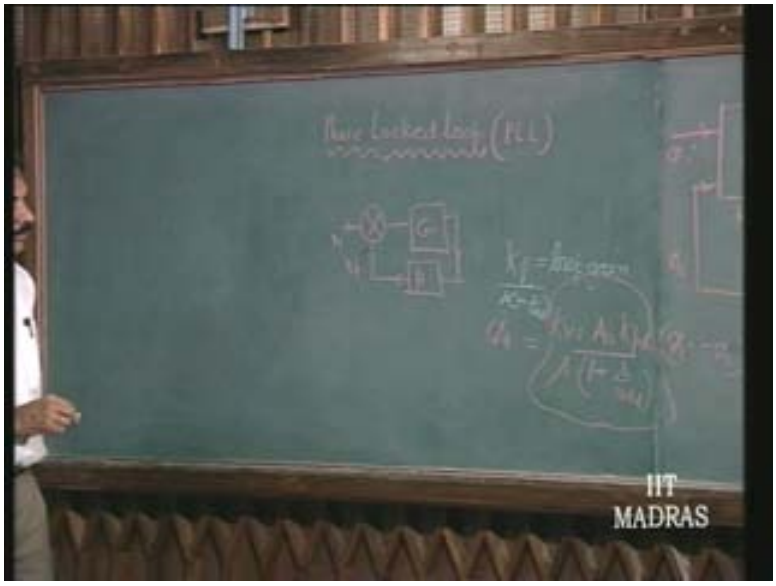

You already learnt about this control loop X_i X_f so what does it mean? This is nothing but G H which is called loop gain. So this whole thing is called loop gain. We will call it K_l as the dc by s into 1 plus s by $omega_{LP}$, this is the DC loop gain.

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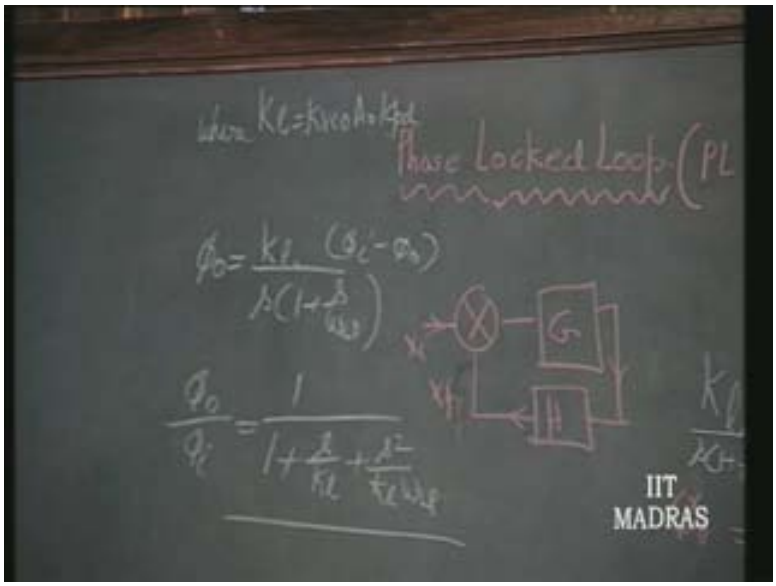

So phi_0 is going to be K_l is equal to K_{VCO} into A_0 into K_{pd} it is simply going through the loop and multiplying all the sensitivity factors where you get the dc loop gain. K_{pd} A_0 K_{VCO}, K_l by s into 1 plus s by $omega_{LP}$ into phi minus phi_0 if you rewrite this as phi_0 by phi_i you will get this as 1 by 1 plus s by K_l plus s square by K_l $omega_{LP}$. If K_l is very high if the DC loop gain is very high this will become equal to 1 that is like in any case the unity gain amplifier of ours.

For example, if this is V_i and this is V_f then it is established that if G H is very high V_i is equal to V_f that is voltage follower. Similarly Ii is equal to If which is current follower. You have this similar concept in voltage follower, current follower and now it is phase follower. That means this is very nearly equal to 1 or $dphi_0$ by, because we do not have any absolute phase here, there is nothing like phi_0 by phi_i it is always with respect to some common thing.

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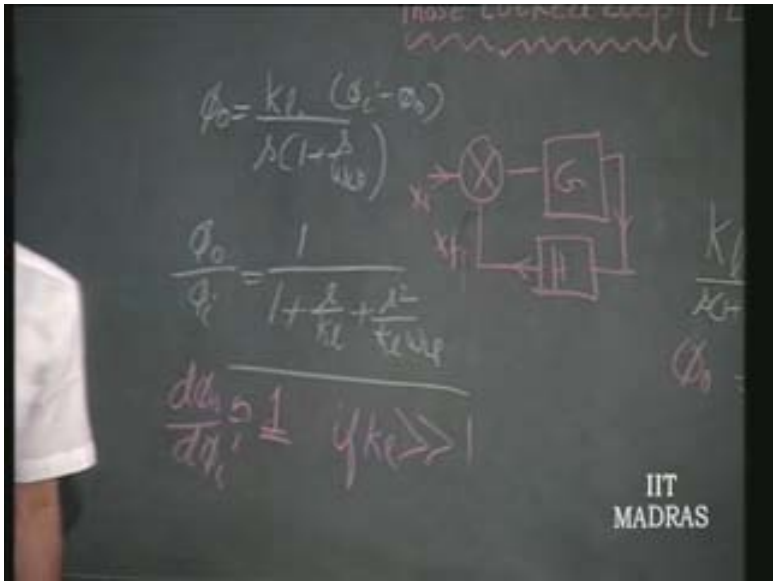

So phase difference dphi$_0$ by change in phase at the output will track the change in phase at the input at all times. Therefore this is a phase follower equal to 1 if K_l is much greater than 1.e. This is the linear analysis for a Phase Locked Loop and what is therefore called natural frequency of this loop. You can call this as the natural frequency of the system, (omega$_0$ is root K_l into omega$_{LP}$). Any such transfer function can be written as 1 by 1 plus s by omega$_0$ Q plus s square by omega$_0$ square where omega$_0$ is going to be root Kl omega$_{LP}$ that is called the natural frequency of the system.

It simply means that if it is high Q system it will give you maximum response at the natural frequency and Q is going to be equal to by comparison you can see that Q is going to be root Kl by omega$_{LP}$. Obviously we want to make omega$_{LP}$ frequency very small and K_l very large and invariably most of the phase locked loops are very high Q systems.

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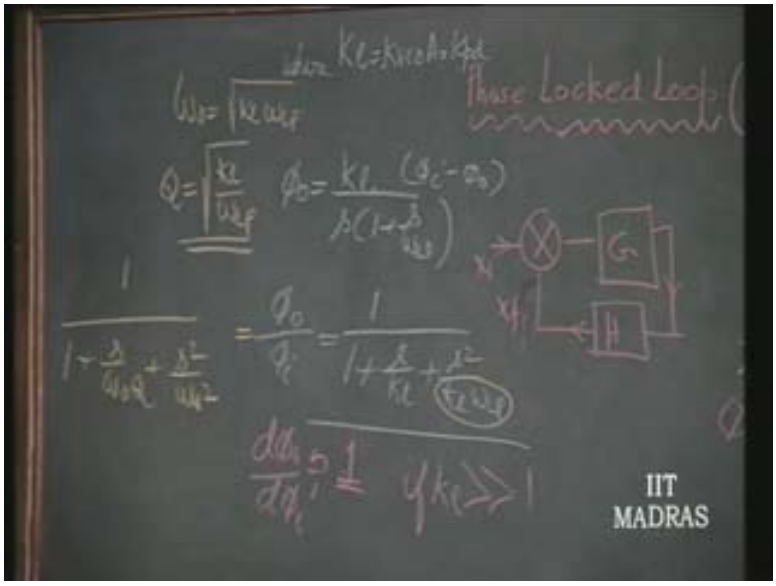

Now this is important, K_l is what is called as the DC loop gain, root K_l into $omega_{LP}$ is called the natural frequency of the phase locked loop and if you plot this magnitude of phi_0 by d_i versus the frequency of change of phase, the phase is the input here but that phase itself can change at a certain frequency that means it is called, phase is changing at a certain rate that is called frequency and that itself can change that means it can be a FM.

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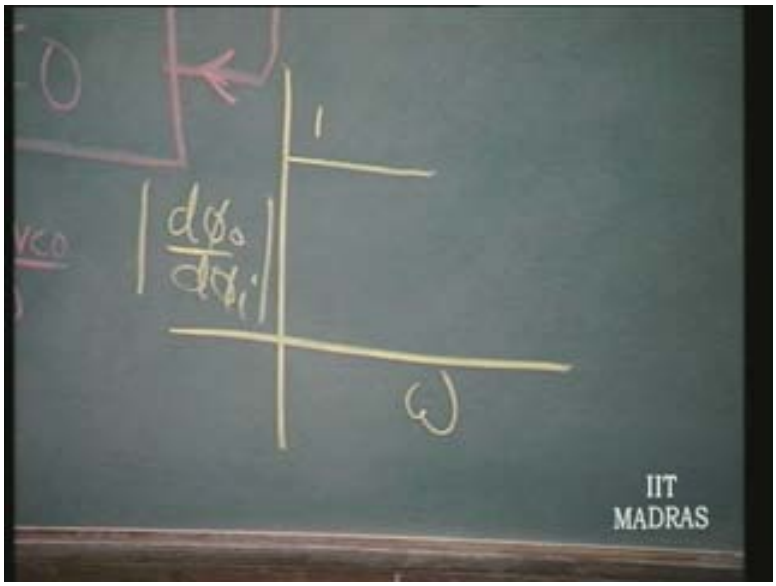

If there is no change in phase there is no frequency but if there is change in phase there is frequency. Now this frequency itself can change that means there will be FM. That means, if I give an FM here and that FM is modulated at a certain frequency it is that

frequency I am talking of and not the carrier. If the rate at which the frequency carrier is changing and then this will be 1 and here this is $d\phi_0$ by d_i what does it mean this also equal to delta ω_0 by delta omega i because they are linearly related. This is how I come to a conclusion that if there is phase locking there will be frequency locking necessarily.

I cannot discuss it in terms of frequency changes because I am assuming a linear system. So I have to necessarily discuss it always in terms of small changes in phase then I go back and I say once phase lock occurs there must be frequency lock. That means invariably if I am inputting a certain frequency here the output has to track the input frequency. So these two frequencies will always be one and the same and that is why in a Phase Locked Loop you have frequency locking. This is the basic concept of Phase Locked Loop a very simple concept. It is a concept which is quiet often understood in controls when we deal with amplitudes whereas here we are dealing with phase and that is the only difference.

At a certain constant frequency input omega i is the same as what is called free running frequency. If there is no input frequency at all VCO will run at a certain frequency because there is a quiescent DC. This is a quiescent DC and VCO will run at certain frequency. There is one frequency input there is no input here so what will be the output? It is just the same frequency will come with a small value.

Actually if it is an ideal multiplier nothing should come because there is nothing connected here. If at all something comes this high frequency comes and that is getting filtered out by the low pass filter so nothing comes here. That means this DC voltage remains the same and this continuous to run at the same frequency. So this is called the free running frequency of the Phase Locked Loop let us call it ω_0 Q. Like quiescent voltage for a voltage amplifier that is the starting point around which voltage can vary in a quiescent voltage. Here this is the starting point around which frequency can vary. So I assume there is no input and I have shown that this free runs at ω_0 Q.

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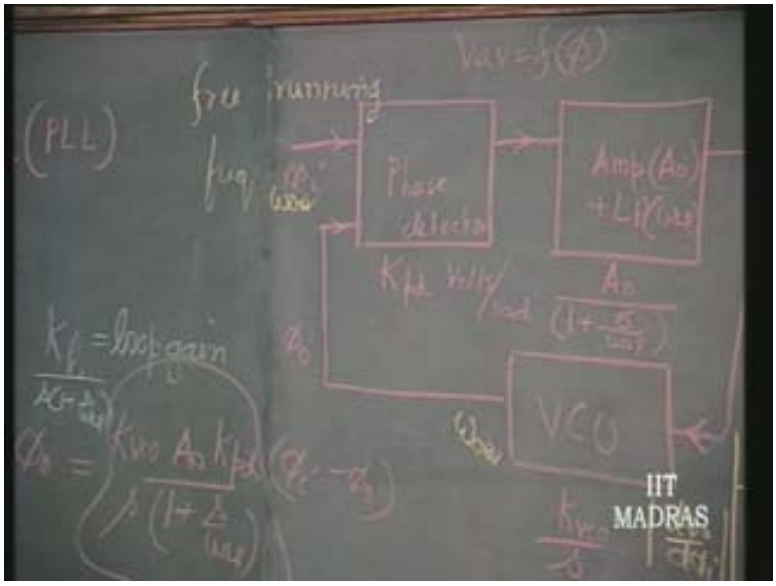

Suppose I give $omega_0$ Q here this is $omega_0$ Q, this is $omega_0$ Q now what should happen is, according to the principle of Phase Locked Loop there is a same frequency and nothing should happen, that is this frequency should not change because I am feeding the same frequency at the input which means the output here should be zero. That means the control loop should adjust its output so that this is zero, when does it happen?

When do you get zero output in a phase detector?
It is when the phase difference is 90. When the phase difference is 90 degrees we get zero phase shift and that is the quiescent state of existence. So automatically if I feed an input frequency which is the same as the free running frequency the quiescent phase shift is adjusting itself to be 90 degrees so as to make this voltage equal to zero and so as this does not change so that this volt frequency does not change. So the quiescent phase shift is established when incoming frequency is same as free running frequency. Now the frequency is going to change from $omega_0$ Q.

If this frequency changes from $omega_0$ Q by a small amount then this should follow, how does it follow? Frequency will always be the same but how does this loop make it follow?
We now said this is going to be different from $omega_0$ Q by a small amount. That means these two frequencies are different corresponding to which now this will establish an average which is going to be magnified and applied here and which will change it to that frequency. That means, now there will be a phase shift which is different from 90 degrees because we need an error output here to sustain that frequency. So this output will correspond to the DC voltage that is necessary to sustain this change in frequency. So omega i which is different from $omega_0$ Q omega i minus $omega_0$ Q by K_{VCO} is the voltage necessary here and that divided by A_0 is the voltage necessary here. Therefore that is the voltage appearing as the phase detector output so you can find out the phase difference corresponding to this. That means it will keep on changing the phase from 90

degrees on either side of 90 degrees depending upon whether omega is higher than $omega_0$ Q or less than $omega_0$ Q.

And now it can go on up to the point where the phase difference becomes equal to basically 180 degrees or 0. That means change in phase shift becomes equal to 90 degrees on either side of this 90 degrees it can and that is what is called the lock range. Beyond this range it cannot any longer sustain this condition that input frequency should be same as output frequency.

In any give Phase Locked Loop if everything else has full dynamic range then the lock range is determined simply by this K_{VCO}, A_0 and K_{pd}. So you can keep on making this omega i minus $omega_0$ Q by K_{VCO} by A_0 should be the maximum voltage you get for a phase shift of pi by 2 and that will give you omega i limit on either side of $omega_0$ Q.

If you take a linear phase detector it is going to be simply K_{pd} K_{VCO} A_0 into pi by 2 if it is linear because K_{pd} into pi by 2 is the maximum change. K_{pd} K_{VCO} and A_0 into pi by 2 is the voltage being the maximum voltage change that can occur at the output and that times A_0 is the maximum DC change and that times K_{VCO} is the maximum deviation that can occur at the VCO. So this is called the lock range and this lock range is there around $omega_0$ Q on either side of $omega_0$ Q so $omega_0$ Q delta minus delta omega l to $omega_0$ Q plus delta omega l actually is the range within which this Phase Locked Loop is going to have the frequency getting locked at all times. Therefore that is called the lock range.