Analog ICs
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Lecture – 16
General Purpose Operational Amplifier-747
And
Voltage Comparator - 711

So, in the last class we were discussing the basic configuration for the operational amplifier and we saw how it is made up of three stages namely the input stage, intermediate stage and output stage. Now, coming to specific popular op amps we would like to see almost all components of this particular op amp. So obviously 741/747 are the operational amplifiers which are general purpose operational amplifiers available. Almost every manufacturer makes this and matches their configuration similar to this. Let us see how various details such as protection, compensation, biasing etc are taken care of by this configuration.

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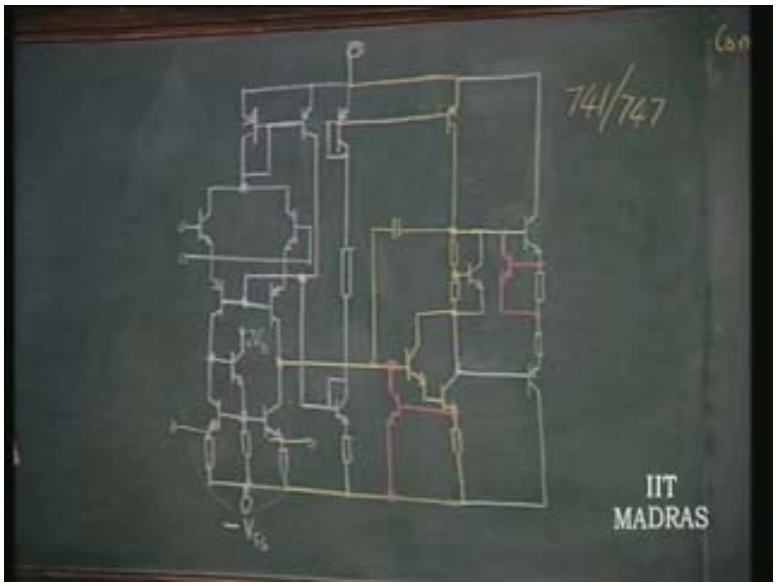

Let us quickly identify here the input stage in white color. Obviously to the input stage we have decided to use NPN current sink as the active load. You can see this active load here, this is the same block as discussed earlier with the current amplifier put there so that the current reflection here is exact. This is nothing but current mirror active load using NPN structures.

Now, in our earlier basic configuration we had not put any of these resistors. Now note that we have put resistances in the emitters, it is not really serving the purpose of making the currents equal. Currents were more equal before these resistances came into existence because resistor ratio is not all that better matched than the geometry themselves. But we

are intentionally putting resistive [d…]. One purpose is automatically served, that is output impedance is increased further. But that is a minor purpose for which it is put. The major purpose for which these resistances are put is for offset compensation.

If these resistances are equal because of the transistor mismatch these two currents will be unequal. If these two currents are unequal even when the input signal is 0 there will an input current into the next stage. If there is an input current to the next stage automatically DC current we are talking of then the output is going to the saturation. So, in order to reduce the output offset one technique is of compensation is to make these two become unequal in a direction such as to compensate for the mismatch. So now, I am introducing two unequal resistances here R_1 and R_2 to make the output offset goes to zero. This is an easy technique of compensation. How do we do it? The manufacturer puts equal resistors then he brings out these two terminals and mentions these as offset compensation terminals.

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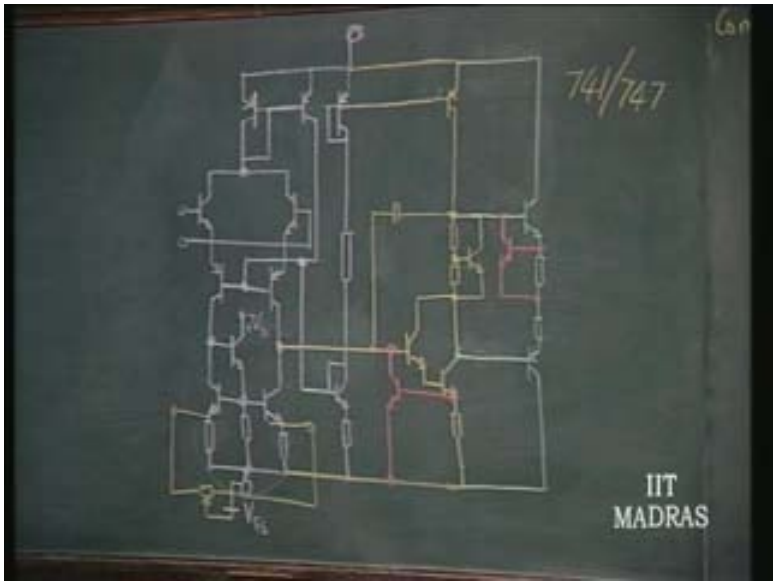

One has to put a potential divider between these two and the centre tap one will connect it to minus V_s. If it is centre tapped then equal resistance will be across this. If the tap is deviating from centre position then we will be generating unequal resistances. Depending upon the kind of offset you can either increase this resistance relative to this or decrease it this relative to this just by using a part here. So this is an externally connected component which is nothing but the potentio meter with the centre tap connected to minus V_s. This kind of compensation is available in certain 741s where these terminals are brought out. If these terminals are not brought out brought out you cannot compensate obviously. So, in certain packages you will find these packed terminals are in fact brought out. Then compensation can be easily done using this procedure.

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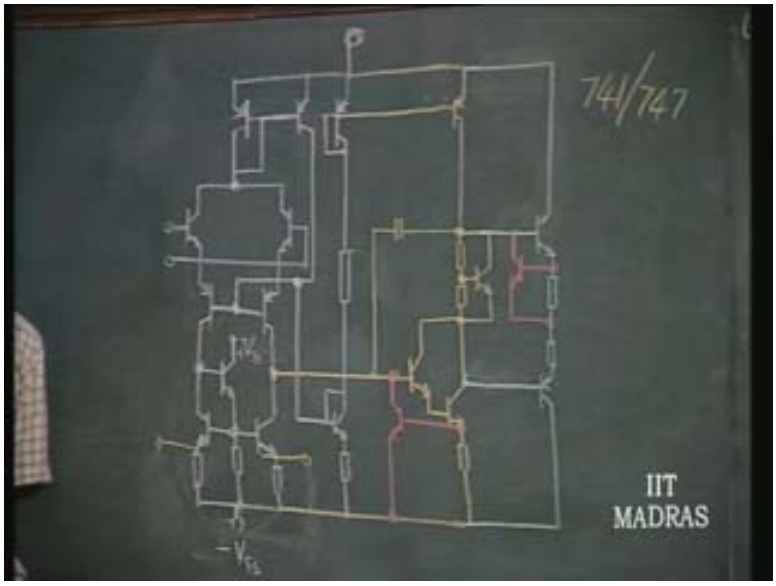

We will remove this because this being an outside component we should not clutter this already complicated circuit with all these. In case of offset compensation we need this potential meter. Now, this resistor is nothing but the bleeding in order to make this transistor operate sufficiently high current so as to prevent the beta fall off so this is connected to plus V_s. Now, for this structure here if we have decided to use NPN current mirrors we must drive it by means of PNP pair. But we do not have a good PNP pair so what do we do? We now use a cascading of NPN with PNP. So in such a manner as far as signal is concerned the base current of this is NPN base current so emitter current is going to be definitely beta times current. So the effect of input impedance etc is going to be retained because of good beta.

This current is going to be the same as emitter current of this structure. And here the base is connected to ground therefore this is a common base structure for signal. So you can see here that by using this structure I have got almost a PNP like structure with high beta. So this is the trick that has been played in 741 input stage in order to get PNP like performance using a combination of NPN and PNP structure and that is taken care of.

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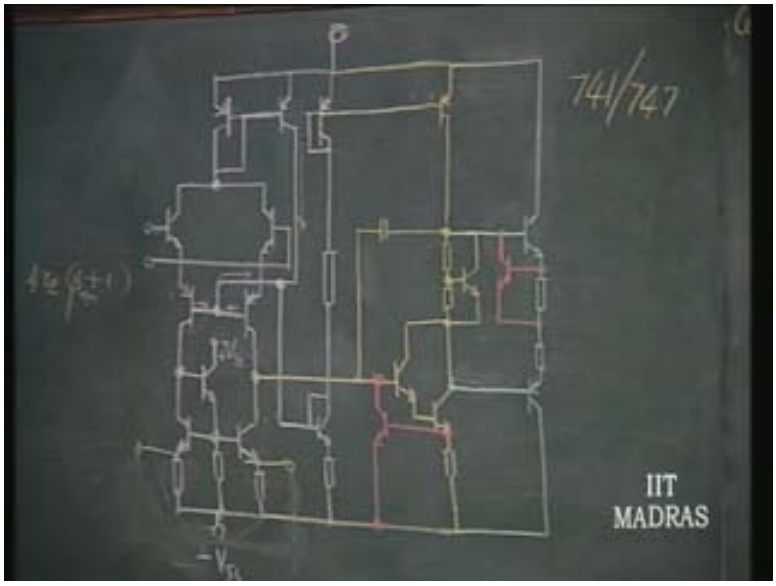

Hence the input impedance is going to be $2R_E$ of this and $2R_E$ of this as R_Es are going to be the same because the operating currents are the same, so it is $4R_E$ into beta plus 1 where beta is that of NPN. Now one thing has to be emphasized here that this base current has to flow somewhere because these both will have finite base currents flowing like this because betas of these are not going to be too high but it is going to be pretty low. So this substantial current is now going to flow through this and of course through this. This is the current mirror in the reverse so it will sense the total current here which is the bias current and feed it here and this current is fed back to this here. Here this is the low valued current mirror and you have to now put a resistance in the emitter. So this is the low valued current that is generated. That low value of current is used in generating the fed back currents. These are the two fed back currents. This is the base current and this is the total collector current getting reflected here.

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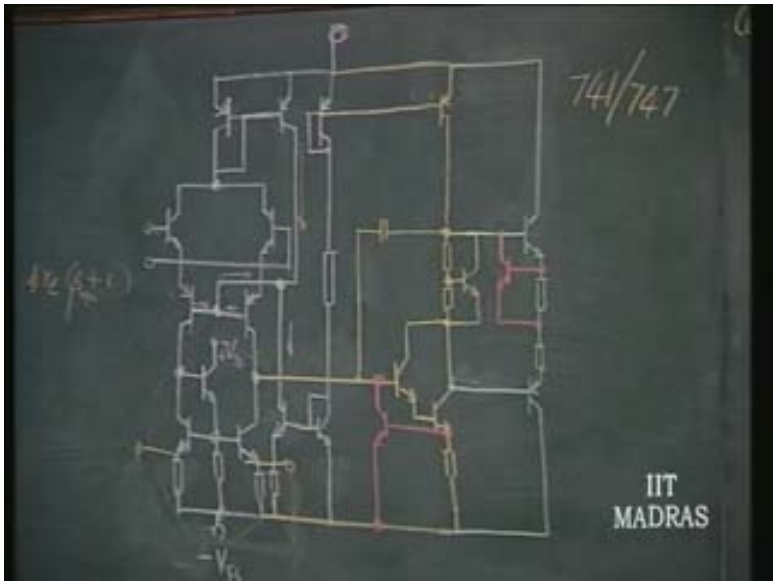

That means the emitter current of the whole thing is getting fixed by feedback now. So this current shall become equal to this plus this which will determine the operating input current of the input stage. So let us say this is I dash then this is going to be I dash so these two currents will be I dash by 2 and I dash by 2 so these two base currents will be I dash by 2 beta PNP the same thing.

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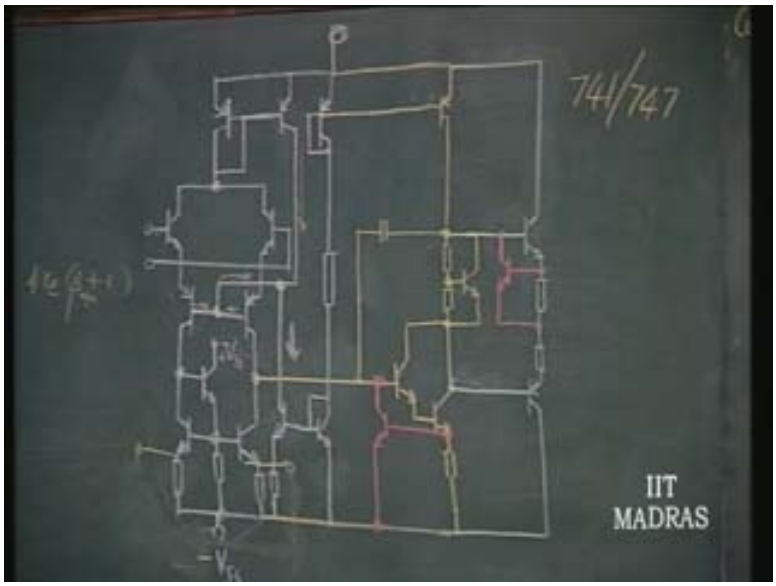

So what will be this current?
This current will be I dash by beta PNP. So I dash by beta PNP which is considerable plus i dash shall become equal to I. So I dash by beta PNP plus I dash is equal to I.

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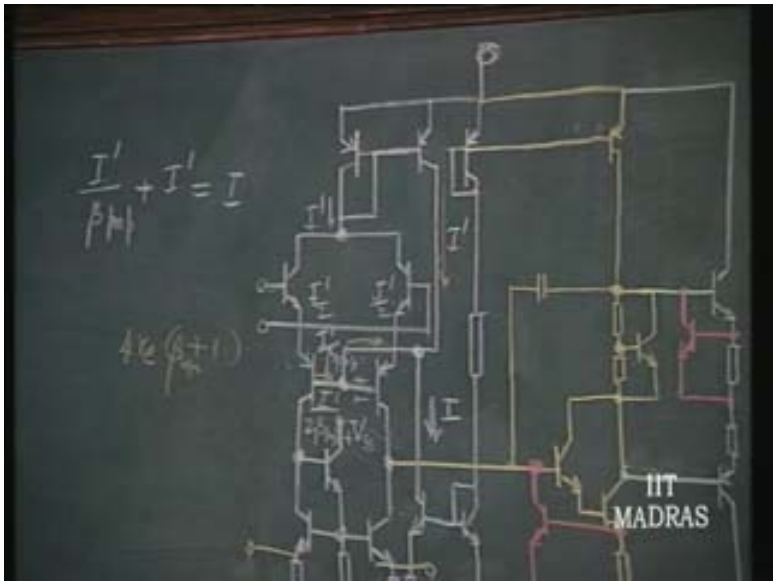

You can see that the bias current of the input stage is fixed in a pretty complicated way compared to the conventional scheme of straight forward current mirror bias. The mirror reflected current is made equal to the fed back current which is equal to the emitter current of the operating transistors. So, for the given configuration please find out for the values of resistors etc assuming supply voltage V_{ss} and minus V_{ss} as 12V find out the value of the operating current I dash, beta PNP you can assume it something like 10 and you will get the value of that. Compared to this we can see how simple the structure was for the one we discussed in the last class. That means if bipolar transistors of good PNP were available we could have straight away gone for the conventional biasing scheme instead of adopting all these round about way of biasing.

Next, this is the reference current V_s minus V_s that is $2V_s$ minus $2v_{gamma}$ by r which is the reference bias current which will bias all the stages in this. So, the ratio of these two currents is the one that is going to be now made very high. This divided by this is made very high so that this current is made current of the order of micro amperes using a resistance of the order of tens of kilo ohms.

Coming to the intermediate structure obviously we have $2V_{gamma}$ here, V_{gamma} and V gamma and we are putting Darlington pair here. So the input stage impedance also is boosted up by the Darlington pair. Not only that this potential is maintained as the same potential as this so the current reflection is good. The early effect is not coming into picture. Now here forget about these transistors. These are coming only as protection transistors.

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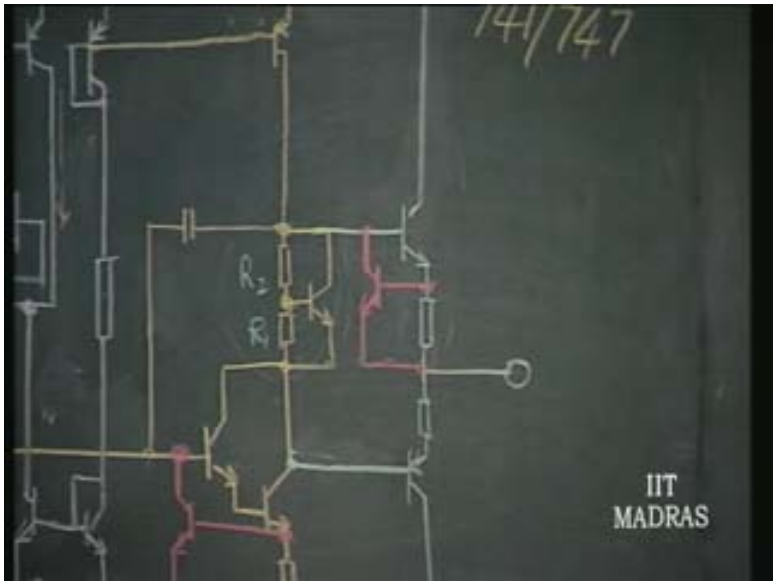

This the compensating capacitor and this portion of it is nothing but voltage reference which can generate a voltage which is nothing but V_{gamma} into 1 plus R_2 or R_1 necessary for biasing class b in class ab mode of operation. So this R_2 or R_1 is made less than 1 so that the voltage between these two is equivalent to slightly less than two diode drop. This comes and this automatically gets biased by this current source. Therefore the Zener voltage here is going to be less than 2V gamma necessary to bias the class b in class ab mode.

Here this is the active load which is straight forward. And this is the output stage, these resistors are current sense resistors for protecting the output stage. The output stage as you see is nothing but again PNP, NPN combination and you can see the straight forward protection which is necessary for any output stage that we learnt in voltage regulator being still used here. This transistor normally is off primarily because this voltage is not good enough to bias it in the forward direction. So this is the sense resistance R sense, the moment a current which is I into R sense develops a voltage V gamma this transistor gets into the active region.

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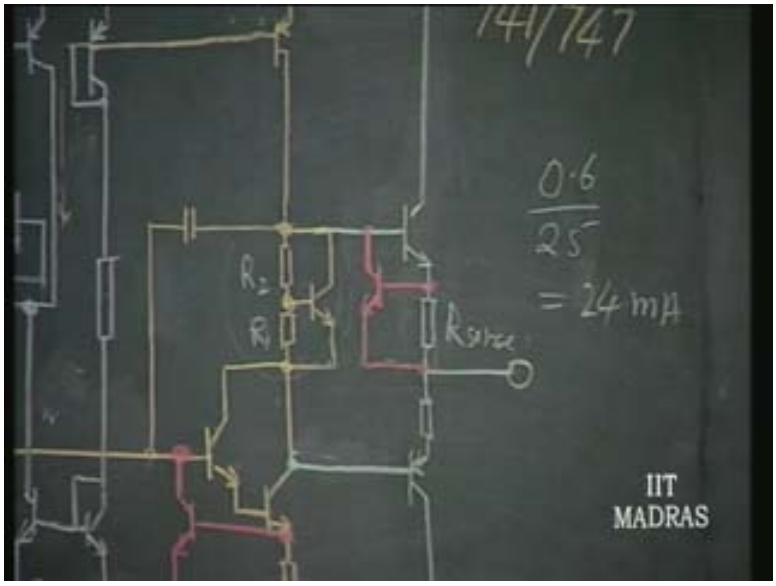

It diverts the additional drive that otherwise would have increased the output current resulting in the output transistor getting destroyed. So this prevention of additional current drive which otherwise would have increased the output current is prevented by this transistor which is already put inside so typical value of that resistance is given as 26 ohms. If you consider that then 0.6 by 25 ohms is going to be about 24 milliamperes. So it is typically of the order of 20 milliamperes that is the order of current short circuit protection current coming here in the case of 741s. That means you must never connect any load. you might just connect a resistance like 1k and expect 10V to be developed so 10V and 1k so 10 milliamperes which is safe.

But what matters normally is that suppose it is capacitive load then you are totally unaware that you are having a capacitance at the output and for the signal frequency which is pretty high the current increases beyond 24 milliamperes. You are not able to notice it because you have put a resistance which is quite tolerably high enough so that this current limit is here. But the capacitive load will keep drawing more and more current at high frequency and the waveform gets distorted now because it goes to the current mode of operation.

Hence, at a certain signal current the waveform gets distorted because of this current limitation coming into picture. This is something that you have to again notice it is similar to our slew rate limitation. So always check on all these limitations coming about because of protection circuitry etc. Now why not an exactly similar structure is put here? If I have to put exactly similar diversion scheme here I should use PNP and PNP is not an efficient structure to divert traffic because while diverting traffic the amount of current drawn from this is extremely small.

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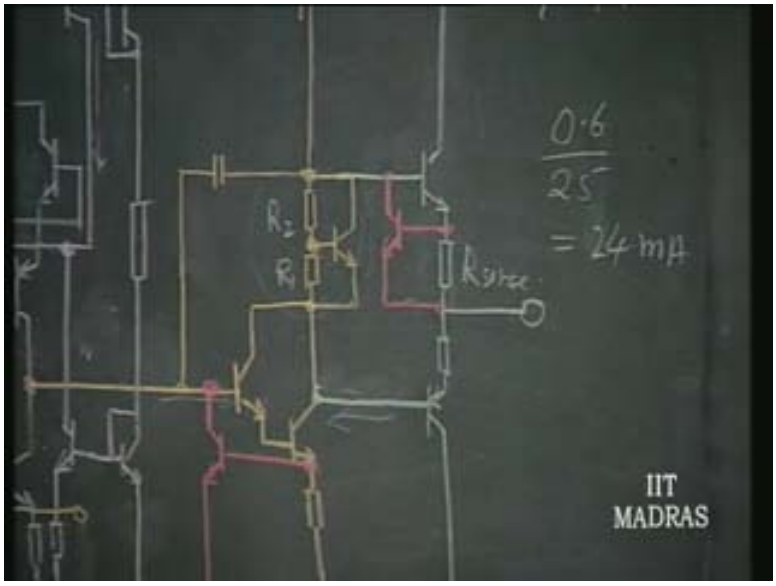

So in such a situation what we do is, for example I do not have to divert the traffic at may be near Spencer, I can start diverting the traffic near Egmore feeder lines to Central itself there is no need because I know most of the lines are coming to Central. I do not have to start diverting the traffic exactly around Central if there is traffic blockage into the Mount Road. So the same thing is adopted here, I do not have to divert the traffic for this here, I will do it, where did this traffic come from is the question now. Obviously this is coming directly from, when I drive a current into this there is going to be current in this direction. If this current exceed then this current correspondingly exceeds. It has nothing to do with these current sources. So the source of traffic here is going to be from here. So it is enough if I divert the traffic here itself. So I put a good NPN transistor and a sense resistance here and that is going to remove the current drive into this.

The moment I think that this current is going to exceed a certain limit. This current is going to exceed a certain limit the vita of the transistor is low so this current is going to be pretty high. Therefore it is this transistor which we are now trying to protect. This current is going to be of the same order of magnitude as this current. So you are trying to protect this so imagine that you are trying to protect this and there by protect this also.

Now you might say why did we put this resistance here?
It is for the AC when it is not coming into the picture still it should act as somewhat a symmetric structure so this resistance has been put there. So this kind of current is the short circuit current protection scheme is adopted in most of these op amps. The values are different and we are not sure because now this is beta dependent so this value is different from this. As long as it is offering some short circuit protection, it is protecting the output transistor. The rating for this transistor is totally different from this transistor. The current capability of this transistor and this are different and that is why all these values are different. After a lot of test and finding out possible variations of vita over the widest range of temperatures etc the designer has put the suitable values here. The gain of

the stage is obviously getting affected here. But because a resistance is put here the impedance level has gone up here.

Actually the gain is not going to get much affected because of this kind of scheme. The impedance level here has gone up that means the gain of this stage has gone up by some amount. This is a low valued resistance here about 50 ohms and this resistance is of the order of hundreds of kilo ohms. So the gain of this stage itself is now hundreds of kilo ohms by 50 Ohms plus Re of this transistor. If transistor is operating at 1 milliampere current then it is 25 so it is 75 ohms. So the gain of this stage is straight away hundreds of kilo ohms by 75 ohms so it is more than about 10 power 3 to 10 power 4. So 10 power 3 to 10 power 4 gain is got by this itself. Then a gain of about 50 to 100 is got by this particular stage. So, overall gain is about 10 power 5 to 10 power 6. That is the kind of gain you have for this stage.

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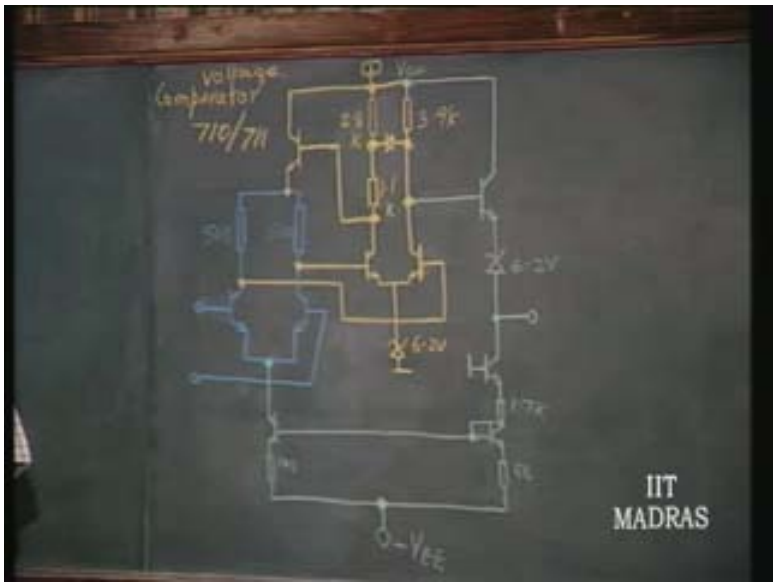

Now that we know how the practical op amps performance factors are fixed what are the internal parameters which have to be chosen properly in order to design the op amp for given specification etc.

We will discuss a variation of an op amp which is called comparator. Now, there is always a tendency to use operational amplifiers which are used for negative feedback application as comparators. Obviously this is not a good practice because when the application is comparison of voltages and there is not likely to be negative feedback we have already understood that there is no problem of frequency instability arising. Therefore there is no need to compensate and if we do not compensate we have the widest possible bandwidth of usage.

So a good sense always is; if the application is for comparison of voltages then we must not use internally compensated op amps at all. You must go either for externally

compensated op amps and we do not put the compensating capacitor or we must go in for comparators which have been designed with the application of comparison in mind. Network-wise obviously both are high gain amplifiers. But there is a lot of difference in the actual design of a comparator as well as operational amplifier. That is why we want to highlight difference in design between comparators and op amps.

What is a comparator?
Again a comparator is a high gain amplifier because in order to compare one voltage with reference voltage accurately the difference in voltages that is necessary to change the state from high to low should be as small as possible. This is achieved only by making the gain equal to infinity. That means a good comparator is automatically a good high gain amplifier or op amp. But we are interested in its large signal properties because it is primarily used either at its low level at its high level. It is intended for use as an interface circuit between may be analog world and digital world where the digital world is facing only two levels high and low.

Therefore the comparator has to be designed specifically catering to the digital world as the output and analog world as the input. So in such a situation we have to bare in mind these different worlds which this comparator is seeing. First of all the output level need not be plus V_s and minus V_s. It needs to be compatible with the logic family to which it is going to be connected.

Let us say it is ttl, then it should be 5V and 0V. When this comparator 710 and 711 became popular ttl circuits were in great use in almost all digital designs. Therefore this was designed with output level becoming totally compatible with that of ttl logic family as far as the output is concerned. The input is still the differential amplifier stage like in the case of conventional op amp. But once again its responsibility is different, it is comparing two voltages and even though the output is going to be in high state or low state it has to go from high to low or low to high and this has to occur at the highest possible speed of operation.

Now we are not bothered about slew rate etc for this. Slew rate is the characteristic of the structure when the output is following input to a certain extent and the distortion starts because now output can no longer rise at that rate whereas here we are not bothered about output input relationship. We want the output to reach high as quickly as possible whether it is a linear relationship or a non linear relationship we are not bothered about that. So the speed is what is important. When we discuss the comparator property we will not talk of slew rate or gain bandwidth product etc but will rather talk of rise time and fall time.

How quickly it can rise from low to high and high to low and that has to be made as small as possible. Again the parameters that make it small will be the same parameters. These are time constants because when the structure is in the active region it is going from high to low or low to high.

Therefore the time constants have to be made low. Straight away capacitors are not to be used at all. Compensating capacitors should be avoided all together. Then resistors have to be made as low as possible. Therefore we very rarely use active load in comparators.

We use physical resistances of the order of hundreds of ohms. Now you might say the gain is going to be pretty low. The operating current is not going to be low but the operating current is going to be pretty high compared to the conventional op amp. So, the straight forward current mirror technique has been adopted to obtain currents of the order of may be milliamperes. Apart from that the resistances are low so the gain of this stage is going to be very low. That need not be a bothering issue as far as you are concerned because you can adopt positive feedback in order to boost up the gain here. No where in application of amplifiers we use positive feedback because it is highly sensitive.

The gain then becomes more sensitive to active parameters than before. But here we do not bother about sensitivity. It is not likely to stay as active mode for long but it is going to quickly go through that and during that time the gain has to be kept as high as possible. The specific value of gain is not going to matter. Therefore positive feedback is used in order to boost up the gain. What is positive feedback? If you have a gain of 100 for the stage, so 100 by 1 minus 100 into 1 by 200 so what will be the gain now? This is a by 1 minus a into beta so the amount of positive feedback is 1 by 200 which is very small.

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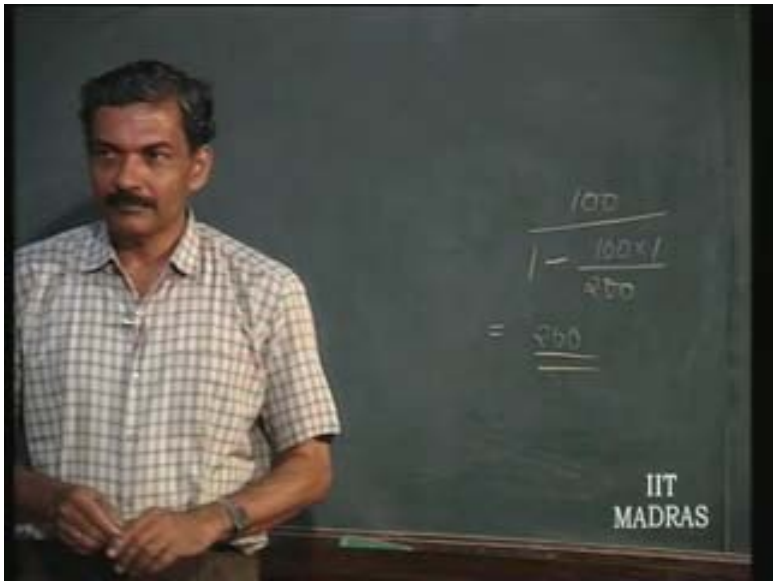

So I have been able to make gain now go to 200, double the gain by using little width of positive feedback. Now that is what is done. This is a differential output stage. This input stage is feeding on to the next stage, what is the next stage? This structure is not a differential amplifier but it is a common emitter amplifier just as in the case of other op amps.

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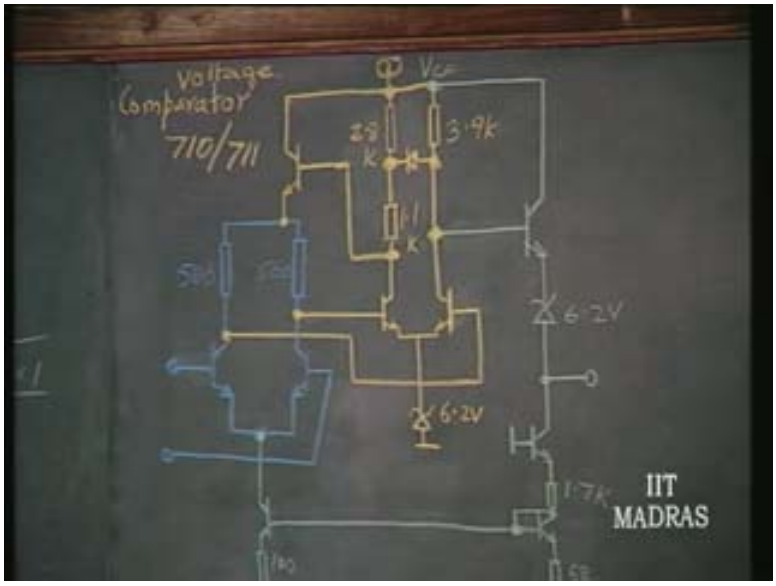

So the next stage is, even though it is drawn like this there is no current source here, this is the voltage source the level shifter. The collector potential here has to be higher than that here. The collector potential here has to be higher than that of the base so level shifting voltage of 6.2V Zener is used. But for AC purposes this is ground. Therefore these two are two independent amplifiers, one is connected to one collector and another is connected to the other collector. Therefore you are likely to lose gain by a factor of 2 because these are two independent stages.

Therefore in order to prevent from losing what is done is, this output is getting amplified here and this output is sensed here by the common collector stage here and fed to this. So what happens now is, for one of the structures there is positive feedback but for the other one there is negative because there is a phase difference of 180 degrees between these two. So, for one there is positive feedback and for the other there is negative feedback. We want positive feedback to occur for the one that is going to be fed to this stage. So you can check that for the input from here to here there is no feedback, there is no phase shift, there is a phase shift of 180 degrees here but no phase shift here and that is positive feedback for this.

Replace this structure by an equivalent circuit and prove that the gain is exactly behaving like this. If the initial gain is 100 the final gain is 100 by 1 minus 100 into 1 by 200 and it becomes twice that. This is another technique of converting differential output to singular output by giving positive feedback adopted primarily in comparator circuits where positive feedback is not going to matter.

In fact you might say that ultimately one might use the comparator with total positive feedback. That means instead of 1 by 200 we will make it 1 by 100 itself and make gain equal to infinity. Therefore now even though if the gain of the amplifier is finite I am able

to make use of positive feedback and boost up the gain to infinity. This is regenerative feedback or it becomes a smith trigger.

If you make this more than 1 by 100 then there is considerable amount of positive feedback and it can never remain in the active region. It will either go from high to low or low to high on its own without signal being necessary to push it. We know that gain is not very important in the case of comparators less primarily. Therefore we live with low gain in order to boost up the speed of operation and then give positive feedback here in order to increase the gain to the original value restored.

Now from here it is connected to common collector output stage. This is of course biased properly. And there is a level shifting arrangement here 6.2V once again. you can check this, this is 6.2V and if this transistor driven to saturation it is likely to happen, this voltage is going to be 6.2V and V gamma, this is 6.2V so this going to be very nearly the ground potential.

If this is off then this is likely to go to the up to V_{cc} and that is prevented by what is called as clamping circuit here. this diode is not going to conduct if this is going to be in active region because these are identical stages 1.18 plus 2.8 is 3.9 so the voltage between this and this is going to be 0.

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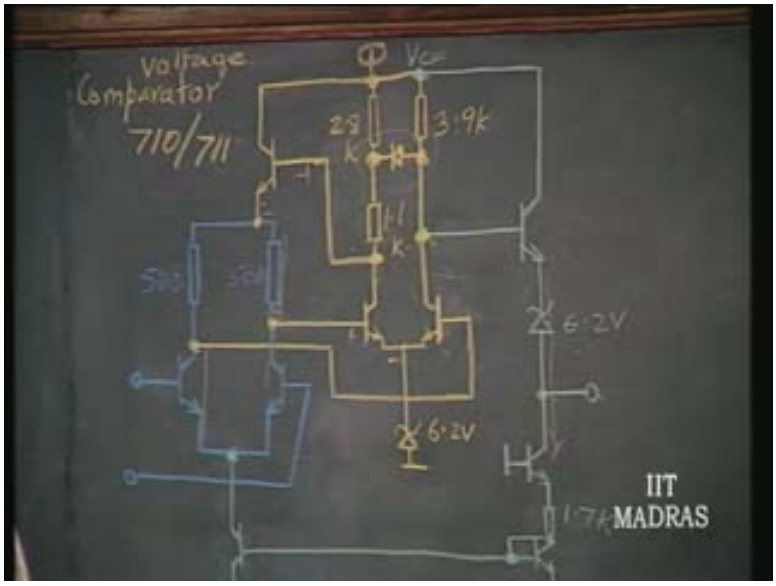

Therefore this going to be reverse biased most of the time when it is in the active region so this diode is not in picture. but the moment this goes off and this is pulled up to V_{cc} this potential is rising very fast up to V_{cc} and it is clamped down up to a certain DC potential which is less than V_{cc} so that the output potential is in a range within the high range. It should be less than 5V greater than may be 2.5V so anywhere between 2.5 to 5V. That is for all the supply voltage ranges it should lay within this range of 2.5 to 5V.

So this clamping structure is for that purpose. The output level obviously depends upon supply voltage you are using.

Therefore you can find out the high state as well as the low state and that simply goes by saying that by this transistor is either in saturation or in cutoff mode. Analyze the whole thing and find out the total gain of this stage, gain is coming because of two effects. One is, it is 500 by $2R_E$ into 2 because of the positive feedback therefore it is 500 by R_E into 3.9k by R_E of this step. How do you find the operating current of this?

You can find the operating current of this and of this structure and all these things. And this potential is going to be the same as this potential and you know this potential here, this is 6.2, this is 0.6 you know the drop here, this is 0.6 so you know the potential here so you know the operating current here, so you have to come in an indirect fashion here to find out the operating current of this. These are common emitter amplifiers so the operating current is fixed because of this potential getting fixed here. So this current is known and therefore this current should be as same as this current so you know the gain of this stage which is 3.9k by R_E of this transistor. The overall gain is that gain into this gain. This comparator is one of the most popular comparators which is good for most of the high speed interface applications that is in d to a converters and function generators and for all such circuits you can use this comparator very well.

But what will be the danger of negative feedback here?
It will start oscillating. You can see that here also. Even without negative feedback if your power supply itself is not bypassed properly you see that apart from high and low you will have a thick line on the top and bottom here because it is still used in open loop and it has all the poles coming into picture and the feedback is coming through the power supply. Therefore, whenever you use comparators in a practical circuit and also in an open loop you have to be extremely careful about power supply lines also. So this cannot be used in negative feedback. This can be used in positive feedback mode without any problem but not in negative feedback mode, none of the comparators can be used in negative feedback mode. If you have to use then you have to put a compensating capacitor between this and this.

There are two separate feedback pass here, there is an internal feedback here and here so it might cause problems. Most of the times the internal feedback itself is sufficient because this collector base capacitor is there, additionally we putting some capacitor to make it dominant so as to make it work for every gain that you are thinking of. But when it is under open loop if it oscillates the amount of capacitor you have to put may be extremely small. Or it is not oscillating because this capacitor is already coming as dominant pole because that is the Miller effect capacitor. So do not assume that there is no dominant pole here. That may be quite dominant enough under this open loop situation even if there is small amount of negative feedback not to cause any oscillation here.

Here for this state the input impedance this is 500 Ohms. If it is operated at 1 milliampere current or so it is about 25 Ohms into beta 200 so about 5 kilo ohms. It is not loading it at all. This input impedance is of the order of 5 kilo ohms or so and it is 500 Ohms here.