Analog ICs
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IC Operational Voltage Amplifier
Lecture - 15

In last class we saw how we can synthesize the basic structure required for an operational voltage amplifier starting from the fundamentals. Ideal voltage control voltage source g matrix is defined with these elements being 0 and only the forward transfer parameter being finite.

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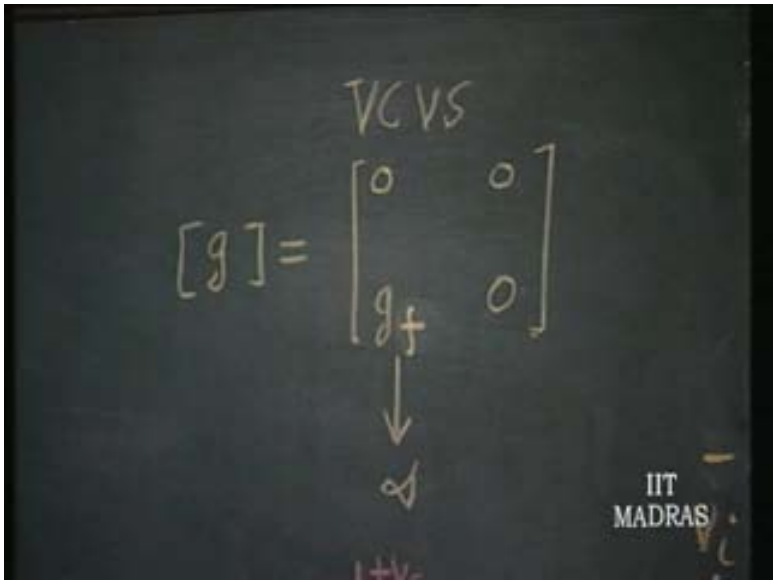

And this finite forward transfer parameter in the case of operational amplifier will become very high or go towards infinity. So this is the standard procedure for synthesis of any of these control sources whether it is starting from Voltage Controlled Voltage Source or Current Controlled Current Source or Current Controlled Voltage Source or Voltage Controlled Current Source.

One must start with the corresponding idealized matrix and make the corresponding forward transfer parameter go towards a very high value or go towards infinity. Then that particular control source becomes that particular type of operational amplifier. It could become operational voltage amplifier or operational current amplifier or operational transconductance amplifier or operational transresistance type of amplifier. These are the only four types of operational amplifiers that can exist. So today we will see a specific structure which we have assembled. We said for taking care of the input impedance input impedance should go towards infinity or input conductance should go towards zero. And that is done by proper selection of input stage and its biasing current.

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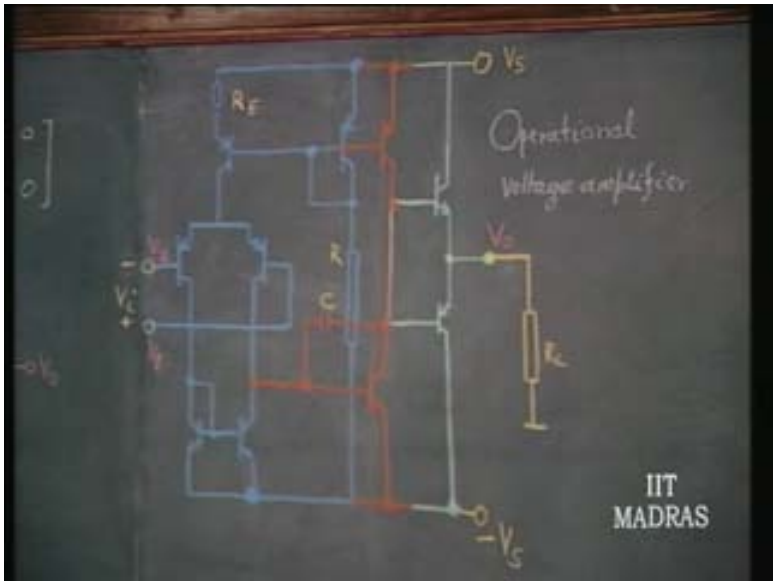

Then the output resistance should go to 0 output impedance should go towards 0 and that is taken care of by selecting the proper stage for output that is common collector stage. And the very purpose of operational amplifier for operational purpose requires the forward parameter to go to a very high value which is done by the intermediate stage.
We could have obviously improved this gf further and decreased this further by cascading more stages. But that will complicate the stage in terms of causing the stage to have more number of time constants which will determine the open loop transfer parameter then result in frequency instability problems when used under the negative feedback situations and that is why we have chosen the number of stages to be three.

Now let us consider the input stage. We already have obtained this structure for a differential amplifier without using any resistors. So these differentials pair in this particular case we have chosen it to be a PNP transistor assuming that in a given technology we have good PNP transistors available and we would select that. So, as to make the load, load is now going to be decided by the NPN transistor which is a current bearer. So this is the active load which is going to be the NPN current bearer.

If we had chosen NPN inputs pair then in turn you would have to go for PNP current sources or current mirror for the active load. So this is one way we have chosen primarily because the next stage is important in giving gain and the next stage has to be necessarily NPN and the next stage is going to be NPN and it is going to have emitter connected to ground AC wise. That means emitter should be connected to minus V_s and the potential here is going to be one diode above minus. Therefore we have naturally this acting as a suitable load without the need for any level shifting stage.

You now understand why this configuration has been chosen?
That is, the intermediate stage has got to be the high gain stage. The good NPN transistor will necessarily have high gain and good speed of operation, high frequency. So this

particular thing is going to have very high gain. That means it is a common emitter stage here, emitter is AC wise grounded that means it is connected to the most negative potential for biasing purposes and then from here we have one diode dropped higher. If you select the NPN active load there will not be any need for level shifting which otherwise would have been. So this is the neat way of getting rid of the level shifting situation. But of course we have to worry about getting good PNP as the input pair. We will see how it can be achieved in practice where NPN is given dominance and PNP transistors have poor beta. In such situations you might have to see how to modify this further. In a situation where both good PNP and good NPN transistors are available this synthesis can be straight away adopted.

The final stage the output stage is nothing but the common collector, positive going signal being taken care of by the NPN and the negative going signal being taken care of by PNP structure. Once again in order that the performance of this composite structure should be good we have to map NPN and PNP equally good. Once again we have to see how in a given situation where no good PNP is available how to modify this structure so as to make it almost as good as the original NPN. But once again we can say that when we have a technology where both NPN, PNP are available we can straight away adopt this simple structure as the basic structure for an operational amplifier. So this kind of topology selection can be done even when we are told that the op amp to be designed should come out of a MOSFET structure or it should be a BiMOS structure. We can then think of appropriate stages using appropriate transistors.

For example, if you are asked to design this stage using BiMOS structures then naturally input stage could be straight away MOS because we can make this go towards 0 straight. The input stage can be straight away a MOS structure. We know how to do a differential structure with this kind of active load using MOS. Then the second structure will be retained as bipolar because gm of a given bipolar for any operating current is going to be one order of magnitude definitely higher than that of the corresponding factor so this is going to be bipolar common emitter.

Next one is a good output stage with automatic short circuit protection could be a CMOS inverter itself. It will give you gain and it can also act as a decent output stage giving you almost the full swing possible. And it is automatically short circuit protected because it is actually operating in the current saturation mode. Therefore this is how we can come up with a sort of BiMOS op amp.

Input MOSFET stage, intermediate bipolar stage and output could be a CMOS inverter. All of these stages in fact have the same power ability. They are not basic stages. But one way to increase the power handling the ability of these transistors is to merely change the geometry of the device. If you make identical geometry devices they will all have equal power dissipation ability. So basically these are not power op amps we can even design power op amps if we make the output stage truly a power stage. Here output stage is merely used as a low output impedance source. Now let us see some of the components coming here. Here this comes into picture for frequency compensation. This capacitor is internally compensated op amps otherwise these two terminals are brought out in

externally compensated op amps where in the user has to put suitable capacitor for his use.

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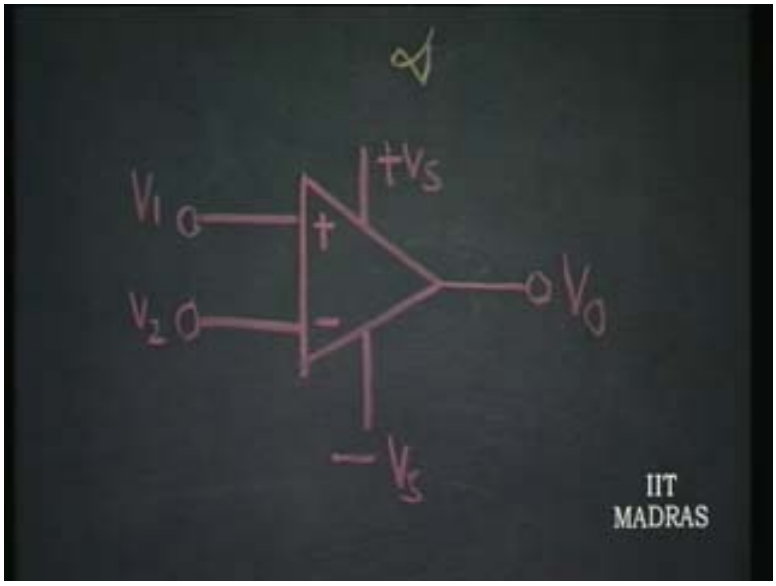

The load resistance can be connected externally. Now the symbol for this op amp would be differential input dual power supplies and the output all of these with reference to a common ground. So output is available with reference to a common ground. we have op amps available with, if V_0 is a times lesser if a is the open loop gain or that is actually gf so a times V_1 minus V_2 you have what are called as dual output op amps differential input differential output op amps where you can also get minus a times V_1 minus V_2. In a differential structure that is already available. One is; a times V_1 minus V_2 and the other one is; minus a times V_1 minus V_2. So in a suitable application you can make it differential output differential input. These are all the variations available to you.

Now, obviously you can notice this mode of biasing. This is a current mirror for obtaining low value current. Here this is obtaining a current which is $V_t \log I_1$ by I_2 by R_E is equal to I_2. If I_1 is the current in this and I_2 is the current in this we know that I_2 is going to be $V_t \log I_1$ by I_2 by R_E. So, given a circuit you can quickly arrive at the value of the operating current here because you know the value of R_e, in fact this equation has to be solved so you can assume a value for I_2 and get the value for I_2, iteratively you solve this ultimately you will approach the correct value of I_2.

So, given a supply here plus V_s and minus V_s the biasing current I_1 is going to be $2V_s$ minus V_{gamma} by r. The main biasing current taken as reference is going to be $2V_s$ minus V_{gamma} by r. Using this equation you can solve for I_2 and get the value of I_2. In a typical situation this will be of order of tens of kilo ohms and this current is going to be of the order of milliampere and this current is going to be of the order of few micro amperes. And typically therefore the input resistance of this is going to be beta plus 1 times $2R_E$ is

going to be of the order of mega ohm or so mainly because you are operating at current of the order of micro amperes.

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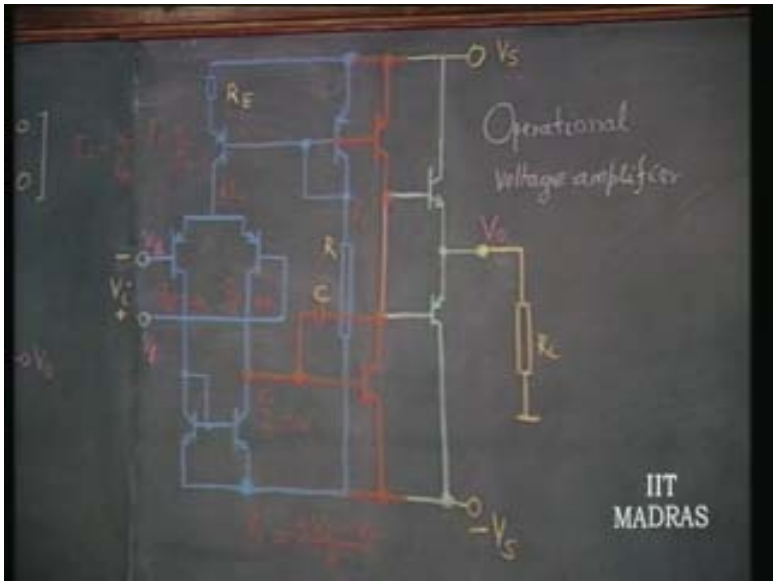

The R_e is equal to V_t by i_2 by 2 so you can evaluate the input impedance of this stage. It has been made under the open loop to be the order of mega ohms typically.

Gain: When V_i is supplied here V_i by $2R_E$ is the change in current superimposed over and above. This is going to be I_2 by 2 and this is going to be I_2 by 2 and we will have this current if it is increasing by some amount this will decrease by the same amount. So, if we have this as plus delta i this will be minus delta i and we will have this as I_2 by 2 minus delta i and we see here that we have a current of 2 delta i being formed here. Under this situation all these things are behaving like ideal current sources or sinks.

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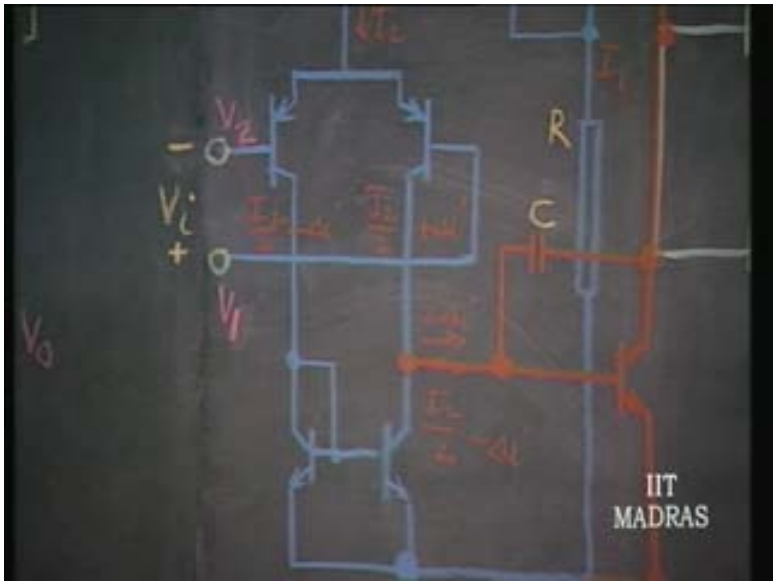

Obviously what it simply means is that this stage is taking away the entire signal current. That is not the case. Actually speaking what happens is there will be finite impedance, finite impedance here due to this and the input impedance which is going to effectively act as the load and the voltage will be doubled. Here it is shown as though it is 2 delta i times the input impedance of the next stage. That is primarily because we have ignored the output impedance of these current sources and sinks. And here this is the base current. So, under the situation that most of the current is going into this the current that is coming here is going to be beta times that current only and if you ignore the capacitor and that has to develop an output voltage here.

Once again the load here in the absence of R_l, if R_l is infinity it is going to be determined by primarily the output impedance of this current source. If you put an R_l here then you have to consider the effect of R_l here which is nothing but beta plus 1 times R_l appearing shunting this output impedance. Now at every point you see the need for knowing clearly what the impedance levels are. This impedance has to be pretty high so that the gain which is nothing but beta times 2 delta i into whatever impedance is seen there which is nothing but beta plus 1 times R_l shunted by the output impedance of this is made as large as possible.

Now, what is the operating current of this and how do you find the gain of this stage? If you are told that these are not given in terms of currents but I give the impedance levels here, impedance levels here and you can find out impedance levels here because the operating current of this is known. If this is $2V_s$ minus V_{gamma} by r if this is the current bearer the same current will flow through this so you know the R_E of this. And the gain of this is going to be nothing but the impedance at the collector by R_E of this. So obviously this is going to operate at higher current than any of these, R_E has to be made low. But when you make R_E low you have to be aware of the fact that it is going to load this also

and the impedance level comes down. So naturally we have to see that the impedance level here does not come down so we have increase the beta.

One way to increase the beta is to use a Darlington pair. These are all the modifications that might have to be adopted here. Here again we can increase the impedance level by putting emitter degeneration resistors or using Wilson current mirrors. So we can improve the gain of this whole thing by adopting proper techniques. But given a situation, we are able to obtain the open loop gain of this stage now.

What is the open loop gain of this particular stage?
It is 2 delta i into beta into the effective collector resistance at this point that is the DC open loop gain. So, I know the input impedance, I know the parameter 1 by that input resistance. I know the open loop gain that means I know gf. Now how do I evaluate the output impedance? This is not very easy because you are saying this is going to be class b where the operating current is 0. So you have to assume some class ab biasing. Ultimately we will see that this is not class b at all and it is made class ab so there is going to be some amount of current in this so that you can evaluate the value of Re at that particular point.

Most of the time the output impedance is going to be governed by this plus this divided by beta. The impedance level here being high the output impedance of this is rather governed by mostly this divided by beta plus 1.

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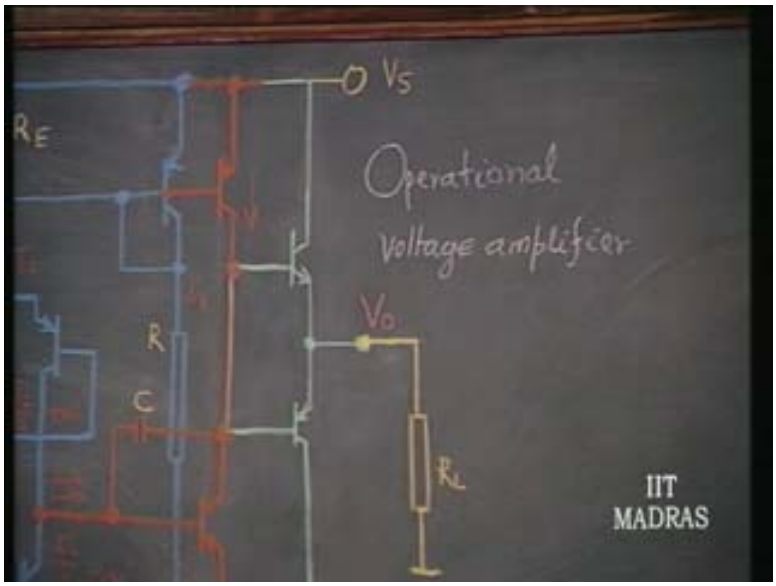

Apart from that you also have to take into account, if you are likely to put, this is an output stage therefore it will require short circuit protection automatically. And again the same scheme of current sensing resistors have to be put here in order to divert the diode. Let us see the protection scheme later but it is exactly similar to what we have discussed

for the voltage regulator. So there will be series resistances coming in series with these emitters and they will naturally come as additional output resistances.

What about the common mode swing as far as this is concerned?
We have now evaluated all these parameters. This is for all practical purposes 0. So we know the way to evaluate the actual g parameters of a given operational amplifier given the configuration.

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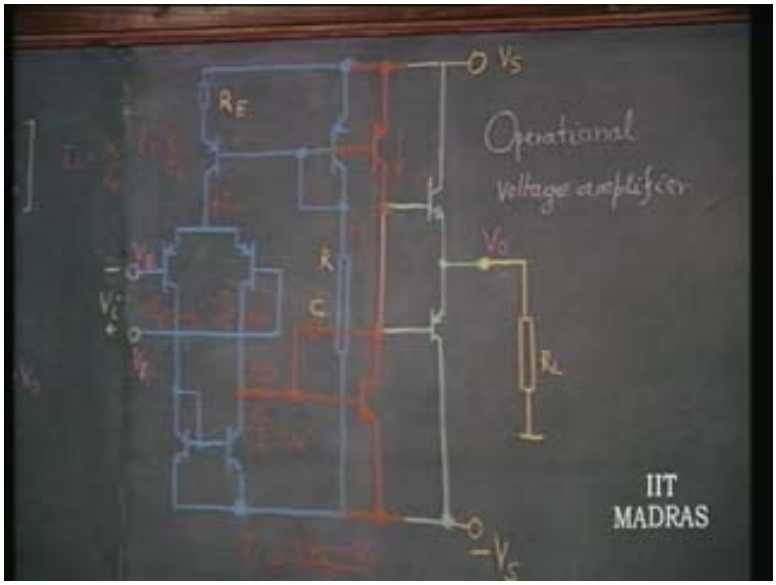

Now let us see something about large signal effect. As far as the common mode signal is concerned we are going to connect this together. And then the common mode voltage can gain vary as much as one diode drop here, this can come up to this no problem and there is one more diode here. So two diode drop less than Vs that is the maximum limit of common mode voltage. Here as far as minimum is concerned swings one diode drop higher than minus Vs. So you can straight away see that it has the maximum common mode signal swing desired so as to prevent any problem when you use it again in negative feedback situation.

Therefore this stage has been well chosen and that is why very few changes have taken place over the years as to the topology of the configuration that is going to act as input stage. Then as far as the output is concerned the output can swing that means two diode drops less than Vs and one diode drop collector and two diode drops higher than minus Vs which is in conformity with what is happening for the common mode voltage almost at the input. Now this is as much for the large signal effect. Now let us discuss about the operational amplifier with two important parameters associated with op amp.

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One is bandwidth the need for frequency compensation and the second one is slew rate which is the large signal parameter. So let us see what is the need for frequency compensation? Most of these op amps are likely to be used in a negative feedback situation.

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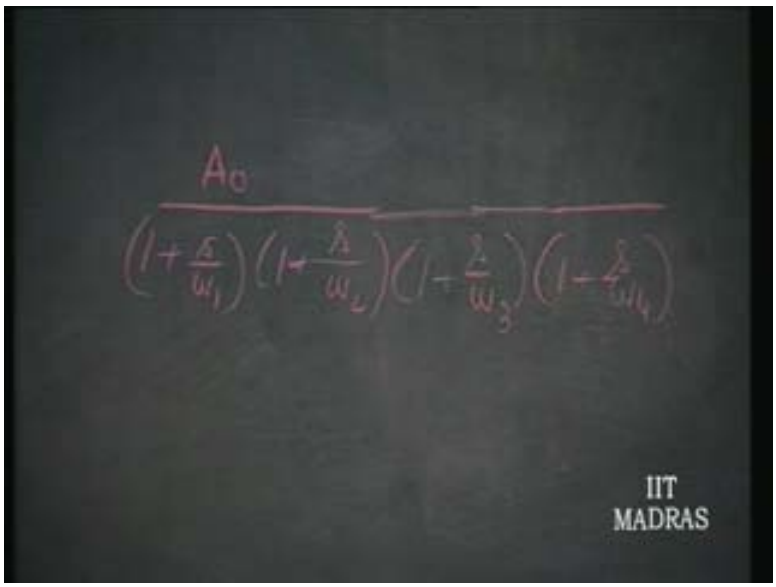

In this particular case it is a voltage amplifier and therefore its open loop gain is going to be A_0 divided by, and as there are three stages there is likely to be four time constants so 1 plus s by omega 1, 1 plus s by omega 2, 1 plus s by omega 3. If this is the first corner frequency, this is the second one, this is the third one and this is the farthest one. In

practice, for a general purpose op amp like 741 or 747 the first of corner frequency occurs at about 1 MHz, f_1 is going to be around 1MHz.

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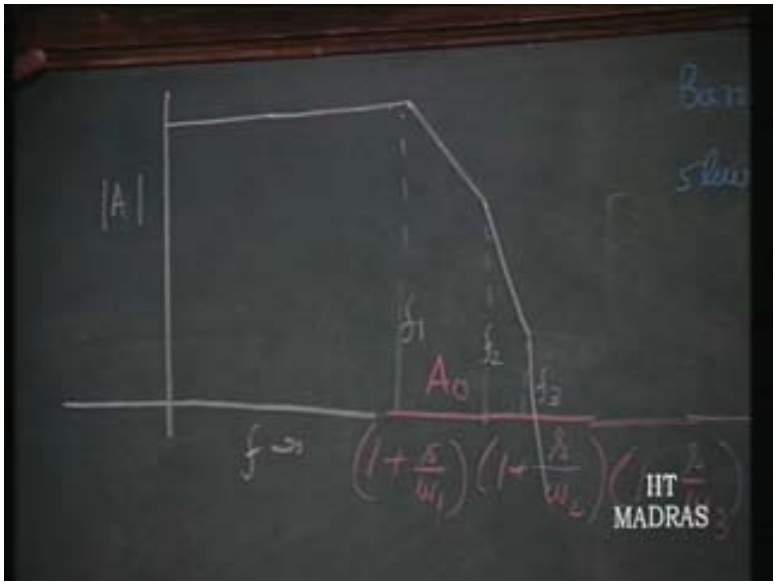

What it means is that, if you plot the gain this is going to be almost flat up to 1 MHz then it will start falling at 6 Db per octave or 20 decibels per decay and then it will start and this is going to be f_1 and this going to be f_2 this is going to be f_3 and may be by the time f_4 comes to the picture where the gain has become less than 1. So, in the useful range where the gain is greater that 1 that seems only this f_1, f_2 and f_3 come into picture. It is the magnitude of A versus frequency.

Strictly speaking you have a possible gain of something like 10 power 5 to 10 power 6 is the typical order of open loop gain for most of these common operational amplifiers bipolar. So 10 power 5 to 10 power 6 and a bandwidth of about 1 MHz, strictly speaking you should have a gain band with product of 10 power 6 MHz, it is 10 power 5 to 10 power 6 MHz. But you are not able to use this bandwidth because there is a cluster of these poles influencing the phase shift over the frequency range. That means even when the gain is high greater than 1 this has already come into picture and causes the gain to have a phase variation with respect to frequency. So, obviously somewhere in between, now what is the phase shift at this point only due to this and not due to other things? At the corner frequency if the other poles are not influencing it is going to be 45 degrees because j omega only 1 plus j so it is going to be 45 degrees here. By the time you go out of this assuming that is now contributing more of its phase shift and already has contributed enough totally giving a phase shift of 90 degrees.

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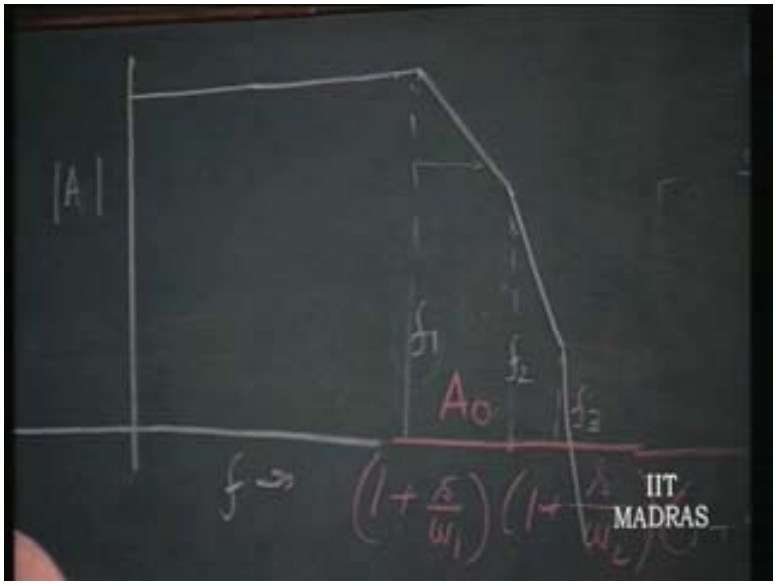

Now, when the next comes, this will contribute 45 so you have 135 here. It may be more if these are very close to one another, if they are farther away from one another this is likely to be 135. So it is 135 or more here. Obviously in a frequency range between this and this it is likely when they are staggered for a part only otherwise it can come anywhere here also. The phase shift can become equal to 180 degrees then it will start oscillating in that negative feedback situation. So, if the loop gain that is A into beta is still greater than 1 then there is a possibility of it oscillating. If A into beta, beta is the feedback factor is less than 1 when this 180 degrees phase shift occurs it is not going to oscillate.

For all values of beta if it is to work then the worst case value for beta is 1. So a general purpose op amp is designed for making this A become less than 1 when the phase shift of the entire thing becomes equal to 180 degrees. That is done artificially by shifting these poles to this side artificially cutting down the gain.

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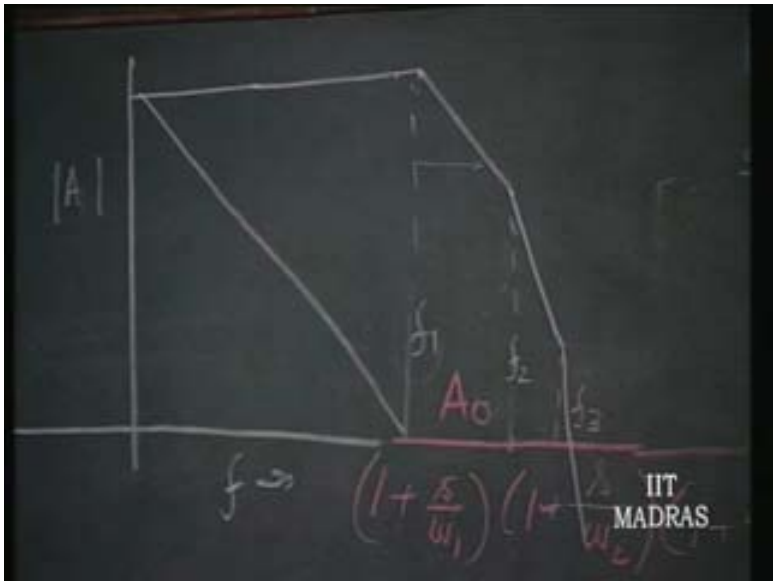

If you cut down the gain it starts falling much earlier and then by the time this first pole comes into picture the gain has been made less than 1 that is what is called as dominant pole compensation which is universally adopted for most of the internally compensated op amps. It will never give trouble to anybody using it. There is enough margin of safety so that it works even if there is a digital phase shift given by the beta, beta meaning the network itself offers some additional phase shift still it is not going to be unstable. So for this eventuality you cut down this scale. You can see that actually speaking this particular amplifier has lost most of its useful bandwidth simply in order to make everybody use it in all sorts of negative feedback configuration.

Suppose therefore you are designing your own amplifier for a specific gain then there is no need for so much of margin. That is why the manufacturers have also given the same configuration almost without the internal capacitor being connected, the provision for you to connect it so as to increase the frequency of usage of time. But however in this case they would like to put as small a capacitor as possible inside for compensation because we know that capacitor takes lot of area within the AC chip so the basic idea behind the compensation inside is always this that the capacitor should be always connected to two high impedance points if they are available because the time constants that determines the cut off frequency always depend upon the capacitor into the net resistance across the capacitor. That is the time constant which determines the reduction in gain.

Obviously you should connect it to two high impedance points. Now the two high impedance points available straight away for you inside the structure are this one and this one. Those high impedance points should have obviously the signal phase shift of 180 degrees so that the connected capacitor will result in negative feedback. So this capacitor comes into picture as what is called Miller capacitor that is another way of looking at the thing. And because you are connecting it between two high impedance points at the input will come as a huge value of capacitance. That means essentially now we can consider

that this is the time constant which determines the gain reduction. So, effectively these time constants are all going to be replaced by this particular time constant and it is enough if we discuss most of the op amp applications only using a simple model for the op amp which says A is equal to A_0 by 1 plus s by omega dominant that is called single pole role of characteristic, dominant pole which is created by the compensating capacitor.

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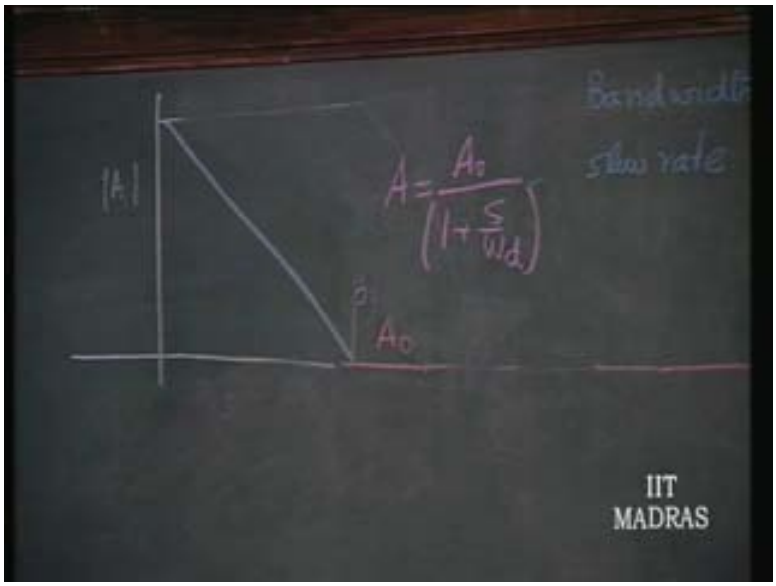

Now essentially this frequency comes pretty close to 0. Typically it is of the order of few hertz. That means in most of the application of the op amp which is much greater than hertz. You can consider that the op amp gain is A_0 by… that means the op amp itself is acting like an integrator. In its transfer function you can see it is acting like an integrator or what is this equal to? It is equal to A_0 into omega d by s called as gain into bandwidth. So this is called, A_0 into omega d is called an important parameter which is gain bandwidth product of the op amp.

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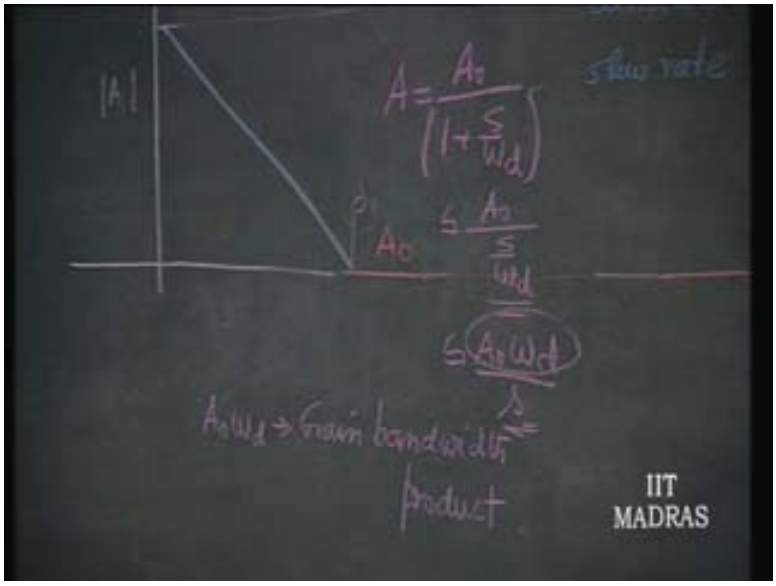

This is the measure of the quality of op amp and up to what frequency it can be used etc with what value of gain. So this is a measure of the quality of the op amp, an important parameter called the small signal parameter.

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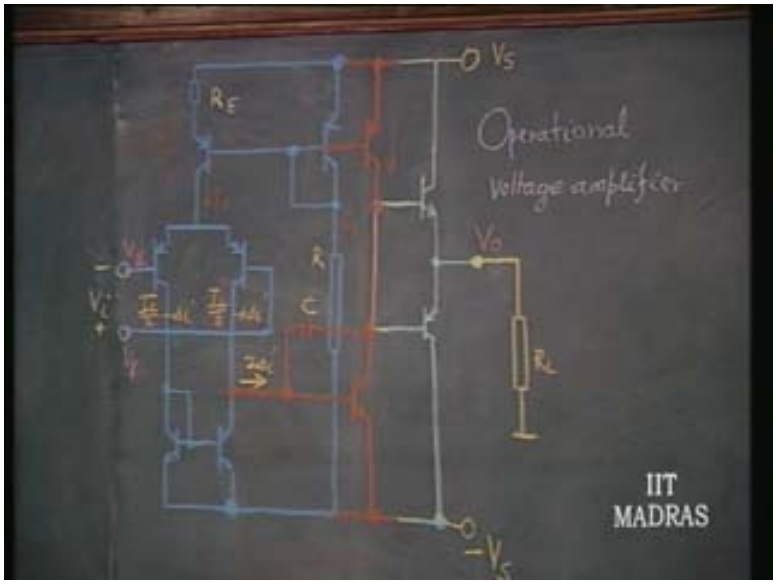

So let us now see how this can be roughly estimated from the internal structure. Let us once again come to this, this is V_2 V_1 and this is V_i so if you have V_i the current in this is going to be I_2 by 2 and I_2 by 2 and this is minus delta i and this is going to be plus delta i. And now we can see that delta i going to be 2 delta i is going to come into this. Now I can replace this whole thing only for signal picture as an amplifier op amp itself. This is

grounded and you have a situation of an amplifier with very high gain because most of the gain of an amplifier is concentrated here, neither here nor there.

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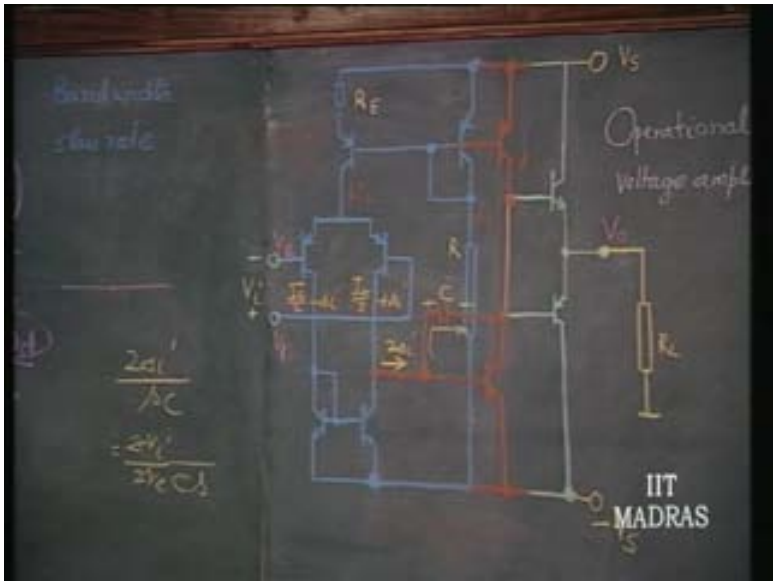

Therefore this 2 delta i is now going to flow through the capacitor because of the Miller effect anyway. So a very little current goes through this most of it goes through the capacitor and develops a potential which is 2 delta i by s sigma. With this n minus and this n plus and this potential it is already at nearly ground potential because this is a high gain stage. So, by just replacing delta i what is delta i in this particular case? The delta i is equal to V_i by 2_i into s. This is a similar approximation as in here.

If you do not make the approximation you would have got the gain as A_0 by 1 plus s by omega d. If you have considered all these impedances and then consider the Miller effect capacitor shunting it then you would have got the output as A_0 by 1 plus s by omega d. We want only the gain bandwidth product so straight away we can go for approximation and we see that gain bandwidth product of the op amp is equal t_0 r_e into 1 by that is gb is equal to 1 by r_e into c. What is Re? It is V_t by I_2 by 2.

Now the designer knows the operating current of this transistor, it is of the order of micro amperes. And c you put it of order of Pico farads and V_t is already known. If you do this you will get the gain bandwidth product.

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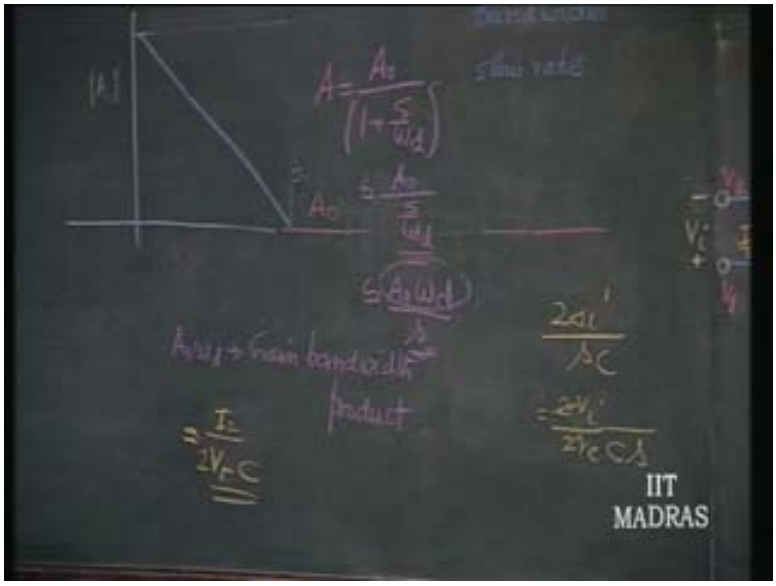

This is actually omega and you have to convert it into f so 1 by 2π you have to make. Then it will be of the order of MHz automatically. So please work out a typical situation where I_2 is the order of micro amperes and c is of the order of Pico farads, V_t is known 25 mV. This is going to give you omega so if you convert it to f you will get it as the order of 1 MHz which is typically what it is for 741 type of op amps. Now you know how you can manipulate the gain bandwidth product based on biased current and compensating capacitor.

So, given the configuration you can immediately tell about the gain bandwidth product of the op amp. This is a small signal parameter. Exactly in a similar manner we can argue something for large signal parameter. After a certain point of time you can no longer say delta i is equal to V_i by 2_i is non linear. We can no longer say that delta i depends upon V_i is non linear.

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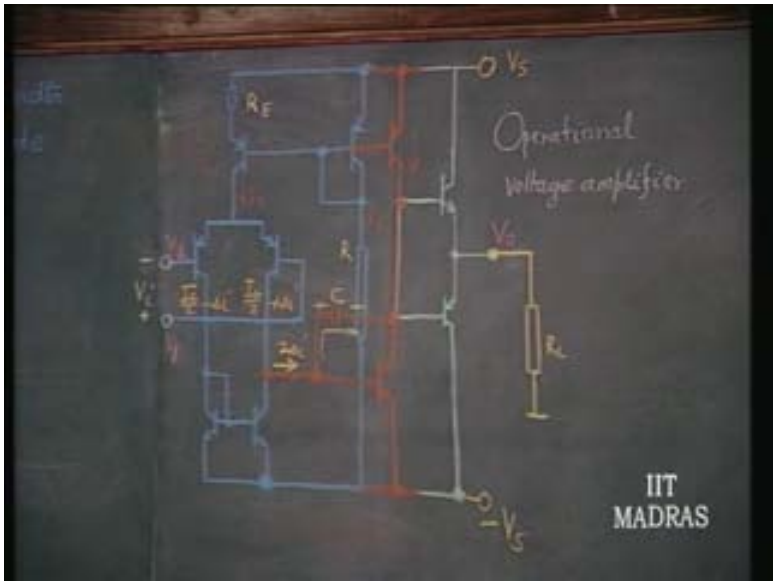

So we are going into that region where delta i is non linear only dependent on V_i. What happens as V_i increases is delta i goes closer to I_0 by 2. at that point of time when delta i becomes equal to I_2 by 2 this transistor is off, this transistor is being given the total current there after further increase in V_i is not going to change anything as far as the circuit is concerned. So this will pump a current of I_2 into this. When a DC current of I_2 is pumped into a capacitor the voltage will be I_2 by c into t. The DC current I_2 is getting pumped into the capacitor and the voltage across the capacitor is 1 by c integral I_{dt} so I_2 is a constant so it is I_2 by c into t.

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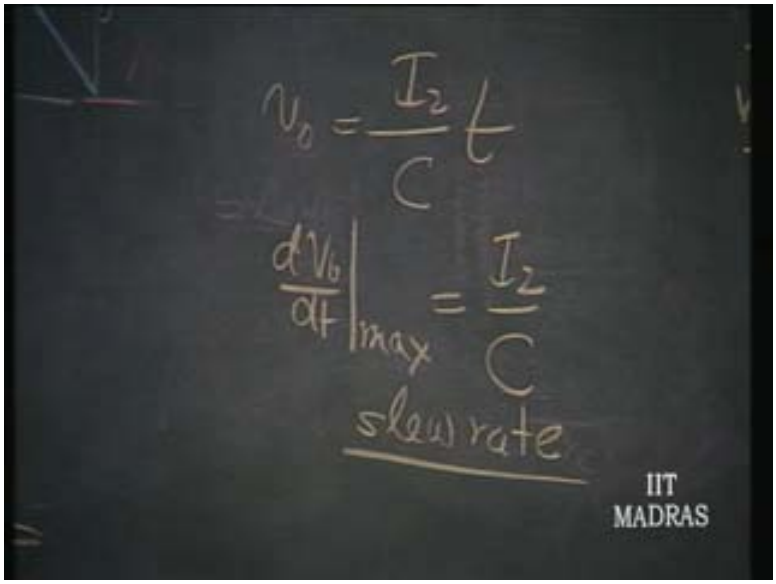

That means, after this the op amp gives up. It says, you are demanding too much from me I cannot increase at a rate higher than the rate which is I_2 by c, what is this? This is nothing but V_0, the gain of this stage is unity, so dV_0 by d_{tmax} is nothing but I_2 by c and that is defined by the manufacturer as slew rate. This is an important parameter of the op amp which every user must understand thoroughly before using it in any application.

Actually this is grossly misunderstood most of the time. This is the highest rate at which the output is capable of rising. If you demand higher rate than this of the op amp then the output will rise at slew rate. So this is not dependent upon actual value of the signal but depends upon the rate at which voltage rises. And this happens normally if it is a sine wave you are expecting at the output when 0 crossing occurs. So this distortion starts occurring not at the highest signal level but at the lowest signal level where the 0 crossing occurs where the rate is the highest for the sinusoid.

Therefore, if you are expecting a sinusoidal output at the output of the op amp and if you are demanding higher rate than the slew rate the sine wave starts getting distorted and gradually transforms itself at around zero into a triangular wave unlike other distortions which are mostly signal level dependent distortion, this is the rate dependent distortion. And you can again find out what the value of this is going to be, I_2 is of the order of micro amperes and c is of the order of Pico farads and therefore typical slew rate is of the order of volts per micro second.

It is 741 like op amps. Therefore with these properties well understood we can actually analyze any given IC and see what small signal and large signal parameters are. And also given the designing a specific IC we can attribute specific values for the various components within the IC.