Analog ICs
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Lecture - 12
Characteristics and Parameters of Voltage Regulator

In the last class we saw something about voltage regulators. We saw some important parameters like line regulation, load regulation, temperature coefficient of V_0 is something that I did not mention but however this is also equally important. Temperature coefficient of V_0 is obviously dependent upon temperature coefficient of V_{ref} and we have already made it to be equal to 0. So we are not bothered much about that factor in the design. Already the IC designer has made it very close to 0. What he wants you to do is to select the resistors properly externally so that V reference into 1 plus R_2 by R_1 will be the output voltage. Therefore R_2 and R_1 should not disturb the already present low temperature coefficient of your output voltage.

Repel rejection is something we have seen. We also understood the importance of output impedance in the last class. Therefore I am not putting it as output resistance but insisting that you should evaluate the output impedance and that should be kept very low.

In today's class we will understand something about the limitations.

What are the limiting factors in the design?
This is an important aspect. There is no pointing knowing about these parameters exactly and not knowing about the limitations. This is something that commonly happens. You have designed your circuit properly but because of your ignorance about your limitations you find that the circuit is not functioning. So limitations are very important and these have to be understood by the designer.

Let us first see the most important factors in the voltage regulator. Obviously it is designed to give a certain voltage which is independent of the input voltage variation. That is, line regulation should be good and load regulation should be good. That means even when I demand from it various ranges of current it should have output voltage remaining constant. These are the two important factors. That means the first limitations we have to consider are the limitations on V_i and limitations on I_0. So let us see how these limitations come about.

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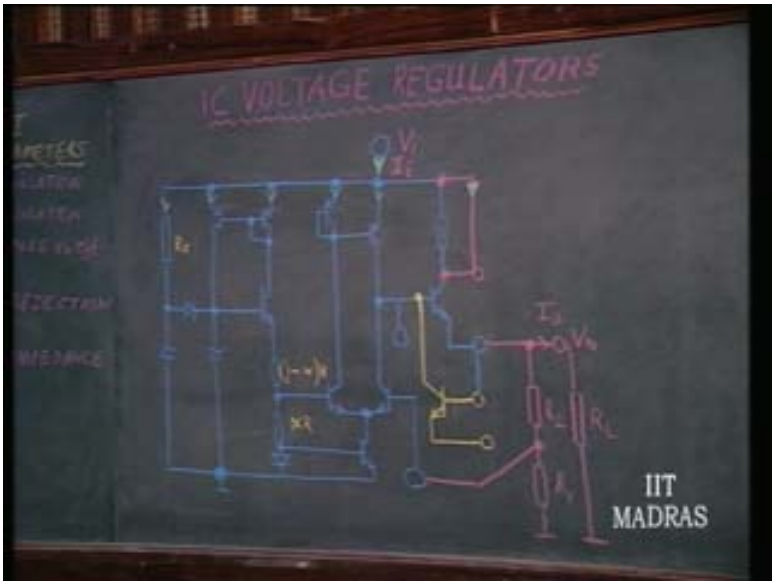

Now the question is, is there a limitation on V_0 that you can get? Actually there is another limitation which is called V_i minus V_0 limitation. Then a very important limitation on this is Pd power dissipation of the IC. So we have to understand all these limitations thoroughly. If you are going to design an IC then we have to understand how each of these limitations come about. Consequent to these particular limitations which is directly coming in terms of the important parameter associated with the voltage regulator is called efficiency.

What is efficiency?
It is nothing but output power by input power tells you how efficient you have been as a designer of this IC.

What is the idea of this [….]
Actually we do not want the regulator to be used at all. When we are designing a separate system voltage regulator is necessary.

Why does it become necessary?
It is because if we directly use this voltage our operating point will keep shifting and we have to make our design more complicated. So we would like this voltage regulator to give us a supply which is relatively independent of the input voltage. So this has been inserted in between your system and the input power. But in this process you should not spend lot of power in the IC itself. That is an inefficient way of doing it. This particular thing is going to be introduced in such a manner that in spite of introduction of this you are using the power efficiently. That means what this IC should dissipate should be very low compared to what you are using from it. That means efficiency of any regulator should be good that means it should be as close to hundred percent as possible.

So what is it that prevents you from getting it close to hundred percent efficiency?

This is something that the designer has to investigate. So that is an important parameter associated with the regulator.

Consequently what are the limitations on the efficiency?
First let us take this way because this is finally the most important thing. The voltage regulator is not doing any amplification or anything but it is being just inserted into the DC power so that the output DC power is something we get with an output voltage being constant.

Obviously we know that V_0 is going to be V_{ref} into that particular design 1 plus R_2 by R_1. This portion of the circuit is something the user has designed. If it is a 5 terminal regulator these components have to be put externally to get the required regulator output voltage. If it is a three terminal regulator even this is incorporated within the IC so you get a fixed regulated output voltage. So load is anyway something that is connected to it.

This load may be varying with time we are not sure what it is going to be because it may be not just a resistance but it is some system and subsystem connected to this. And these subsystems are in turn may be drawing power depending upon how they are acting on the signal.

So, this is a varying load. Now I am putting R_1 and R_2 to the inverting terminal in this fashion so that V_0 into R_1 by R_1 plus R_2 is what is compared with V reference which is here. So, if the loop gain is very high V reference is very nearly equal to V_0 into R_1 by R_1 plus R_2. Or, in turn, we know that V_0 is equal to V_{ref} into 1 plus R_2 by R_1. This is an important design equation.

So now the question is, given V_0 because you are going to design it for a certain V_0 and a varying value of I_0 from I_{0min} to I_{0max}, this is the design. So V_0 is given to you and I_0 is going to change from I_{0min} to I_{0max}. In such a situation we are having already limitation on V_{IN}. V_{IN} may be changing from V_{INmin} to V_{INmax}. Does this circuit works satisfactorily when V_{IN} changes from V_{INmin} to V_{INmax} when I_0 in turn changes from I_{0min} to I_{0max}?
Now when we are having V_0 as the output voltage and I_0 is the current drawn there is going to be some amount of current drawn from this also. Obviously this current is going to be made much less than this current because this is in my hand. But you should not make it too small in order to make sure that the voltage here is R_1 by R_1 plus R_2 this current should be negligibly small compared to this.

So there is a maximum limitation on R_1 plus R_2 as well as minimum value for R_1 plus R_2. So R_1 plus R_2 should not be made too low lest this current becomes comparable to this current so this current should be very small compared to the load current that is how a designer should design. This is only for sampling the output voltage. And this current should not be made too small because otherwise you cannot now assume V_0 into R_1 by R_1 plus R_2 as the voltage. That, you should let it become, because unless that becomes the voltage here we cannot then equate it to V_{ref}. That means if this current becomes comparable to this current there is a dependence on active parameters on output voltage which we do not want. So these are designed properly. If you assume then this current is

going to be predominantly the output current. So this output current is flowing through this and it is essentially flowing through this and that is going to be the dominant input current.

Input current now will comprise of this current plus various bias currents these are of the IC. So input current is normally going to be output current plus the various bias current drawn from this. And input current in a good circuit has to be very close to output current because for biasing these things you should take as low a current as possible. So essentially in a regulator we are going to have this consideration. So I_i is going to be I_0 plus various bias currents required and this has to be made very small so that this is very nearly equal to I_0.

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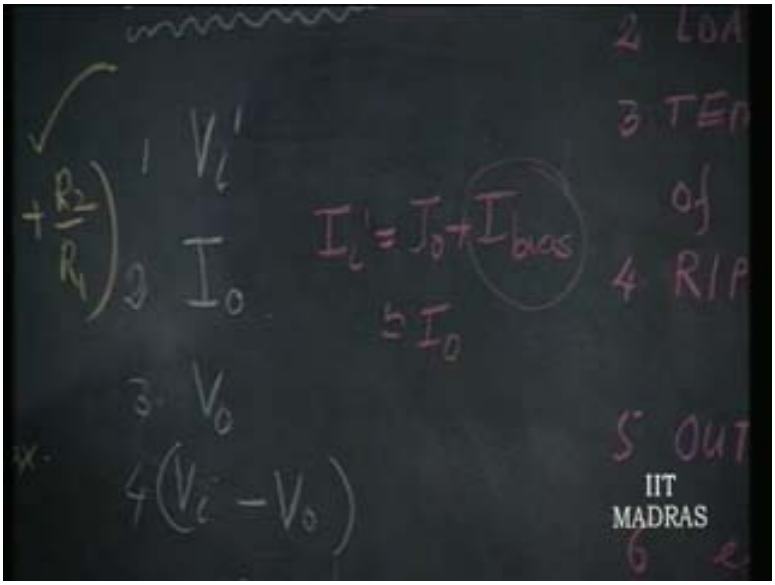

What is the efficiency under that situation?
Efficiency is given as V_0 into I_0 by V_i into I_i and we have just now said I_i is normally very close to I_0. Particularly we are discussing efficiency when it is delivering lot of power. But here it means when it is for a fixed voltage you are designing it means it is delivering maximum current.

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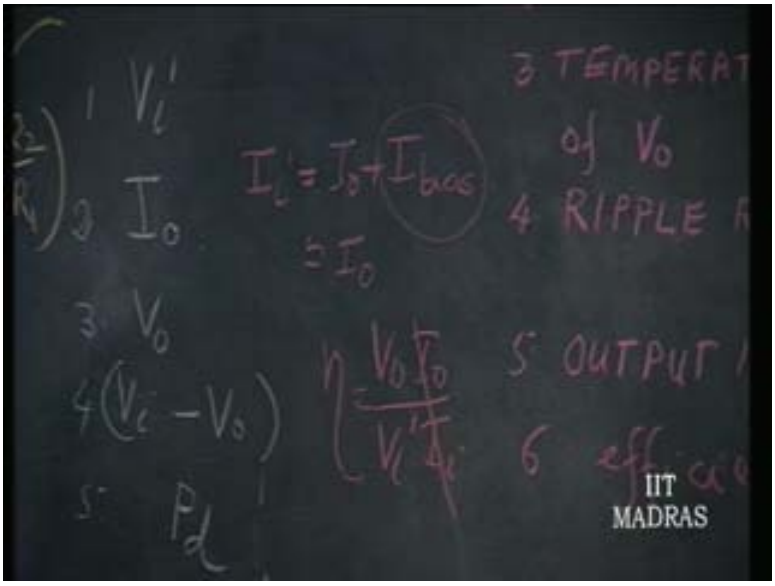

Under that situation obviously I_0 is very close to I_i. Therefore efficiency is in a good regulator, ratio of output voltage to input voltage. So what does it mean?
This is nothing but V_0 by V_0 plus V_i minus V_0. What is important is that V_i minus V_0 should be made very small in a good design. This is what is called differential voltage. This differential voltage is important in the case of voltage regulators and it is given as V_i minus V_0 differential that there is a minimum. You cannot make it lower than a certain value.

So what is that limitation?
That limitation on V_i minus V_0 minimum, this has to be made very low that we understood, can it be made as small as we please? It cannot be made small. Given a circuit we can find out what that minimum is going to be. This is V_0, we come through this and come to the circuit here we have here one V_{gamma} then we come to this, this is connected to this and this potential can swing and come close to this another limitation so this can be 0. So if this can be 0 there is one more V_{gamma} so you have two V_{gamma}. Whatever you do, it cannot be made less than two V_{gamma} for this circuit.

Now if you put a Darlington pair here it will become three V_{gamma}. In order to increase the power capability of the transistor IC the regulator you put more and more of this pyramid like structure accordingly the V_0 minus V_i differential will increase.
So, for example, in the case of 3085 how many such transistors are there?
You can quickly look at the circuit or 723 you can quickly look at the circuit and for yourself find out what will be the V_0 minus V_{imin} that can be had in a given circuit. So, in the collector to base voltage the limitation is that it can be made as small as 0V and given that the rest of it is due to the V gammas. In this circuit it is two V_{gamma} so, that is one limitation. That is coming because we want to make the efficiency as close to 1 as possible. In the process we are having this problem of not being able to make it less than a circuit.

Now is there a maximum?
Yes, what happens is……., let us consider the power dissipated in the IC.

What is the power dissipated in the IC?
It is V_iI_i minus V_0I_0 and we said this is very close to V_i minus V_0 into I_0. When power dissipated in the IC is maximum when it will be become maximum is, here I_0 is maximum and V_i minus V_0 is maximum that means P_{dmax} occurs in one case when V_i minus V_0 is maximum and I_0 is maximum.

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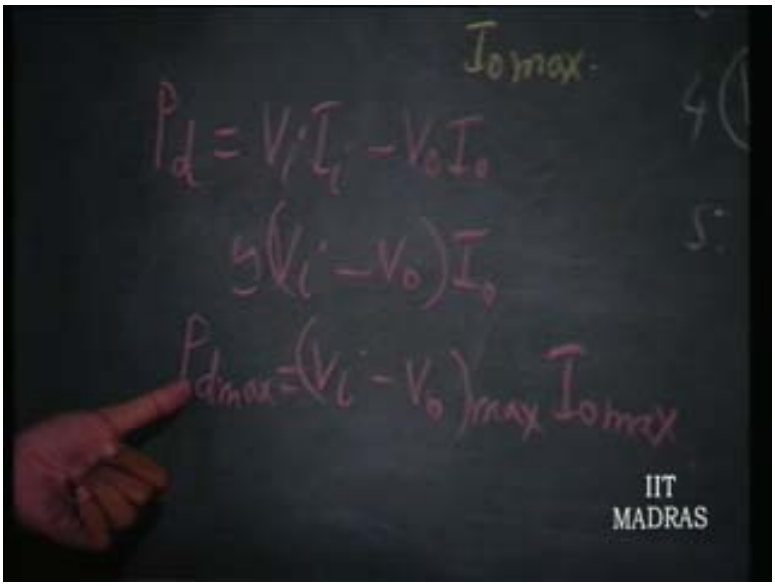

So given P_{dmax} for the IC the manufacturer will tell you that this IC is capable of dissipating only this much power. Then given P_{dmax} and knowing I_{0max} you are able to find out V_i minus V_{0max} that you can have. If V_0 is already fixed as equal to V_{ref} into 1 plus R_2 by R_1 then this will give you a limitation on V_{imax}. One limitation on V_{imax} is going through this procedure of power dissipation. This does not mean that this is going to be the final thing. So one limitation on V_{imax} can be obtained from P_{dmax} and that comes finally because of V_i minus V_{0max}. Now, if both V_i and V_0 are made variable in the sense, V_i is varying anyway from V_{imin} to V_{imax} but V_0 is what I want to keep varying because it is a varying regulated power supply I want to do. In that situation obviously you have to consider here V_{imax} minus V_{0min} into I_{0max}. And that should be the V_{imax} to which your circuit should be limited.

Now, is there any other problem connected with this. Is I_0 minimum causing any problem? Should there be a minimum or will it stop working if I do not connect or draw any load?
These are the things which you have to answer. Anyway there is a bleeder resistance here. In any case this current is going to be drawn from the circuit. And as long as it is being drawn if this circuit is still functional there is no problem. So I_0 has a limitation on this that I_{0max} is something that can come about from P_{dmax} also if it is not given. And you

know the variation of V_i from V_{imin} to V_{imax} then you can get a limitation on I0 max from the circuit that is based on power dissipation. There are a variety of things here. You should understand the circuit thoroughly when you are a designer.

If this is I_0 and this is some I_R current going here this current is going to be I_0 plus I_R and this current is going to be I_0 plus I_R by beta plus 1. You put it as beta plus 1 because in order to improve the power dissipation capability of the transistor you might put this Darlington pair of transistors so betas need not be very high for those. So, if you are putting Darlington pair do not take effective beta as beta 1 beta power 2 or beta power 3 or something, it will be beta 1 into beta 2 into beta 3. So this is the base current that is given. Therefore you have this particular thing that this current is going into this and this is a current source current going.

Now there is a constant current drawn from this I_0. How does this work? This current is going to be either decreasing or increase. Now this will be I_0 by 2 minus delta I, this will be I_0 by 2 plus delta I depending upon the control scheme, depending upon how much you are demanding here. And around the cohesecent whatever it be so it is going to be I_0 by 2 then we have I_0 by 2 minus delta that means it is going to be deprived of current.

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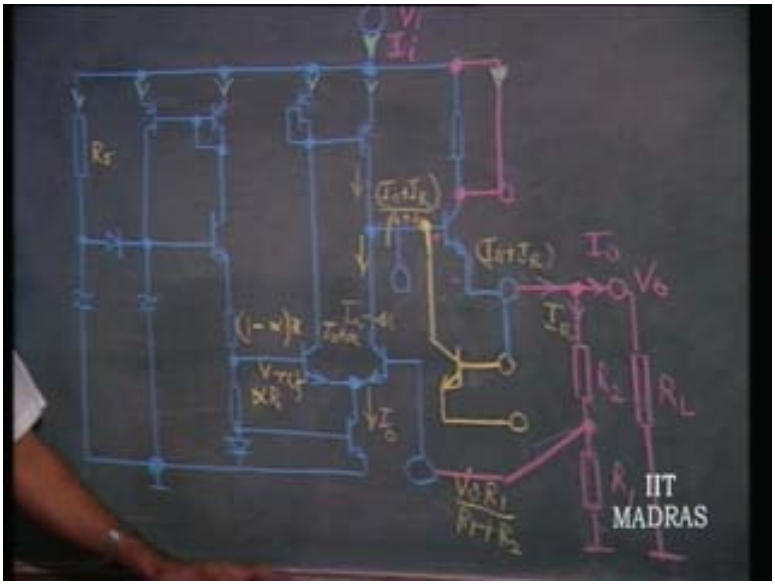

Where is the current going?
This is demanding current here.

How is it demanding current?
You are loading it more and more. When this is getting loaded more and more this current has to come from here. Where is it coming from? It has to come from this constant current source. Originally this was I_0 by 2 and this was I_0 by 2 and this was giving very nearly 0 current. This is what is necessary to sustain the biasing field.

Now, as the current demand here increases this is going to increase and this current is going to decrease. Ultimately what will happen is this can go to 0. That means most of the current is going to be demanded by this. The value of this current is I_0 itself because by that time this transistor is going to be deprived of all current and this current is going to be drawn by this I_0 and therefore this I_0 is going to be pumped into this. So I_0 is going to be pumped into this. Therefore the maximum current that you can have is I_0 into beta plus 1. This is the maximum current that the circuit is capable of giving with this differential amplifier functioning satisfactorily. That is the only available current to you and that is another limitation.

If you demand more current than that this circuit will no longer act as a regulator. This is not coming for what any power consideration; this is independent of the power consideration. What I have done is, I have kept V_0 here and varied this load so that the current demanded is more and more. What might happen is, power dissipated may be still very small because V_i is kept very close to V_0. Therefore I am getting another value for I_{0max}. From circuit operational view point you are getting another value for I_{0max}.

We already have two values for I_{0max}. The lower one will prevail ultimately. This is again something which is not really seen by the user. When he is using it, he might just wonder why the circuit is not functioning in spite of the fact that power dissipation etc is perfectly all. It is simply telling you that do not load me more; I am not capable of giving you that current. So you put the current amplifier that means the solution comes in the form of another transistor being connected in Darlington mode. That will reduce the demand on this and for that load it will function. Therefore this way you can go on doing it until obviously the transistor says that is my maximum current of operation now.

There is a maximum current of operation for the transistor itself. So the third limitation now is I_{0max} can occur simply because the transistor says that current cannot be positive edge, I_{0max}. Transistors themselves will have maximum current of operation and maximum voltage that can occur as reverse bias voltage between collector and base and maximum power dissipation. So, all these three limitations are there even for the transistor. So the final transistor limitation can come about. So I_0 is going to be therefore fixed by all these factors and the minimum of these will be the permissible maximum current in the given circuit.

Now V_i, we know that we have to have this circuit operating for such certain I_0 maximum. Now what is the range up to which V_i can be changed or V_i is permitted to change. This particular thing is very important because after you do this design and come up with V_{imax} and all V_{imin} etc and then you start meddling with the circuit again these things will again change. You will start meddling with the circuit particularly to provide protection for the circuit. And at that point of time you should not forget about these limitations. These limitations will now change when all the protection circuitry comes into picture. Now without the protection circuitry coming into picture we know that V_i can keep on increasing now by itself.

How much can V_i increase without going into power dissipation?

With power dissipation we have come up with a V_{imax}. Perhaps we need not bother about minimum in a variable voltage regulator. That V_{imax} is known, power is not at all demanded, it is not loaded.

Now I am changing V_i, breakdown, what is going to breakdown?
Obviously the collector base voltage will keep on increasing.

This voltage is remaining constant, what is it?
It is V_0 plus V_{gamma}. And this voltage is going on increasing. This collector base breakdown voltage is the limitation of that. Now, as far as that output transistor is concerned. But other transistors might be having more problem than this in terms of breakdown voltage. Therefore you have to see all the transistors and see what the collector to base voltage of all these transistors are. The lowermost transistor is the one which will most probably likely to carry the highest breakdown voltage in the given situation if it is connected to the input. If it is not connected to the input you do not have to bother.

For example, particularly here this potential can keep on increasing and this base potential is less than the output potential by R_1 by R_1 plus R_2. So this collector base potential is definitely greater than the collector base potential of this. Suppose now you are changing V_0 itself, as far as this is concerned you are not bothered about it now because V_0 itself is very high because V_0 is V_{ref} into 1 plus R_2 by R_1 corresponding to which V_i has to be still higher. So you have to worry about that V_{imax} which comes about due to that not when this is at a certain V_0. Here, as far as this transistor is concerned it is only V_i minus V_0 differential and that will be always less than V_i whereas other transistors are there wherein collector base potential can be higher and they might breakdown. Now you come to this point, just this may be a trivial situation. This is V_z the current in this is going on increasing, this is V_i minus V_z by R_s.

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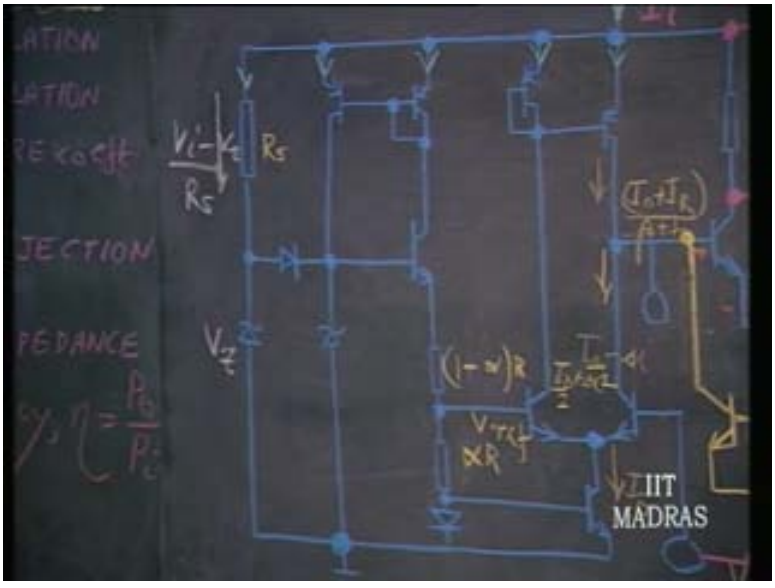

There is a maximum current limitation on the Zener, because of its power dissipation etc there is a maximum cover current limitation on the Zener. That might exceed and that will give you another value for V_{imax}. So you have to be very careful in your design. At all points you have to see that if I increase this voltage is there any device it is going to breakdown. Here it is this transistor alone which will have. In this you have to identify because we do not know how the transistors various transistors are connected so you have to identify.

Actually this is always at V_{gamma} less than this and this is always set to V_{ref}. And if you are having output voltage always greater than V_{ref} it is this transistor here which is always having problem, it is not even this transistor. Therefore you have to evaluate all the limitations due to breakdown, power dissipation and the basic maximum of current etc which is occurring in various devices before you conclude which is the final thing that limits V_i, what is it that limits I_0?
Now that we have understood something about the limitations, given a circuit you can find out the limitations or given the limiting values you can design a circuit. This is up to the designer's concern. But you should totally aware of all these limitations. Next, we have to protect.

Why protection?
Protection comes into picture only if we have not understood the circuit. If you have understood the circuit there is no need for any protection. But we cannot guarantee that everybody who is using this circuit has understood the circuit. So protection is an important part of all the circuits dealing with high power. Basically we have some ICs and then the discrete transistors attached to this which is really carrying the high current. And if it is these discrete transistors which would like to protect because they are the costly elements now.

The IC may be pretty cheap. So when it involves large amount of current drawn etc we would like to have I_0 versus I_0, V_0 versus I_0 absolutely constant at V reference into 1 plus R. But obviously because of all the limitations that are occurring we would like to limit the current to a specific value. This in a given design might be coming about because of the following factor, may be because of power dissipation, may be because of the current itself getting limited so these you have to investigate at. So there is obviously a maximum current which you are letting it to be permitted to go through the output transistor here.

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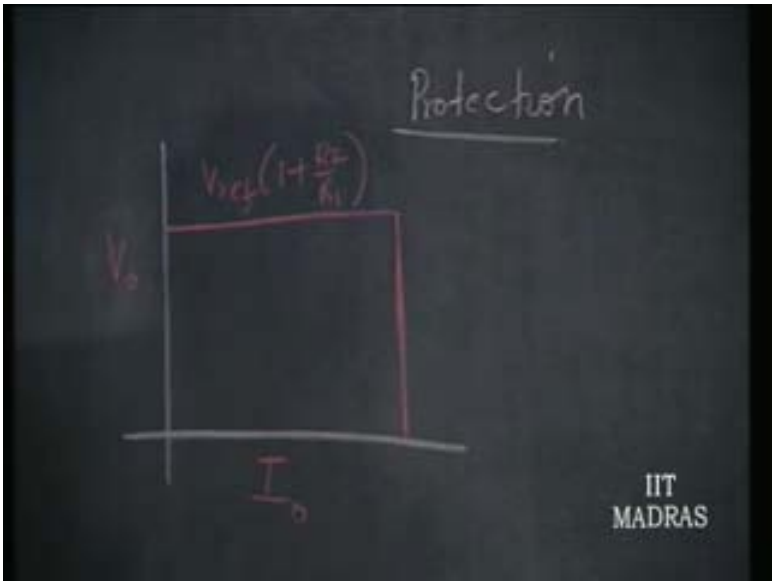

So where is the maximum dissipation in the IC concentrated?
It is in the output because all these things are carrying very small amount of current negligibly. This is the only one which is carrying the highest current in this circuit. Basically the output transistor has to be protected.

How do you protect it?
Why should it be protected is mainly because as I go on connecting higher load or lower resistance to this, this is delivering that current assuming that the design is properly done here. That means there is no question of this comparator misbehaving. The current division is still allowed. In such a situation this current is going on increasing when power is going on increasing and because of that there is a limitation. Therefore I do not want to permit such a higher current flow, how should I do it?
So one way to do it is, convert this as this is nothing but a voltage source and that is why irrespective of the load output voltage is remaining constant. At this point of time I would like to convert it into a current source.

The moment current is trying to exceed a certain value I do not want this circuit to behave as a regulator, purposely I am preventing it from acting as a voltage regulator because I know that this is a damaging current that is likely to flow and therefore more than this current if it is flowing through this it will damage this so I will convert this whole thing into a current sense. So, current sense is done. These are terminals for sensing the current. How do you sense a current? The current can be sensed always by using a series resistance.

So I am now using this series resistance to protect but actually if I want to limit the current I can as well put a series resistance but that is a bad way of doing it. That is, I do not have to worry any anything about the whole thing, I want to protect this transistor so I will put a series resistance here and then connect the load. But that immediately

degenerate the performance of the voltage regulator because series output resistance is increased.

You cannot put a series resistance in order to protect the transistor. You can only put a series resistance low enough only to sense the current through the load. So the load is now put here and this is the R short circuit as we will call it. Actually I am not shorting, this resistance is supposed to sense the overload current. This is sensing the load current in this because it is coming in series.

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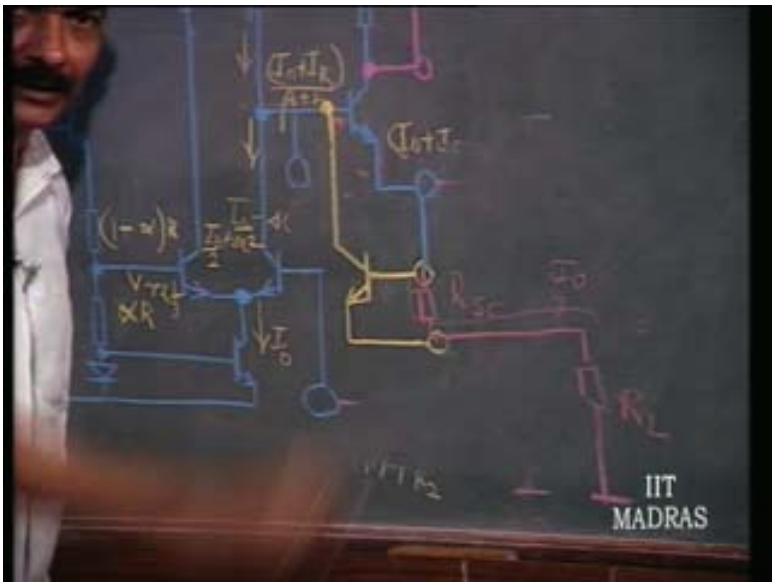

Forget about the transistor for the time being. The voltage across this is I_0 into R_{sc} that is going on increasing so if this voltage increases above a certain value you divert a traffic, traffic is this, say for example, this is the Mount Road the main, the high current. The only way to prevent the traffic jam is to divert the traffic. Why is it that the Mount Road is having traffic jam problem? It is because there are feeder roads coming into the Mount Road. This feeder is coming from this so I divert the traffic here to another road the bypass so I divert the traffic. Therefore this is deprived of further excess traffic and therefore there will be constant traffic here that high traffic which is permitted to flow through Mount Road will now flow. So this is the sense resistor which will tell you when exactly you have to start the diversion.

The moment this voltage becomes equal to, this is done electronically V_{gamma} this is the police fellow, so the instruction is very clear, the moment this becomes equal to V_{gamma} this is forward biased this is already reverse biased so this transistor comes into the active region until that time you have told him you can sleep. But the moment the traffic jam is likely to occur you awake and open the bypass road. So this is the bypass road where the excess traffic is now flowing.

Here this is the original transistor and this current is going on increasing. So I sense this current using R_{sc} and then I obtain this as a voltage. This current is sensed and obtained as a voltage and then is again converted back to current. It is very sensitive because even if this voltage changes slightly there will be more opening of this and more of this traffic is involved to this. So that is negative feedback. Originally this traffic was only flowing through this, this was not coming into picture if I was flowing I into beta was flowing here that was beta. Now if I is flowing here it is due to Meddler current source with current feedback. So there is now exact relationship between this current and this current. So this is a current source now dependent only on this and these are following one another exactly.

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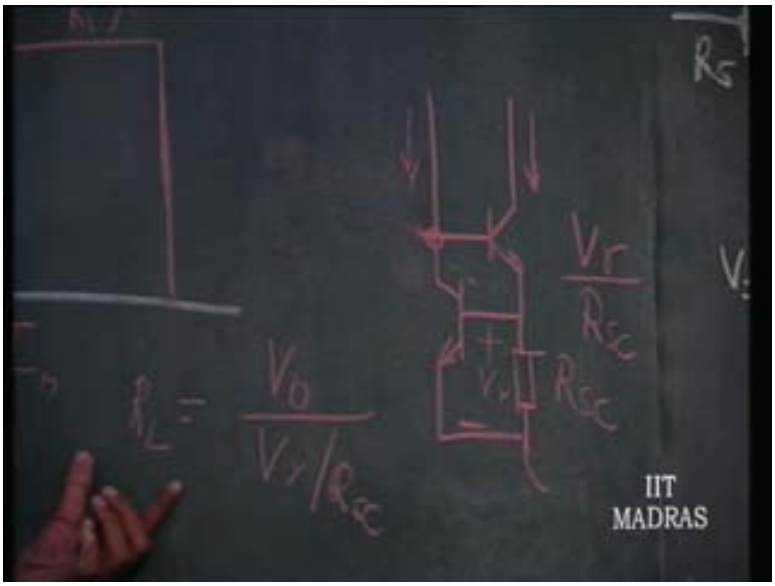

What is the current in this?
It is V_{gamma} by R_{sc}. So this is changed about current source now. That means if I connect a load resistance value here which is lower than V_0 by V_{gamma} by R_{sc} that is the lowest resistance it can tolerate then put lower resistance than that and the current flowing through that load resistance is going to be now V_{gamma} by Rsc. So this kind of a limitation is now going to protect your circuit as is explained here graphically. This is the [d…] voltage regulator. Here you can sustain any output voltage which is no long voltage regulator it is a current source of V_{gamma} by R_{sc} constant current. So this is the way we can protect. This transistor is within this device itself. This is not a good way of protecting the circuit.

Here the P_{dmax} is governed by V_i minus V_0 into I_{0max}. The maximum current is flowing but V_0 can be anything now starting from this value down to 0. Let us say it is real short circuit R_L is real short circuit that means V_0 is equal to 0 then the entire input power is getting dissipated in the IC. Now this will give you another V_{imax} which may be pretty low and it is fertile to design a circuit for this V_{imax} which may not occur, V_i minus V_0

may be pretty low. Therefore if I design this circuit only for this V_{imax} it is not going to be an efficient design. So this kind of a scheme has to be modified.

What is the use of converting it to a current source?
You convert it into anything. As long as you are protecting the transistor it is not necessary that you should not convert it into a current source. So, depending upon what V_0 is likely to be I would like to therefore convert it into something which is not at all a current source that this is fold back the short circuit protection because after this load resistance is connected for all the lower value of load resistances it need not be a constant current. That means I have to sense the output voltage also apart from output current. If the output voltage becomes different from this then I need not sustain that constant current through the resistor.

So we will discuss in the next class this fold back short circuit protection which is the one that is to be recommended in regulators which are going to be remotely located where if a short circuit occurs I may not come to know immediately and the poor regulator might be by that time fail. So this kind of thing particularly becomes necessary for the remote locations where until somebody comes and repairs it should be in this mode.