Semiconductor Device Modelling and Simulation
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Lecture – 31
MOSFET

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Hello, let us discuss MOSFET, welcome to lecture number 31, so, in this lecture we will discuss the MOSFET I-V characteristic and the small signal equivalent of the MOSFET.

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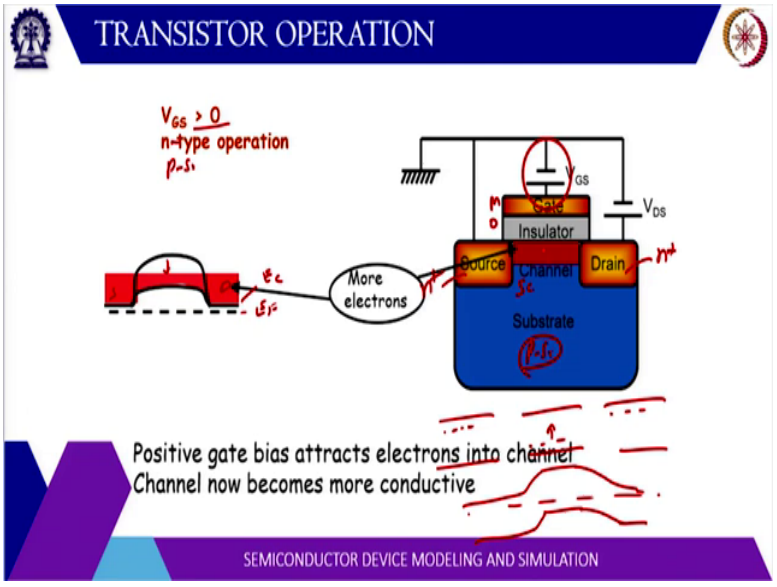

So, if you look at this diagram here, we have already discussed metal oxide and semiconductor structure, MOS structure and we know that if you draw the band diagram

because let us say this is P-type silicon this source is n-type then is also n-type. So, if you see their band diagram here, source then a n-type. So, their permeables are here substrate P- type so, permeable is here when this formulas are align.

So, there will be some kind of band bending here. So, this will be here, this will go up, this is here, this will go up, it will go up. So that is what you will see so that band structure is shown here. So, this is source, this is drain which is lot of electrons. Here there are holes and there is a barrier there basically and this is the Fermi level. So, this is let us say this is your e c so, these electrons all the source and then both are filled with electrons.

But due to this barrier they cannot cross over. Now, when we apply the gate bias, what we do? We convert this P-type silicon into n-type silicon. So that means this Fermi level is coming close to the conduction bandage. That means this barrier is reducing now, once this barrier reduce for a positive, gate voltage, so that is n channel MOSFET or P-type silicon substrate.

Now, due to this channel, this electron can move and we have a conducting channel here. Now, this is little exaggerated is usually quite thin. So, quality bias attracts the electron and then it allows the current to flow between the source and drain.

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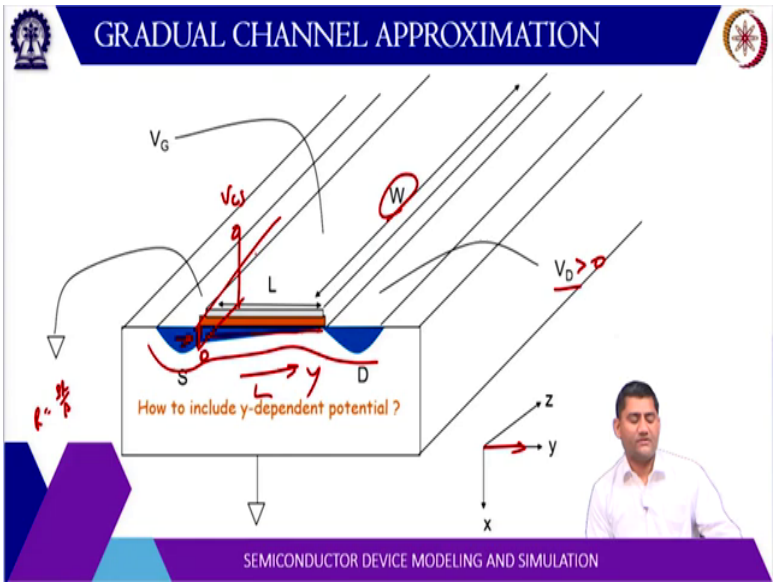

Now, the procedure that is used for calculating the I-V characteristic of MOSFET is called gradual channel X approximation. So, usually it is applicable for long channel devices for short channel. We have to make some changes but let us go ahead with this derivation so on

the source side. So, there is some V gs volt here and then the depletion region here and then there is a channel region here.

So, there is a depletion region this is channel region. Then, as you go to the drain because V D is greater than 0, so, at the drain end V GD is smaller. So, this channel actually reduces here so, this channel is gradual. So, let us say this axis is y axis, this axis is y axis. So, along the y axis, as you move from source to the drain, the channel which is basically reducing or drain voltage.

Now, if the drain voltage is very small then we can assume more or less constant channel. Let us say V D is 0 then this channel will be uniform and as the drain voltage increases this channel reduces. And if you look at the 3D picture, this is the length of the channel and there is a width of the channel. This is pretty large because larger width allows a larger cross section, so, more current will actually flow.

Because if you look at the from source drain side it is the current is going through this thin line here. And then which is extended in in along the Z direction. So, through this area because if you recall that R = rho L by A. So, area is more the resistance will be less so, the width has generally we kept quite large for the large current to flow.

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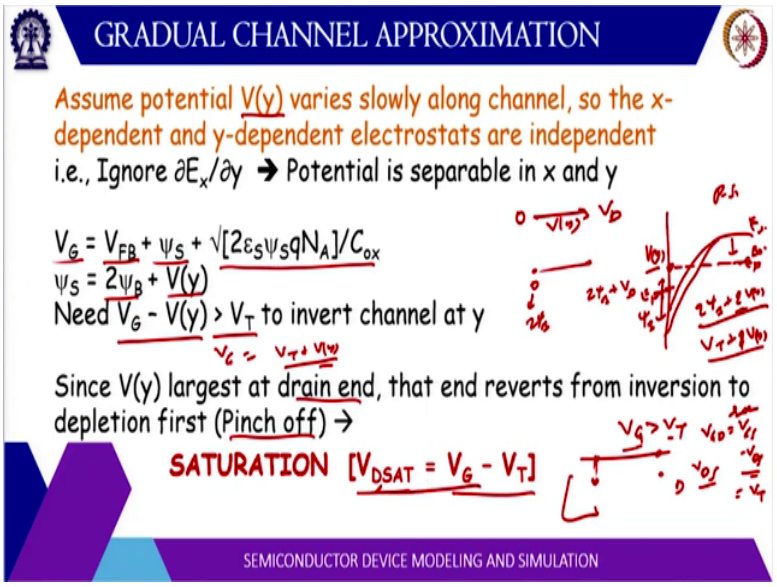

Now, let us assume this potential along the channel is varying slowly. So, at the source side it is 0, at the drain side it is V D. And individual we call it V as a function of y. So, these are the two boundary condition. Now, if you look at the channel, there are two times types of electric

field. One is due to the gate, so, there is a vertical electric field. One is due to the drain voltage, so that is horizontal electric field.

So, there is electric field in the X star XR, due to gate voltage, electric field in y direction, due to the drain voltage or drain Source voltage. And in gradual channel we can separate these two potential in x and y direction. Now, alright, the gate voltage is basically flat band voltage plus the surface potential plus the depletion charge by C ox. And of course, for when the gate voltage is more than threshold voltage.

This psi s should be more than 2 psi B. So and if this becomes less than 2 psi B then there is no more inversion there basically. So, no more inversion channel there. So, psi s the surface potential can be written, as so, at the source and this is 2 psi B and on the drain side it is 2 psi B + V Y. So, here V Y is 0, so, it that the psi s is 2 psi B here and here is 2 psi B + the V D the drain voltage.

So, the voltage that is required to create a channel is now V G – V Y should be greater than V T. So that means your V G should be greater than the gate voltage should be greater than V T + V Y. So that means some extra voltage is required to create the inversion when the channel voltage has changed. Now you can understand like this. If you recall the band diagram, let us say this is your P-type silicon this is a band bending here.

Let us say this is your Fermi level it is your intrinsic level. So, it is P-type here and it becomes n-type here. Now, this is the situation when a Fermi level is same here when this channel has certain voltage let us say V. So, if there is a channel voltage, let us say V as position by, let us say general voltage is V Y. Then this Fermi level here will change and how much it will change it will be – Q times V Y.

So, voltage is positive, so, this will reduce because now V Y is positive. So, – Q V Y is negative. So, permeable here will be somewhere here so, this is the Fermi level in the channel. Now, for the inversion to exist, the gap between these two should be psi V. So, it should actually go down even further, so that means the gate voltage required for the band bending is even more so.

The band has to bend to psi B + this Q times V Y. So, this once it has to change so, your threshold voltage is effectively has changed. So, this is V T + Q times. So, for voltage we can of course, remove the Q. Because Q when voltage, is multiplied by Q the energy. So, these are the energy, so, we have multiplied by Q, voltage we do not have to multiply by Q so, it will be V T + V Y.

Now, if you remember all these voltages are with respect to body. So, when we say V GS with respect to source. And source and body are connected together, so, this V Y is with respect to the body. So, this is the Fermi level in the body, this is the Fermi level in the channel region, so, the voltage that is required to invertise V T + V Y. So, since V Y is largest at the drain end.

So, at the drain end inversion will disappear first and that we call it pinch off and the point at which this goes off from the inversion region we call it saturation. So, the V D the drain voltage for the saturation is V G – V T. So, you think like this, let us say this is your V G and let us say V G is more than V T. So, at the source side because this is V G with respect to source and body less are connected.

So, V GS is more than V T so, channel will exist here. Now, on the drain side, if you see the voltage is V DS with respect to source. So, the difference between the grid and the drain V G V D will be V GS – V DS. So that is a difference so, now the voltage difference is small here, so, it has to be more than V T for channel to exist. And the point where this is x axis is equal to V T.

So, plus this is equal to V T, so that requires that V GS – V T = V DS or saturation region. So, this is for saturation condition that V Z = V T. So, we get this expression for the saturation region.

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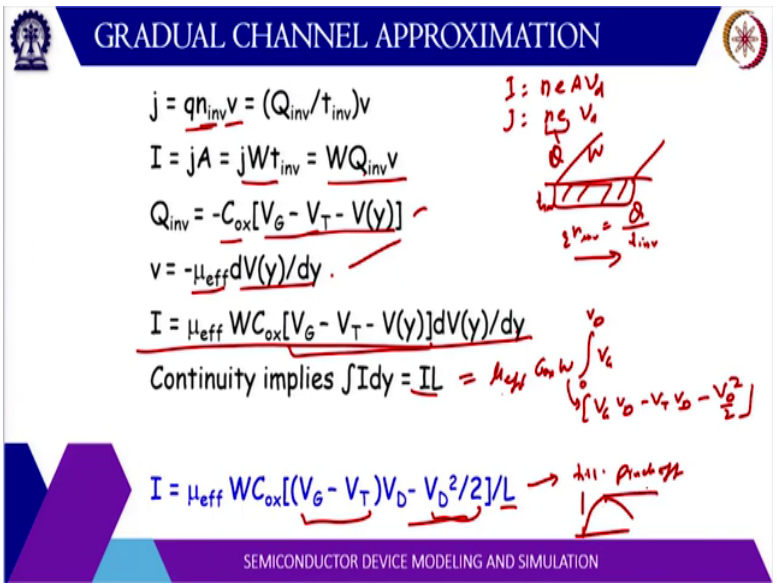

Now, along the channel region we can write the equation of current. So, current density, you know there is a total current if you recall the expression I = n e a times the drift velocity. So, j is basically divided by A so, it is n times e times V D. So, this n is basically the total charge, charge per unit volume. Because n is the carrier density is the charge on this carriers. So, this is a charge density per unit volume times velocity.

So, j is qn times velocity. Now, qn inversion if you look inside the inversion region, the total charge is basically n inversion times the area. So, area is basically this width times this inversion layer thickness. So, this n inversion is basically or qn inversion is basically this charge per unit area divided by inversion layer thickness. And of course, if you multiply by the area. So that is area is W times T inversion.

So, j times T inversion and then that is WQ inversion times V and Q inversion is given by C times V G – V T. And because this channel voltage is varying so, V G – V T – V Y and velocity mu effect M times gradient of the potential that is, electric field, a negative gradient of potential along the y direction. Along the channel directions then, if you substitute here these two expression then you get I = mu effective WQ is this C ox V G – V T – V Y times DV by dy.

So, this is your expression for the current. Then, of course, when you integrate take dy on the other side, so, when you integrate. So, I dy is I times L = mu effective C ox W times integral of this times D V so that will be V G times the limit will be 0 to V D. So, 0 is of course, 0 so, if you integrate it, you will get it V G times V D – V T times V D – V D square by 2. So,

your overall expression becomes I = mu effective C ox W by L times V G – V T times V D – V D square by 2.

So, this is the expression till pinch-off. After pinch-off the current become constant. If you use this expression, what you will get you will get that current goes up then burnt pinch of it will come down from this expression but in reality, it does not come down, it becomes constant beyond pinch-off or we call it saturation region.

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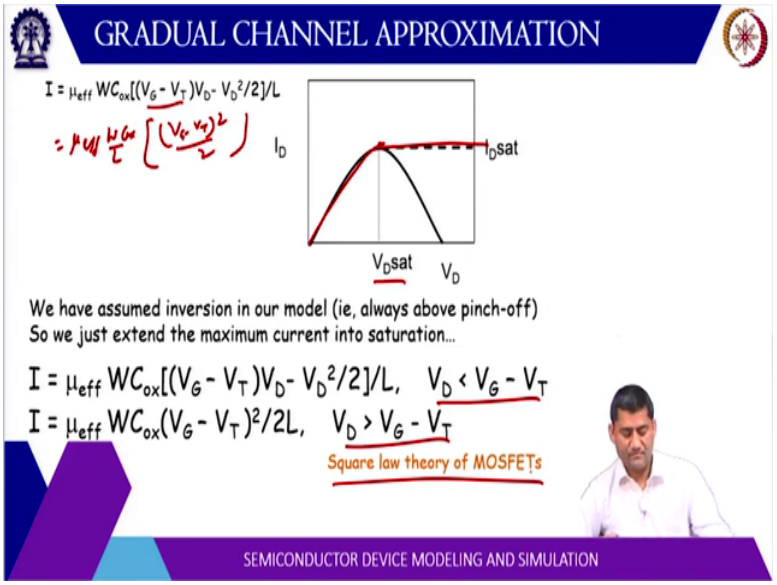

So, your I-V curve basically look like this. So, up to saturation, this is the expression beyond saturation the current at this V D set. So, current at the V D set will be mu effective, W C ox by L times at V D sat is V G – V T. So, if you substitute V D = V G – V T you will get V G – V T square – V G – V square by 2 so that is 1 by 2 so, these are two expression for linear region and for the saturation region this is the equation for the current. And of course, this is valid for long channel devices.

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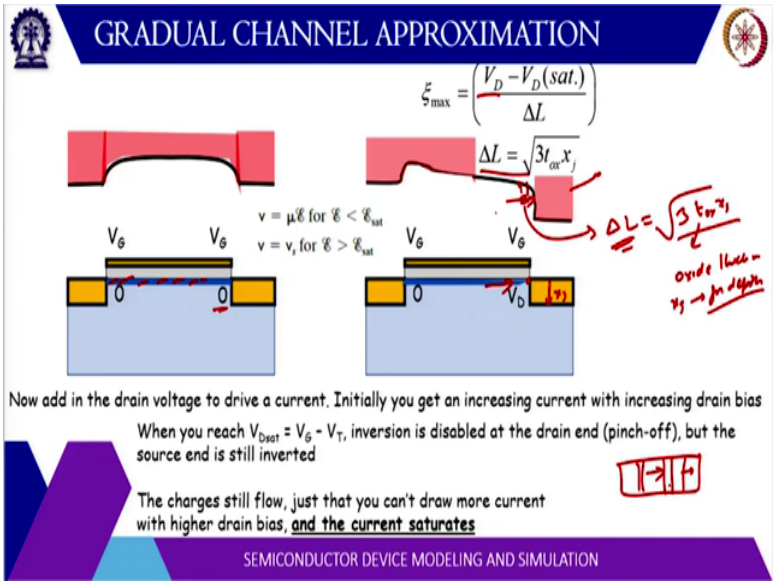

Now what happen when you go beyond pinch off? So, for a small voltage, let us say drain is close to 0. This channel is uniform when the drain voltage increases then the channel start to disappear here. And there is a small this is little exaggerated this small L is there where channel does not exist. And this actually region absorbs most of the extra electric field. So, in the length of this region which is delta L is actually pretty small.

So that is usually 3 times t ox times x j, t ox is your oxide thickness and x j is basically the junction depth. So, this is will be your x j junction depth. So, if you keep small Junction depth then this delta L will be small, so, it will be more close to a ideal MOSFET and the electric field in this region will be because potential up to V D set false across here. So, whatever extra voltage you apply here, more than V D set will fall across this delta L.

So, the electric field in this region will be V D – V D set divided by delta L. Now, delta L is more or less constant. It does not vary with the voltage because the field is pretty high here. Now, you might be thinking that in this region there are no carrier so, how the current is flowing. It is very similar to the BJT structure, if you recall, in case of BJT Base Emitter Junction is forward bias but the base character is reverse bias.

So, there is a depletion region here. So, there is no carriers here but the carries that are coming they can go through it. So, same thing is happening here the carriers that are coming from this channel region. They can go through this depletion region and they will move actually at high speed. So, it is a depletion region with no carriers but carriers moving will be allowed to go through it.

So, it does not contribute to the increase in the current but it maintains that the current will be constant.

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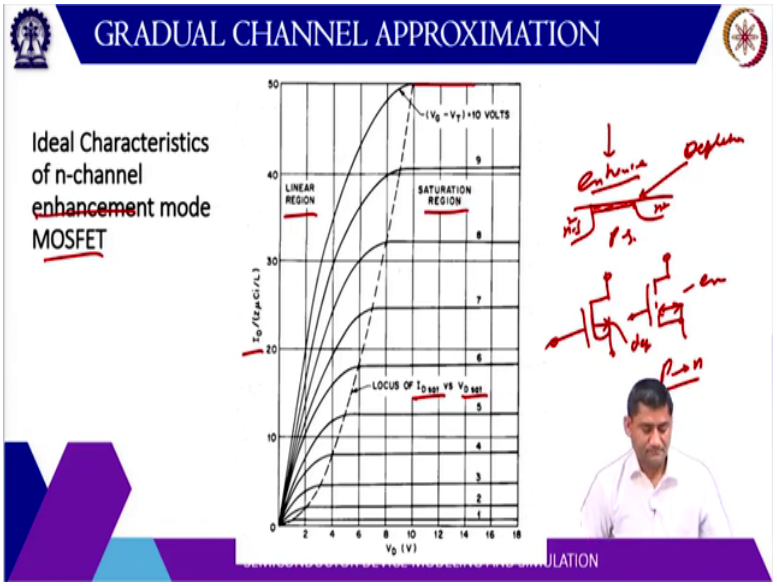

Now, this is that ideal I-V characteristic for a MOSFET. Now, here the name is written enhancement mode. So, basically there are two types of mode basically one is enhancement mode another is depletion mode. So, in enhancement mode normally the MOSFET is off. So, let us say this is your P-type silicon, this is n-type, silicon n+, this is also n+. So, it will not conduct basically.

So, the when you have to apply the voltage then the inversion layer will be created then the current will flow. So, this is called enhancement mode you have to apply the voltage. In depletion mode what happens? You have a small layer of n-type silicon there. Then this channel is already existing. So, when you do not apply any gateways, the current will flow. So that is called the depletion mode.

So now, what you have to do? You have to apply the voltage to deeply it is a small layer. So, you have to apply a gate bias so that it does not conduct. So that is a depletion mode MOSFET. So, if you see the their symbol, this is your MOSFET. So, here it is connected in some cases you may see that this is not connected, so, this will be enhancement mode and this will be depletion mode.

Then there may be another variation to this one let us say this source is connected through this or the arrow direction will be either this way or this way. So, this arrow always point from P to n. So, this is P to n -type region, so, if channel is n channel so, it will point basically away. And what is P channel? It will point towards the channel. So, these are the meaning of these symbols of different MOSFET that you may encounter in the literature.

Then here, if you look at the I-V characteristic. So, current is increasing in the linear region and then it actually saturates. And then this line locus of I D set versus V D set, can be plot like this. So, this is where V D = V gs – V T. So, this is another curve for I D V D at V D set. So, this is basically at V D = V D set. So, these two regions, the linear region and saturation region can be separate on this. I D V D curve.

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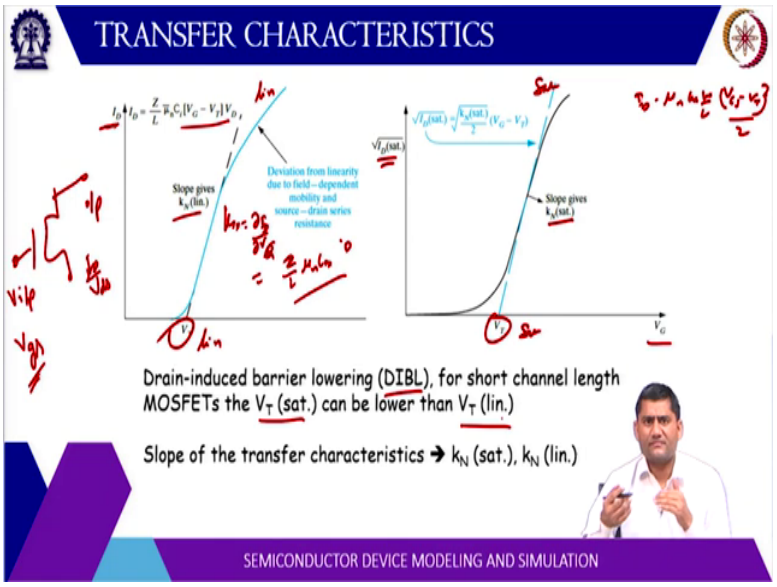

Now, we can also obtain the transfer characteristic which is basically I D versus V G. Because if you see here there is a gate here, there is a drain here. So, this is your input and this is your output, so, your V gs will be the input V ds and I D will be output. So, at the input you are applying a voltage that is V G, I D is at output. So, this characteristic is called transfer characteristic.

Because output is at the dependent variable is from the output and the independent variable is from the input. So, it is a transfer characteristic and when you plot I D V G you will get some linear region and this is for linear region basically. So, this linear region, the slope if you obtained so that slope will be the K n will be del I d by del V G. So that will be Z is basically the width, so, you can have Z by L mu n C ox times V D.

So, this will be the slope some places they also obtain the slope of this square root of I D versus V G. So and this is done for the saturation region, so, this is in linear region. This is in saturation region. So, in saturation, I D = mu n C ox W by L V GS – V T square by 2. So, if you take the square root then becomes proportional to V gs – V T. So, the slope will gives you the K n in saturation region.

And where it intersect the x axis, we call that as a threshold voltage and these two threshold voltage may be slightly different. So, one is basically V D set corresponding to linear region. Another V D set threshold voltage corresponding to the saturation region and there are some advanced phenomena called drain induced barrier lowering. So, for short channel MOSFET VD set can be lower than the V T linear.

That is because at higher drain voltages the role of the gate actually get reduced. Because of this band bending so that you will see in next lecture.

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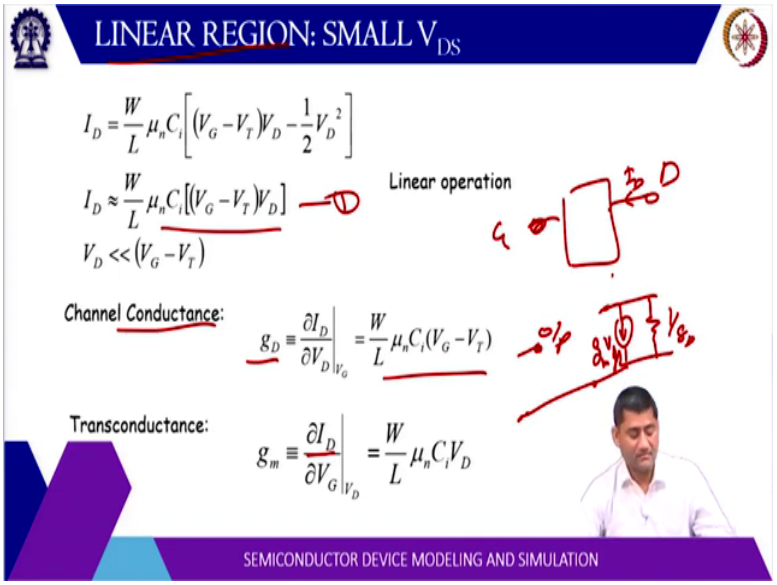

Now, if you want to get a small signal equivalent circuit. We can differentiate this let us say now considers a linear region. So, the channel conductance is del I D by del V D. So, you can look like this. This is your input gate this is output drain. So, an output current is here at ID. So, del I D by del V D is the output conductance or the channel conductance. So, this is the output characteristic.

Then, when you differentiate this equation here del I D by del V D so, you will get W by L mu n C ox times V G – V T. So, this one is output the conductance, so, you can also represent this output as a some resistance here and this will be 1 over G D. Then trans conductance is output current derivative with respect to the input voltage so that again, how can you differentiate this equation One you will get W by L times mu and C x times V D.

So, this is basically you can write I D = g M times V gs. So, this is a characteristic of the output. And of course, input there is a gate here so which is kind of open because no current flows through the gate. So, this will equivalent circuit of a MOSFET. Here we have ignored the capacitance we will consider them after this.

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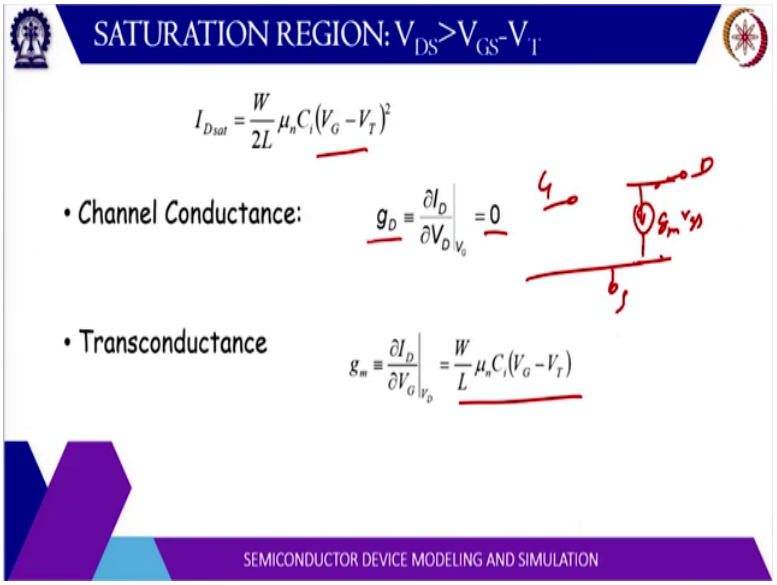

Now, in saturation region the current is constant with respect to the drain voltages only dependent on the gate voltage. So, now here the equivalent circuit will be let us say this is your gate. So, G D 0 because there is no variation of I with respect to drain voltage. So, this will be open basically then g m is del I D by del V D so that is if you differentiate with respect to VG it will be two times V G – V T.

So, you will have this think here. There is a current source here g m V gs. So, this is your drain, this is the gate, this is the source. So, for such resurrection, this will be the equivalent circuit. This R out is basically open. So, there is, the conductance is 0 basically or infinite resistance.

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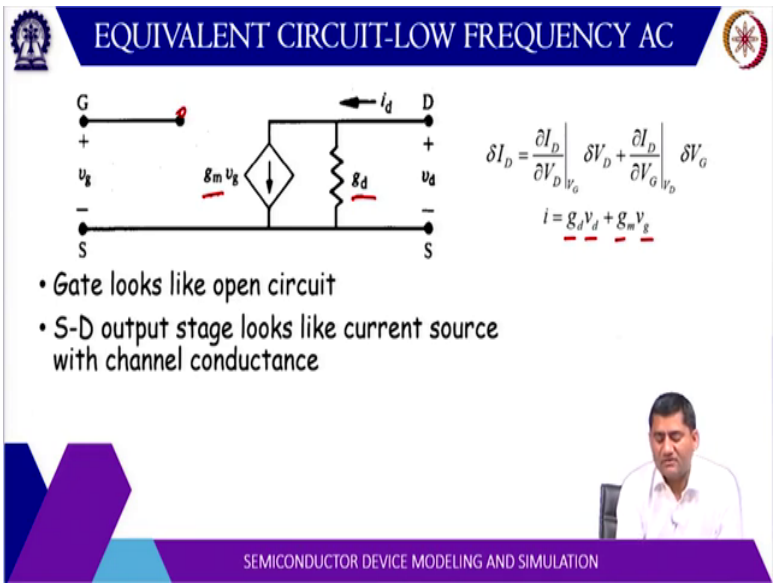

So, this is a equivalent circuit. So, here you can substitute the value for g m and g d for different regions, saturation region and the linear region. So, your I basically can be written as g d times v d + g m times v g. So, this g m is contributing the current due to the gate voltage and g d is basically the current due to the drained voltage.

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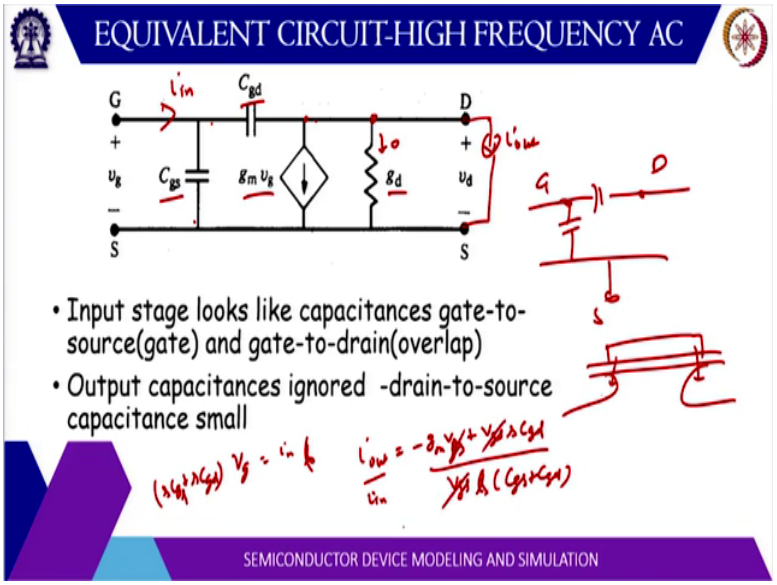

Now, at high frequencies, the capacitance layer all basically, so, you can see here C gs. C gs is the gate to source. So, if you see here, this is the gate, this is the source there is a drain here. So, this gate can have a capacitance with the source. It can have a capacitance with drain also, so, this is called C gd, this is called C gs and rest remains same g m v g and g d. So now, from where this capacitance actually come.

Let us say this is your drain region source region so, this is your gate here. Now, this gate has some overlap with the source. It has some overlap with the drain, so that gives rise to some kind of capacitance. So, gate-to-source capacitance and gate-to-drain capacitance and they actually enter into the picture here.

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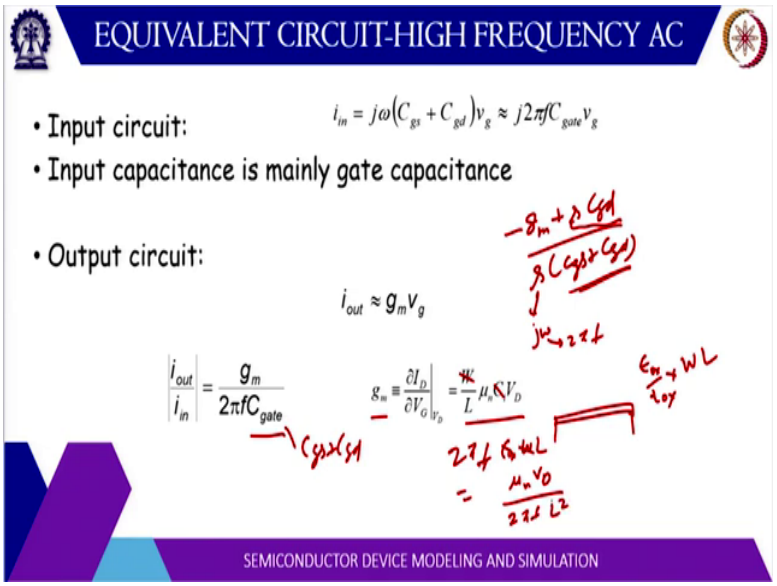

So, for input circuit we can actually calculate if you consider the circuit. Let us say there is I input here and then let us say we calculate the I output, so, let us say we sort it and we calculate I output. So, if we know the I n we can find out v g. So, v g will be I n times these two impedances C gs and C gd because this is sorted here so, and they are in parallel. So, their admittance will actually add up, so, I can be written as v g times admittance.

So, admittance is basically SC gs + SC gd times Vg = I n. And I out you can write the K CL here. Now here the current will be 0 because this is already sorted. So, your I out is basically these two currents basically I out is negative of g m v g and plus V gs times SC gd. So, this will be a I out then you can take the ratio of I out and I n so, both have g m V gs. This is V gs.

And then we so, this is basically, if you take I out by I n you will get V gs times SC gs + C gd. So, V gs will cancel out. So, you have g m – SC gd divided by SC gs + SC gd. So that is what is shown here. Let me know the expression – g m + SC gd divided by SC gs + C gd. Now, g m is quite large. Actually so, you can ignore this SC gd. So, you have this g m by S times C gs + C gd.

So that is a total gate capacitance. So, this is for given frequency if you use S = j omega and omega is 2 pi f. So, the magnitude can be done as g m by 2 pi F times C gate. So, C gate is C gs + C gd and this gate voltage can also be calculated. from the gate structure because this is a total gate capacitance. So, this is oxide here, so, epsilon oxide by T oxide does the gate capacitance per unit area times W times L.

And for MOSFET g m is del I D by del V G which is W I L mu 1 C ox times V D. And that has to be divided by 2 pi f times C gate, so that is C ox times W L. So, this W will cancel here C ox will also cancel here, so that comes out to be mu and V D by 2 pi f times L square, so, mu and V D by 2 pi L square.

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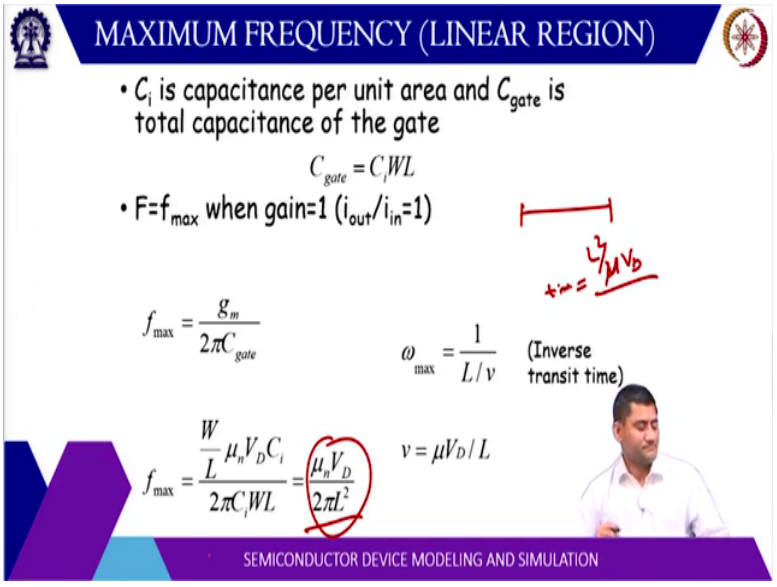

And when this is equal to 1 so, this I out by I in. This is I out by I in and there is a f here now when this gain is 1 F can be found from this one. So, F will be mu and V D by 2 by L square. Now, if you read this expression carefully, frequency will be in terms of the time it takes for the carrier to cross over the channel region. So, it will be L by V and V = mu times e. So, mu times e and e is drain voltage divided by L.

So, L square by mu V D and that is what you have here. L square by mu V D is the time and progressively of course opposite. So, frequency is mu V D by L square. So, 2 pi f is mu V D by L square. So that way also you can find out this unity gain frequency that is for linear region.

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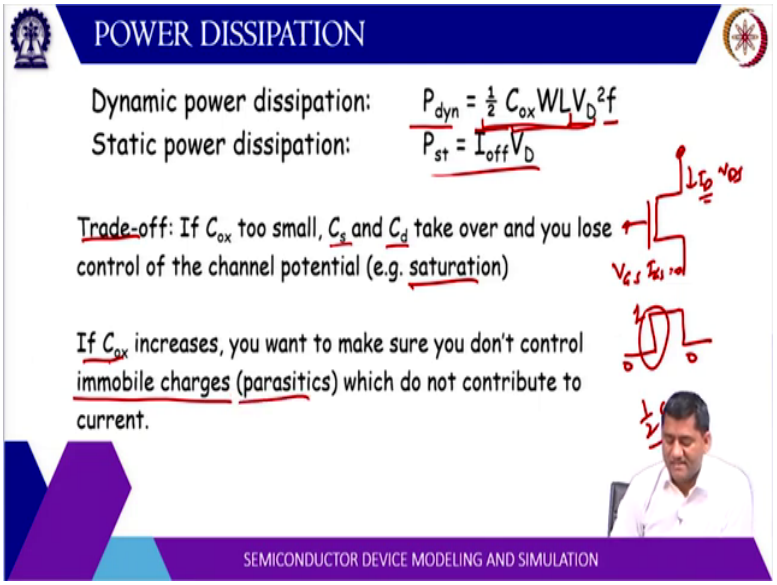

Now, another consideration in case of MOSFET is the power dissipation, of course the static power dissipation. So, if you look at the MOS structure here from the gate side, there is no current drawn. So, V gs times I gs is 0 because create current is 0 if there is a I D here. Then the power drawn from the supply connected to the drain side will be I D times V Ds. So, if there is some off step state drain current then that will be the static power loss, so, power dissipation.

The dynamic power dissipation is basically when it changes the state. So, if there is a certain frequency at which it is changing the state. So, for given state change from let us say 0 current to you know or 0 state to 1 state to again 0 state so, for each transition there will be some power dissipation because what will happen? This capacitance will charge and discharge, so, the energy stored by the capacitor is half C V square.

So, this is half C V square. Now C is C ox times W L because C ox is basically capacitance per unit area. The overall constants is C oxide W times V D square. And now this is the energy stored in the capacitor. So, for each frequency it will each change in the state. This power will be dissipated and come back. So, the dynamic power is basically the power stored in the capacitor times the frequency so half C V square times f.

So, if you look at the trade-offs, so, if C ox is too small, C s the source substance and drain coefficients may take over and you may control the loss of the control over the general potential. And that is the saturation effect. And if you increase the C ox then of course the dynamic power will of course increase as well, as it may affect the immobile charges, also so,

the parasitics they also come into the picture. So, these are some considerations by designing the MOSFET.

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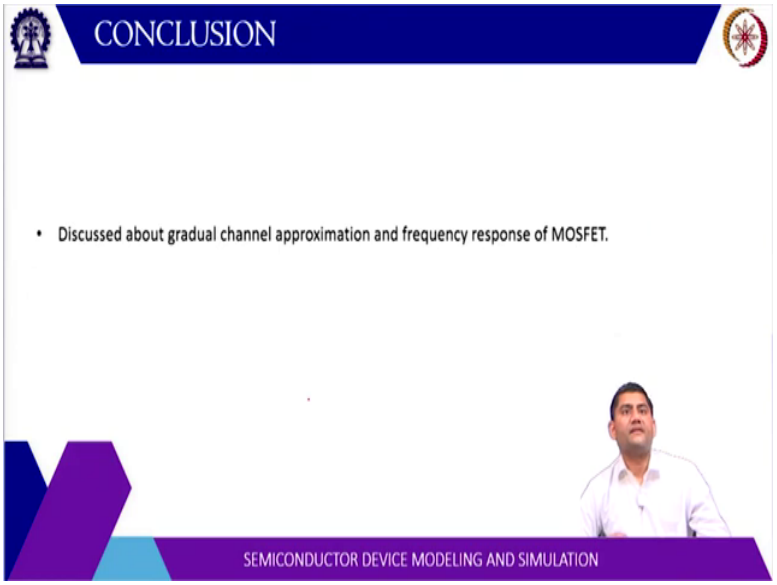

So, in this lecture we have discussed how the gradual channel approximation and the small signal equivalent circuit and the frequency response of a MOSFET. Thank you.