Semiconductor Device Modelling and Simulation
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Lecture – 30
Real MOS (Continued)

Hello, welcome to lecture number 30.

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L30 REAL MOS-CV

- INTERFACE CHARGES
- REAL / NON-IDEAL MOS CV

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We will continue our discussion on MOS structure. So, today we will consider the effect of interface charges inside the oxide and the difference between the Fermi levels of metal and semiconductor and the known ideal or the real MOS CV characteristic.

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REAL MOS CAP

- Work functions different for gate and semiconductor
- Oxides are not perfect
  - Trapped, interface, mobile charges
  - Tunneling
- All of these will effect the CV characteristic and threshold voltage

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So, let us consider work function difference. So far, we have assumed for ideal MOS we assume that there are no charges in the oxide and the Fermi levels were aligned, so, the flat band voltage was actually 0. So, when we apply zero voltage the bands were flat but that is not the situation in reality because semiconductor and metal they have certain back function difference.

And when you do not apply any bias or zero bias under equilibrium, Fermi level will try to align and that will result in the band bending. Band bending can also come from the charges, so, there may be some trapped charges, there are mobile charges so and the charges can come from other sources also. So, they will alter the capacitance voltage, characteristic and the threshold voltage.

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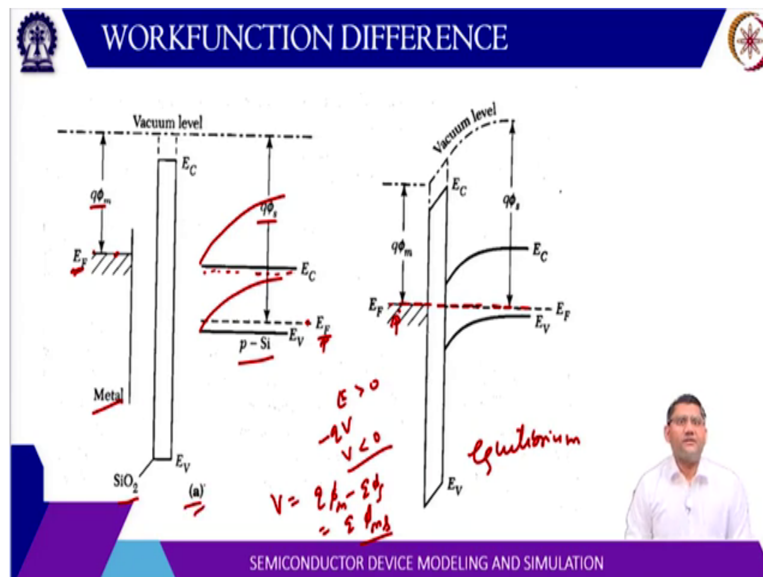

Now, let us look at the typical metal semiconductor p-type silicon and the insulator band diagram. Now, here you notice the Fermi level in the metal and the Fermi level in the semiconductor they are not at the same level. But when they come together, the Fermi level has to be aligned. So, in that case there will be some band bending. So, you can think like this. What we are doing? We are pulling down this Fermi level on the metal side.

So that it aligns and when we pull it down then the other bands will bend on the semiconductor side or you can think like this. We are pushing up the Fermi level on the semiconductor side so that it aligns with the Fermi level on the metal side. So, when we push it then as it goes up, so, it is something like this you can visualize something like this. So that is what you see here on right side and we do it till both the Fermi levels are aligned.

Now, although the gap may be more than the band gap but not all the voltage falls across the semiconductor some of the voltage is taken away by the insulator also. So, therefore, the increase in the band bending on the semiconductor site is not that big compared to the Fermi level difference. Now, if you see this equilibrium band diagram now to get a flat band, what we have to do? We have to push this Fermi level on the metal side to it is original value.

That means the difference between two Fermi levels between E F on metal side, E F on semiconductor side should be the phi m q phi m and the q phi s that should be the difference. So now, Fermi level on the metal side has to go up that means the energy is positive. That means energy is minus q times voltage that means the voltage is negative. So, we have to apply negative voltage.

And what will be the value of that voltage? That voltage will be equal to q phi m – q phi s or curl q phi ms. So, phi ms is basically phi m – phi s and you see the value phi m is less phi s is more so, phi ms is actually a negative value. So, phi ms is the voltage that is required to be applied on metal side for the bands to have a flat structure like as if you know in the diagram A.

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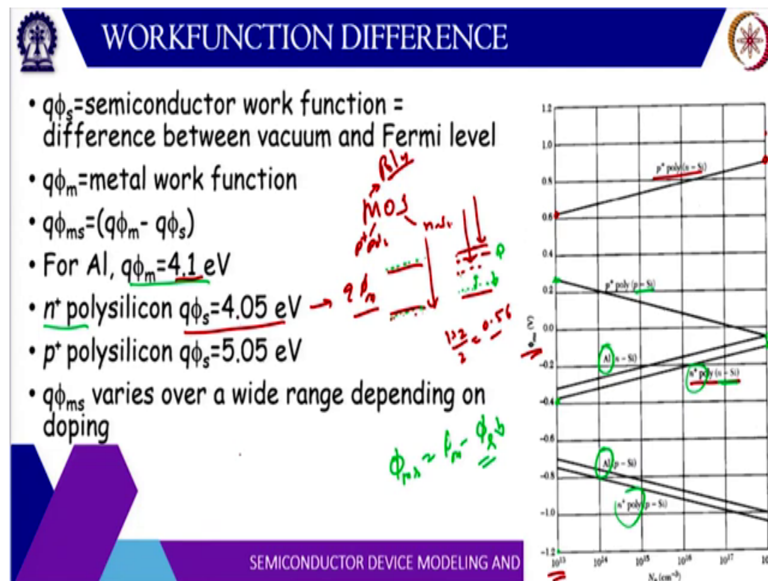

So, this is the continuation of the work function difference to the band diagram. Now, here is one picture which shows how the phi ms changes for different combinations of MOS structures. Here, metal is replaced by some poly n + poly or p + poly and if you notice for

n-type polysilicon, q phi is 4.05. So that will be basically, that is in place of metal, so, we can call it q phi m in our convention.

And if you see the first structure here which is p + poly and n-type silicon. So, this metal is p + poly and this semiconductor is n-type silicon. So, if you see the p + poly, the Fermi level is somewhere inside the balance band for n-type silicon Fermi level is somewhere here. Now, when the doping is very large, this will be close to the conduction bandage and then this is phi m this is phi s.

So, this will be roughly equal to the band gap, so, you see here around 10 is to power 18. So, if you go further, of course, it should reach around more than 1 basically. And when the doping is small, it should be in the middle and that should be the difference will be half of the band gap. So, half of the band gap is around 1.12 divided by 2 so that is around 0.56, so, you see here. This is close to that one because this is for 13 doping so, it is around 0.6.

And you, as you increase the doping this Fermi level goes up and the difference actually increases. So, phi ms is increasing as the doping is increasing and because Fermi level is going up so, the difference the phi m and phi s difference is actually increasing and it is positive. So, as far as phi ms is concerned for p-type, p + poly n-type silicon it varies between 0.6 and 0.9 and with the doping it increases.

Similarly, we can see for again n-type, silicon with n + poly, so, in n + poly that means different colors. So, n + poly the Fermi level is somewhere here at the balance conduction bandage and now the value will be actually negative. So, when doping is small, this will be roughly the half of the band gap but the value will be negative, so, you see here for n + poly and n-type silicon.

This is around –0.4 so, it is slightly above the band gap and this is slightly above the band edge, so, this is –4 and as you increase the doping, this Fermi level goes up. So, the difference actually decreases. So, it decreases from –0.4 to somewhere around –0.1 because this phi ms is phi m – phi s. So, as a doping is increasing, the Fermi level is going up and phi s is decreasing.

So, for n-type silicon it will always basically increase. So, with respect to p + poly or n + poly, the only the point on y axis will change and as the doping increases this phi ms will basically increase. For p-type silicon it will have opposite trend because for p-type silicon the Fermi level is close to the balance band and as the doping increases, it goes down. So, this phi s actually increases.

So, this is basically decreasing for p-type silicon. So, this is p + poly p-type of silicon and you can also see let us say, p + poly will have around here and this is p-type silicon. So, this should also for high doping it should be close to 0. So, it is somewhere here and as doping is less this goes up and it is around 0.3. And you can change with aluminium also for aluminium 5 m is around 4.1.

So, for aluminium and n + poly will have similar characteristic, so, you see here, aluminium n + poly. Then aluminium and n + poly, they are very close the difference is around 0.05. So, this is a 5 ms relationship with the doping.

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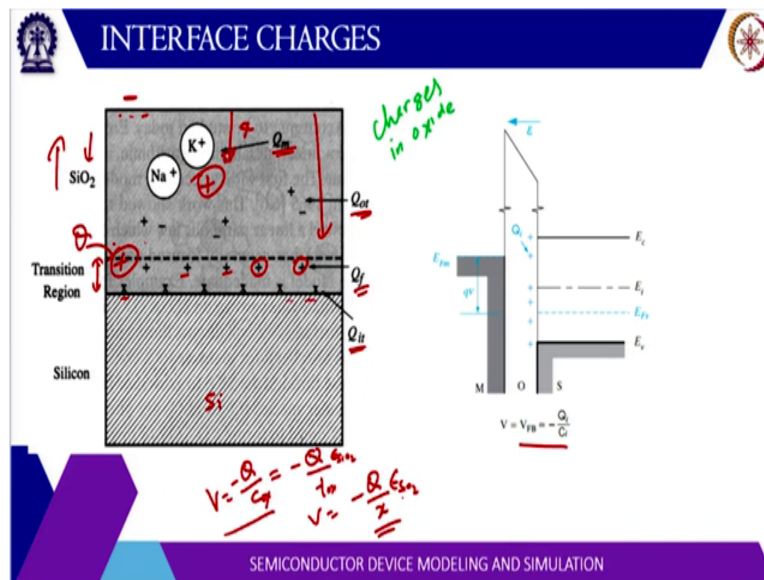

Now, the second effect is due to the interface charges or the charges in oxide. You can write charges in oxide. So, there are different charges that are found inside the oxide. So, if you see here this is silicon and then on top of the silicon, we are growing the silicon dioxide. So, it is possible that some of the bonds may not be properly connected in case of silicon dioxide, especially near the interface of the silicon and silicon dioxide there is a transition region.

So, there may be some fixed charges. Now, fixed charges they do not change or they do not move and usually these charges are positive charges. So, this is one type of charge that is found inside the oxide. Then there are mobile charges which can move around. These are generally the impurities of alkaline atoms, so, sodium carbon these are also positive ions. Now, when the field is such that is a field is up then these impurities will move in the direction of the field.

So, they will somehow try to accumulate here when the field is down, they will try to some come around here. So, these are the mobile charges but they do not move at room temperature or low temperature. So, they can be moved at high temperature or high electric fields. So, these are the mobile charges. Then there are oxide trap charges. So, there may be some energetic electron and holes they hit the interface and enter the oxide and get trapped.

So, these are the oxide trapped charges. Then there are interface trapped charges because of the interface of silicon and silicon dioxide. There are possibility of states and this state can have these charges. So, the charges hold by these states at the interface of silicon, silicon dioxide these are interface trapped charges. Now, how do they contribute? Less assume there is a layer of positive charge at the silicon dioxide interface, unless this charge is q.

So, what it will do? It will attract equal charge on the metal side. So and the potential difference will be if the capacitance of this region because this oxide is sandwiched between two conducting regions. So, the potential will be $Q = CV$ so, it will be Q by C. So, this is negative charge is accumulated on metal side. So, it should be minus Q by C on metal side and this is C oxide or C insulator.

So, this much voltage has to be applied on the metal side to revert back to the flat band voltage. So, this charge basically contribute Q by C. Now, if this charge is not at the interface, let us say it is somewhere here in the middle of the oxide then this variably modified. Because this Q by C if you see it –Q divided by C now C is what T oxide by epsilon, epsilon SiO_2 so, this is distance is T.

If this distance is some other let us say x then this V flat band will become – Q by x times epsilon SiO_2. And if it is distributed then of course we have to integrate this over x and calculate the flat band voltage. Because the contribution from charge at position x is this.

Then of course, if there is a charge at position x + dx then this will be Q by x + dx like this, so, the W integrated basically to find out the overall effect of this charge inside the oxide.

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INTERFACE CHARGES

Q_M= Mobile charges (Na+/K+) - can cause unstable threshold shifts - cleanliness has eliminated this issue

Q_{OT}= Oxide trapped charge - Can be anywhere In the oxide layer. Caused by broken Si-O bonds - caused by radiation damage e.g. alpha particles, plasma processes, hot carriers, EPROM

Q_F= Fixed oxide charge - positive charge layer near (~2μm) Caused by incomplete oxidation of Si atoms(dangling bonds) Does not change with applied voltage

Q_{IT}= Interface trapped charge. Similar in origin to Q_F but at interface. Can be pos, neg, or neutral. Traps e⁻ and h during device operation. Density of Q_{IT} and Q_F usually correlated-similar mechanisms. Cure is H anneal at the end of the process.

Oxide charges measured with C-V methods

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Now, mobile charges because they can move around. So, they make the threshold voltage unstable and this was the main reason that initially, most structure could not be realized because of these charges. So because the results were not predictable. So but due to development of the clean rooms this issue is more or less eliminated and it does not play a significant role.

So that means charge concentration is somehow below order of 10 is to power 10 and so on. Then their oxide trap charges, so, they can be anywhere inside oxide layer. So, usually, this silicon and oxygen bonds are broken by the energetic particles. So, they can be hot carriers or some particle alpha, gamma radiation and so on, due to plasma processes. So, this charges do develop during certain device processing operations.

Then there are fixed charges, they are very c-lose to the interface, usually within the toxicity micrometres around 2 micrometre of the interface charge layer. So, this interface charges they are at the interface of the silicon and silicon dioxide and typically within the 2 nanometre and caused by the incomplete oxidation of the silicon atoms. So, of course, it does not change with the applied voltage that is why they are called fixed charges.

And then interface trap charges there are also similar origin as a fixed charges but they are at the exactly the interface and they can be positive, negative or neutral. So, what happens?

There are interface states at the silicon and silicon dioxide and then these states can be occupied. So, let us say there is some neutral level somewhere here this we have already discussed for the interface state during the Fermi level pinning.

That if it is occupied up to the neutral level, so then Q IT is basically 0 if it is above then there are excess electrons there. And if it is below then there are less number of electrons then so, it becomes positive. So, it basically depends on where is the Fermi level line there and the density of these interface charges and the fixed charges they are somehow correlated because the mechanism is similar.

So, to get rid of this interface trap charges this interface has to be treated with hydrogen anneal at the end of the process so, it passivates the surface. And then of course, we can reduce the interface charges to a acceptable range. And these charges they are again measured with the CV method. So, because CV characteristic, the capacitance works versus the voltage characteristic depends on the charges.

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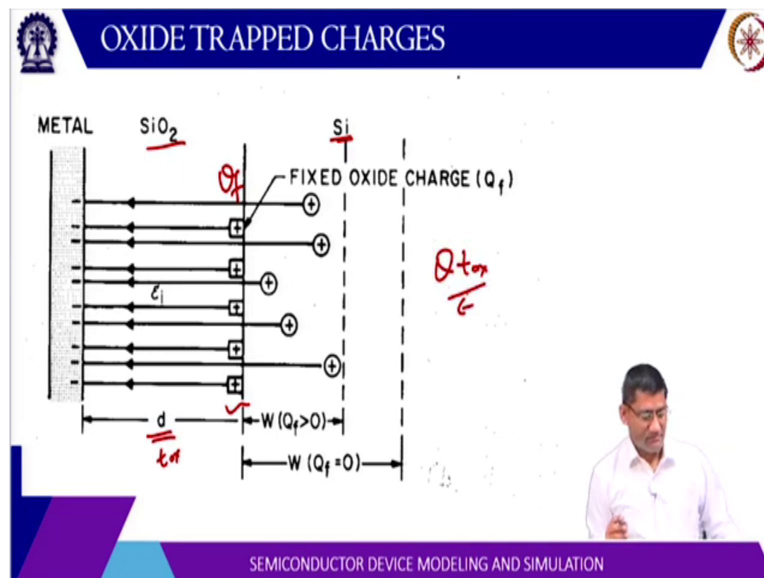

So, from the measurement we can extract out the information about these charges. Now, this is the picture basically shows this is the silicon here, this is a silicon dioxide here and there are fixed oxide charges here, Q f. Then they may be at certain distance at the interface and let us say this is the oxide thickness d. So, the field due to these charges will be Q by epsilon and then field times the distance is the voltage so, Q d by epsilon or t oxide, so, Q t oxide by epsilon.

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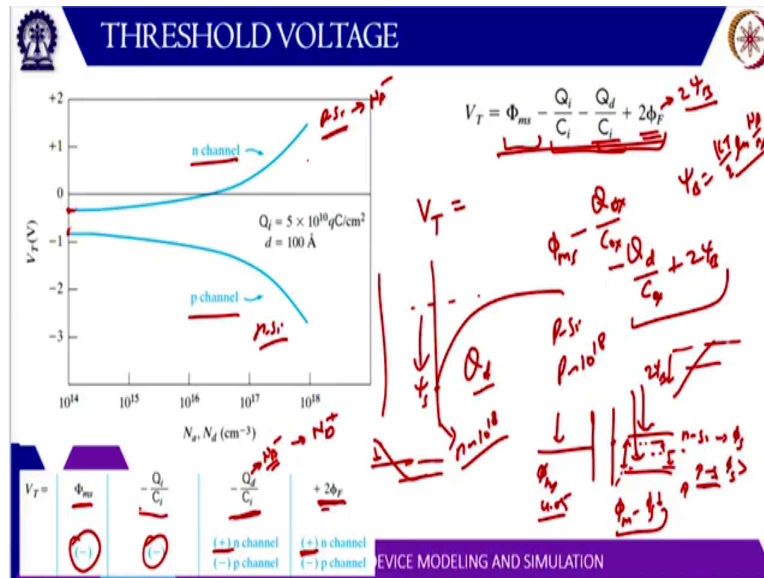

So, there is a pictorial presentation. Now, how these two factors affect the threshold voltage? We have already seen that the threshold voltage when these semiconductor and oxide they are ideal. It depends on the band bending inside the semiconductor. So, there is a depletion region here and there is some kind of band bending. So, this gives this surface potential. It is usually measured with respect to this bulk level.

So, this is 2 phi F or this you remember we saw this one as 2 psi B. Then there is a depletion charge here Q d so, for let us say, for n channel is the p-type silicon, so, there are acceptors here and a minus so, this Q will be negative. So, this will induce a positive charge on metal side, so, it was minus Q depletion by C oxide then plus 2 psi B. So, this was the threshold voltage.

Now and of course, we assume the flat band voltage was 0. Now, if we include these two effects, the Fermi level difference so then we have to add this is the Fermi level difference that is phi ms. So that is due to the Fermi level familiar difference then another is due to the charges at the interface, so that is Q I insulated charge divided by C I or C ox or you can write this as also Q ox by C ox. So, this is the overall expression for threshold voltage.

So, threshold voltage let us recall it is a voltage at which we adjust as the verge of creating the inversion region where the inverted carrier concentration is equal to the doping carrier concentration with different polarity. So, it is let us, say this is p-type silicon with whole concentration let us, say 10 is power 18. So, in case of inversion region, when the surface electron concentration is 10 is to power 18, we call that voltage as a threshold voltage.

Now, let us look at the polarity there are two types of doping, n channel and p channel, so, n channel means p-type silicon, p channel means n-type silicon. If you look at the band diagram, let us say this is phi m from vacuum to formula in the metal then inside the silicon, this phi s can be here for n-type silicon and for p-type silicon. So, if you notice the difference phi s for p-type silicon is more this phi s is more than phi s power n-type silicon.

So, phi ms will be less for p-type silicon because this phi s is more so, phi m – phi s will be less. So, you see so, for p-type you can you see this is a phi ms here and for n-type channel phi ms is little more. But in both the cases this is usually negative because this if you see for the metal so, in the slide that aluminium recall that aluminium it was 4.05. If you recall this one so, for aluminium is 4.1.

And for poly silicon or silicon, it will be between around 4 and 5. So, it is slightly actually negative. So, here it is between 4 and 5 so, phi m phi s lie between this band gap so which is more than 4. So, usually it is negative basically. Now, if you increase the doping then what will happen? For p-type silicon phi s is decreasing. So, your phi ms is increasing, so, doping does not change these parameters they may be slightly affected.

But this is the primary change, so, this actually increases the threshold voltage because phi s is decreasing. In case of n channel if you increase the doping, this will go for n-type silicon. So, if you increase the doping then phi s is actually decreasing. So, when phi s decreases phi ms phi m – phi s is decreasing, so, phi ms will actually increase so, this is one factor. Another factor is 2 psi B and minus Q d by C i.

Now, 2 psi B if you recall psi b is defined as the gap between the intrinsic level and the Fermi level. So, let us consider p-type silicon, so, this 2 psi B is basically psi B is KT by q log of N A by N i. So, this is also dependent on the dope in concentration and for p-type silicon this has to basically go down. So, if you look recall, this is the intrinsic level this is the Fermi level and this has to go down. So, this is your 2 psi B.

So, this potential is going down. So, if you see 2 psi B for n channel, this is positive, basically because potential the energy level going down. So, this is minus Q psi B so, the potential is basically increasing. So, for n channel this 2 psi B or 2 phi f is basically positive here. And

depletion charge is negative, so that is also contributing to point voltage so, – Q d by C i is also positive.

Because this depletion charge is composed of acceptance which have negative, so, this term will be positive, so, for n channel these two terms are positive and phi ms and Q inside the oxide by C ox or the insulator they both are negative, basically. So, for n channel this actually increases as we increase the doping. So, the factors that play into the picture phi ms it changes with the doping.

The depletion charge also change with the doping because this is still the N a concentration there is a doping concentration basically and phi f. So, these three play into the picture but the change due to phi ms is small. If you see this picture recall this picture, the change due to phi ms is quite a small. It goes from 0.6 to around 0.9. So, for this 10 is to power 13, 10 is to power 18.

And if you see here, this is going from some negative value to more than 1. So, it is not only the phi ms but these two factors also following the role. Then for p channel which is n-type silicon these both the terms are negative. Because now here you have donor ions so that is N d plus. And the bands have to bend like this in case of because Fermi level on top and this is the intrinsic level and it has to go up and cross the Fermi level.

So that means the energy going up that is the potential coming down. So, it should be negative, basically for p channel. So, both are negative for p channel and but phi ms and Q by C they are basically same. So, the difference in these two terms you see the difference because phi ms is also changing with the doping but that effect is small but this surface potential and the charge inside the semiconductor. They are giving rise to this kind of difference.

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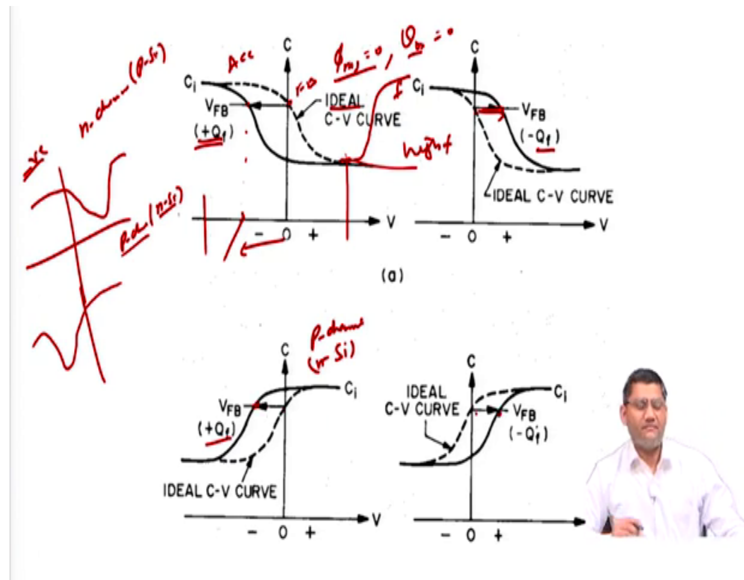

Now, when we measure the CV characteristic of a MOS structure, so, of course for ideal case when phi ms is 0 and the oxide charge is also 0 this what you will get. So, if you recall the whole thing this goes down then it goes up like this for low frequency and for high frequency you get like this high frequency. So, we only consider this region which is basically kind of accumulation and the flat band. So, this is accumulation this is a flat band.

Now, if you include the effect of phi ms and oxide charges then these both terms are negative. So, your V threshold will change from 0 to some negative value and that threshold voltage is basically have this information phi ms and the Q oxide by C ox. If this fixed charge is positive, if the fixed charge is negative then it will shift to the right let us assume that for timing, like phi ms is 0 only the fixed charge is there.

So, fixed charge is positive then it will shift to the right so, sorry when fixed charge is positive, it will shift to the left. When the fixed charge is negative, it will shift to the right because it is –Q by C so, –Q is now positive. So, this threshold voltage will be positive and that is for this was for n channel. For p channel if you recall this one CV characteristic so, for n channel the accumulation occurs at negative voltage. For p channel accumulation occurs at positive voltage.

Because p channel consists of n-type silicon n channel consists of p-type silicon, so, holes will accumulate for negative voltage. Electrons will accumulate for the positive voltage, so, this curve basically will be mirrored. So, it will be something like this accumulation so, this is for the bottom curve is actually for p channel, p channel means n-type silicon substrate. And

then of course, the fixed charge is positive it will shift to the negative value if fixed charge is negative it will shift to the right sides so, V T will become positive.

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INTERFACE TRAPPED CHARGES

- Surface states - R-G centers caused by disruption of lattice periodicity at surface
- Trap levels distributed in band gap, with Fermi-type distribution:

$$\frac{N_D^+}{N_D} = \frac{1}{1+g_D e^{-(E_F - E_D)/kT}}$$

- Ionization and polarity will depend on applied voltage (above or below Fermi level
- Frequency dependent capacitance due to surface recombination lifetime compared with measurement frequency
- Effect is to distort CV curve depending on frequency
- Can be passivated with H anneal - $10^{10}/cm^2$ in Si/SiO_2 system

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Then how these interface trap charges affect the CV characteristic. So, let us understand this interface charges, so, these are basically similar to the generation recombination centre. And they also some kind of follow Fermi direct distribution so and let us say for donor ions. What is the probability of a donor state being ionized? So, donor basically gives away one electron. So, if you recall the Fermi direct distribution, it is 1 over 1 + exponential E – E F by KT.

Now, here if you see it is n + so, this is which it is the absence of electron. So, it is basically hole, so, it should have 1 – F and 1 – F will have basically, instead of E – E F it will is E F – E. So, for donor atoms we have some kind of this degeneracy factor because as we discussed in present discussion that for a electron to occupy, it should be this format is E – E F so, it should be N D by N D+.

So, for electrons near the balance band so, there is this acceptor level now electron can come from two bands, the heavy hole and hole all and they can have either a spin. So, this degeneracy factor was 4 for donor level which is close to the conduction band. So, here the g D e level was 2 because of either spin. So, this g D will basically be 2 for donor atoms. Now, the ionization and the polarity will depend on the applied voltage.

So, whether this is above the Fermi level or below the Fermi level. So, if these are occupied above the Fermi level then this will be negative and if this is occupied below the Fermi level

then it will have positive charge net, So that basically gives rise to a frequency dependent capacitance. And the surface recombination lifetime affects the frequency dependent measurement.

And what it does basically? It will distort the CV characteristic depending on the frequency so, for high frequency it will take some time for this electron to rearrange. So and of course, at low frequency the time is enough so, the distortion will be more basically and these interface trap charges they can be passivated with hydrogen annealing in silicon dioxide system.

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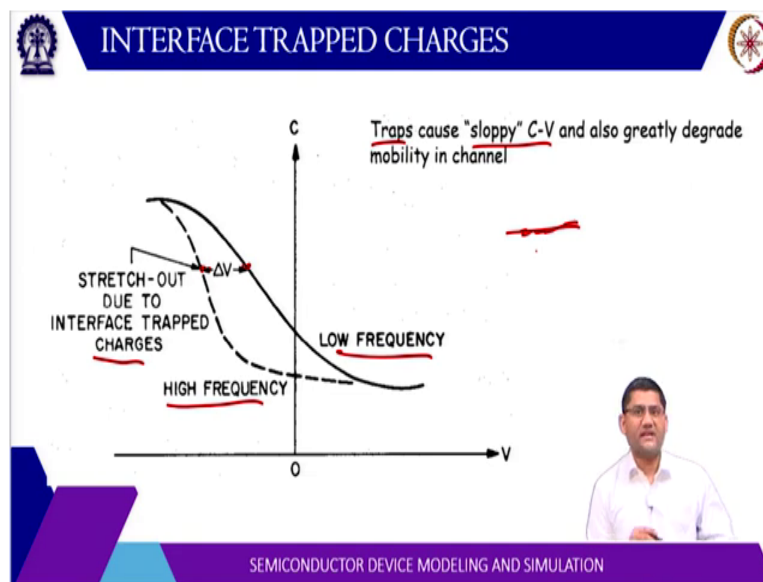

Now, if you see here for low frequency, it is more sloppy, so, the distortion is more for high frequency this is pretty fast. So, they do not follow up so, quickly. So, if you compare this low frequency and high frequency CV characteristic, there is some difference here. And this difference of the flat band voltage is due to this interface trapped charges. So, this drop these interface traps, they cause sloppy CV characteristic.

And they of course, also degrade the mobility of the carriers in the channel. Because this charge is present at the interface, they will give some kind of coulombic scattering to the carriers moving inside the channel.

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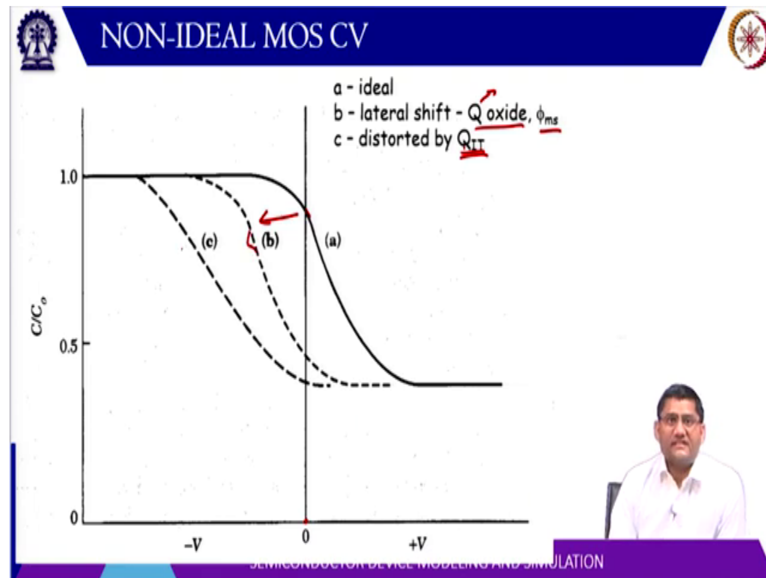

Now, this is the summary basically for known, ideal CV so, for ideal where phi ms is 0, there are no charges. So, this is the flat band voltage which is 0. Then if there is an oxide and there is phi ms so, if there is a positive charge and phi ms non-zero, this will shift to the left. And if you include these interface trap charges then instead of being the slope get actually changed. So, it slowly changes here because with the probability of filling these interface trapped states.

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NON-IDEAL MOS CV

- Work function difference and oxide charges shift CV curve in voltage from ideal case
- CV shift changes threshold voltage
- Mobile ionic charges can change threshold voltage as a function of time - reliability problems
- Interface Trapped Charge distorts CV curve - frequency dependent capacitance
- Interface state density can be reduced by H annealing in Si-SiO_2
- Other gate insulator materials tend to have much higher interface state den

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So, the work function difference and the oxide charges they shift the CV curve in the voltage compared to the ideal case and there is a shift of the threshold voltage. Now, this mobile ionic charges they pose some kind of reliability problem. Because sometimes they may be close to the silicon interface, sometime they may be close to the metal or the gate interface. So, according to the threshold voltage will change.

And compared to the mobile charges, these interface charges they distort the CV curve. So, the frequency dependent capacitance becomes more sloppy. And other gate insulator, so, other gate insulator means other than silicon dioxide they tend to have much higher interface state densities. So, this is the one reason why silicon, silicon dioxide combination is so, popular.

Because here you can have very less number of these interval trap states and the known idealities and the charges in the oxide.

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NON-IDEAL MOS CV

- For the three types of oxide charges the CV curve is shifted by the voltage on the capacitor Q/C

$$V_{FB\text{-}oxide_charge} = \frac{-1}{C_i}\left[\frac{1}{d}\int_0^d x\rho(x)dx\right]$$

- When work function differences and oxide charges are present, the flat band voltage shift is:

$$V_{FB} = \phi_{ms} - \frac{Q_{eff}}{C_i}$$

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So, if the charge is distributed then if you recall that V = Q by C and C is basically epsilon by t, so that is per unit area. So now, what can be done here? We can write t times Q by epsilon. So, this can be written as t times Q can be written as integral x rho dx. So, what we are doing basically? That say this is your metal interface and this is oxide and if you consider resistance x and let us say there is a charge dQ.

So, let us say distance x from the metal there is a dQ charge so, due to this, the capacitance will be or voltage will be dQ times x by epsilon. And when we integrate over whole range, so, dQ can be written as rho is, let us say the density times dx. Because now we are having this 2 times x so, we have to integrate the numerator by rho dx times x at denominator by dx and 0 to d here, 0 to d here. So that is how we have got.

So, if you integrate dx from 0 to d you get d in the denominator and x rho dx in the numerator times 1 by C so that becomes your flat band voltage so, this is due to the distributed oxide charge. So, what we can see? We can represent this expression on the bracket as Q effective, so, Q effective is not the actual charge but what is the net effect? Assuming that there is a effective charge at the silicon, silicon dioxide interface.

So, this distributed charge is represented by a q effective charge at the silicon, silicon dioxide interface, so, assuming at the distance d. So, this is a flat band expression for the distributed charge where Q factor is given by this term under the bracket.

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BIAS-TEMPERATURE STRESS TEST

Used to determine mobile charge density in MOS dielectric (units: C/cm²)

Na⁺ located at lower SiO_2 interface → reduces V_{FB}

ΔV_{FB}

Na⁺ located at upper SiO_2 interface → no effect on V_{FB}

Positive oxide charge shifts the flatband voltage in the negative direction:

$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_{ox}} - \frac{1}{\varepsilon_{SiO_2}} \int_0^{t_{ox}} x\rho_{ox}(x)dx - \frac{Q_{IT}(\psi_s)}{C_{ox}}$$

$$Q_M = -C_{ox}\Delta V_{FB}$$

SEMICONDUCTOR DEVICE MODELING AND SIMULATION

Now, how do we measure the effect of these mobile charges? So, for that there is a technical bias temperature stress test, so, what we do? Let us see this is your metal. This is a silicon dioxide. This is silicon. So, let us say we apply a high field that is a positive charge here at high temperature. So, what will happen? This will push away the carriers. So, these all these positive charge will be pushed to this region.

So, their contribution will be minus Q M by C ox. Then let us say again we at elevated temperature we apply a negative potential here. So then all this positive charge will come here. Now, their distance is 0, so, their contribution will be 0. So, when you measure the CV, the threshold voltage in case of in the first case will be shifted by minus Q M by C ox. So, this delta flat band will basically will be minus Q M by C ox.

So now, so, if you look at the expressions of flat band voltage, phi MS is constant Q fixed charge is same this is due to the distributed charges and this is due to the interface trap charges. Then here again, you can write for one branch for the second case it will Q M will be 0 and Q M by C ox because they are at the interface here. So, they will not contribute any shift in the threshold voltage for first continuity minus Q M by C ox.

So, if you take the difference of two flat band voltage, so, this will, let us say V FB V 1 let us say this is V FB V 2. So, the difference of V FB 1 and V FB 2 is delta FB V FB = –Q M C ox. So, Q M the mobile charges can be calculated from the bias temperature stress test finding the difference between the two flat band voltage and multiplying by the oxide capacitance which is a physical parameter. And we know this is epsilon by t ox.

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So, in conclusion we have discussed that for a MOS structure the factors that play the role, so, this is a metal semiconductor interface, metal semiconductor work function difference. Then there is a contribution due to oxide charges and then the band bending and then due to the depletion charges. So, overall expression is basically V T = phi ms + 2 psi B so, psi B is basically the difference between the intrinsic level and the Fermi level for a non-disturbed, semiconductor side.

Then this is due to the depletion charge and then Q factor is the oxide charge by C ox. And we also found out in earlier lecture that the charge the inversion charge. So, this is V T here so, inversion charge is linearly proportional after V T. So, this is C ox times V G – V T with a negative sign here for n channel. Thank you very much.