Semiconductor Device Modelling and Simulation
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Lecture – 25
Metal- Semiconductor Interface

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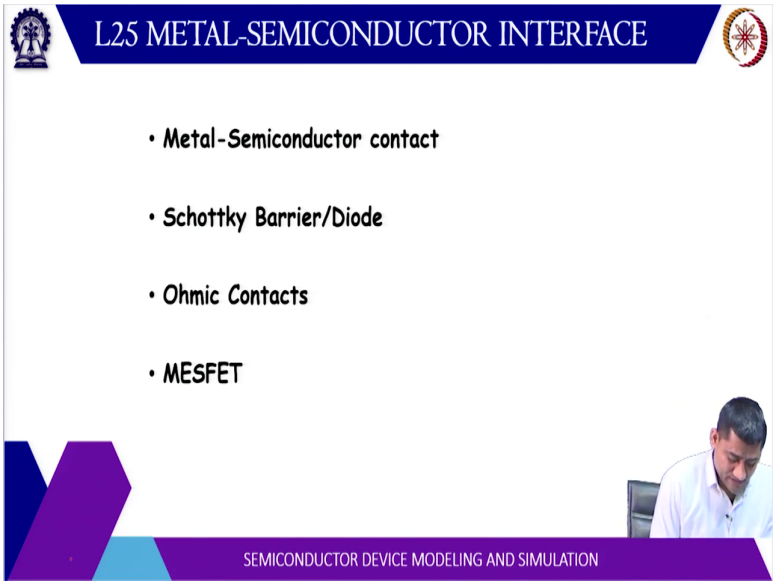

Hello, welcome to lecture number 25. So, in this lecture we will discuss the metal semiconductor interface. So, metal semiconductor contact or one of the important parameters one of the important contacts because metal semiconductor contact can be rectifying like a diode. So, that we call it short key diode or short key barrier they are usually fast and majority carrier based device.

But even for a p N Junction diode if you want to use it we have to apply a voltage and that has to be done through a metal contact. So, as soon as you attach a metal there is a possibility that this metal semiconductor contact may be rectifying. So, we would like to also know how can we make these metal semiconductor contactors ohmic contact. Ohmic contacts are those contacts where I versus V is linear.

That means whether you apply a political voltage or you apply a negative voltage it does not discriminate it gives you the same current on the contrary the short key diodes or rectifying contacts they behave differently. So, when you apply certain polarity of the voltage no current

will flow when you apply other political voltage some other current will flow. So, such contacts are called rectifying contact.

And these are called ohmicond then we will also briefly discussed what are these metal semiconductor field effect transistor.

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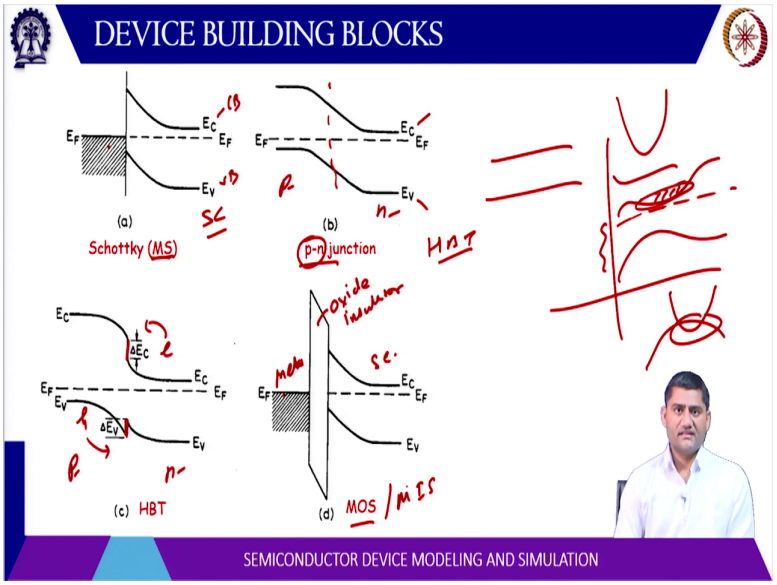

So, these are the four device building blocks are shown here one is short key that is metal semiconductor contact. So, in case of semiconductor we have this band structure there is a conduction band there is a valence band and there is certain Fermi level and when we connect it with a metal, metal does not have this kind of band structure or a metal is basically characterized by a filled state. So, even if there is a some band like this.

So, what is there in metal let me show it here let us say this is the band diagram or this is let us say the band structure or if you recall from the lectures we discussed in the beginning a band structure may look like this you know. So, some different this thing so this is basically a bandgap but then this is filled. So, in case of semiconductor the Fermi level lies somewhere here in the bandgap region.

So, these bands are not fully filled but in case of metal these Fermi levels lies somewhere in the band. So, this band is actually filled. So, this top band which is filled contributes towards the conduction. So, instead of showing a band structure here because there is a band which is fully filled or it is possible that the conduction band and the balance band they may be overlapping. So, there is no bandgap as such.

So, in case of metal we simply specify the Fermi level and of course when in equilibrium when these are connected this Fermi level will unite. So, this Fermi level will have same it will be constant across the two materials and when they it unites there may be some band bending but that band bending is only on the semiconductor side not on the metal side. So, this is one device building block.

Another device building block is a p N Junction which we have already discussed where there are two types of semiconductor this is p type semiconductor this is N type semiconductor and when they are connected together there is some kind of band bending. But we see here the conduction band E C and the balance band E V they are continuous there is no break or there is no discontinuity. Had it been a different material as we discussed in HBT you can recall.

So, in HBT the material or this p type semiconductor and N type semiconductor they are different materials. So, their bandgap is different. So, therefore there is a discontinuity of the interface. So, this is Delta E C this is Delta E V and this gives advantage to one type of carrier. So, in this case these holes will have a smaller barrier compared to the electrons here then another building block we will discuss will be metal oxide semiconductor.

So, in short key metal and semi conductor are directly in touch they are directly connected to each other in case of MOSS the metal and semiconductor they are separated by a small oxide layer. Now this oxide is a insulator. So, be a metal we have insulator and we have semiconductor. It is also called metal insulator semiconductor junction or MIS structure. So, these are the various building blocks that we will go one by one.

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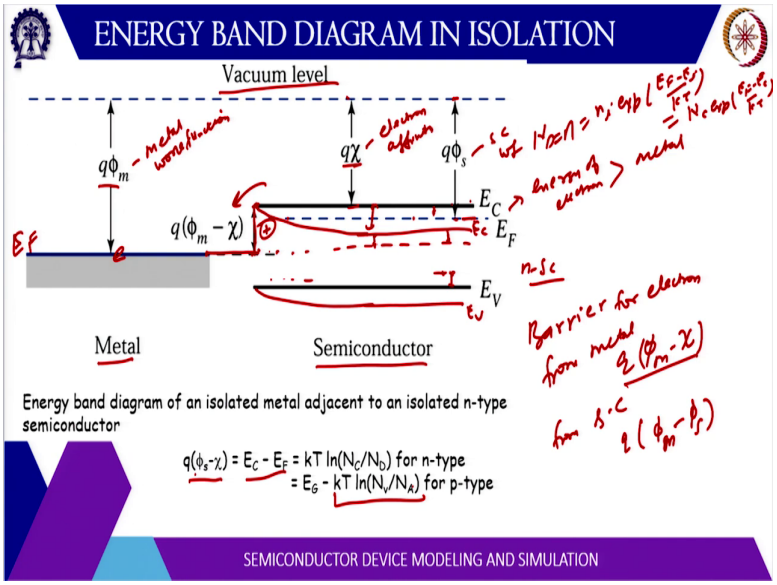

Now as I discussed in the beginning also that for a device engineer it is very important to the draw the band diagram because this band diagram will tell you about thE Conduction properties of that structure. So, now let us look at the two materials metal and semiconductor. So, this is the Fermi level in the metal E F and this is vacuum level. So, vacuum level is basically ideally a place which is infinitely away where the potential is zero.

So, when electron leaves this region and goes away at rest so, that energy required is a work function that is represented by q Phi m. So, this is called metal work function. Similarly in case of semiconductor you can also define the difference between the vacuum level and the Fermi level in semiconductor is semiconductor work function. And the difference between the vacuum level and the conduction band in semiconductor is called this q Chi this is electron affinity of that semiconductor.

And the difference between the Fermi level in the metal and the conduction band in the semiconductor is the difference of these two parameters q Phi m minus q Chi. So, this is q Phi m minus q Chi this is the difference and that is basically constant. If you notice in the previous diagram this will be constant it is not going to change. So, what will happen now they are in isolation when they will come together this Fermi level will be aligned. So, Fermi level and E C gap is fixed.

So, E C will be somewhere here and by same amount E V will also come down and then at the interface it has to aligned properly with this one. So, this is how the band diagram will look like inside the metal this, this is a semiconductor and that is an equilibrium because

Fermi level is constant now and this will be your E C this will be your E V. Now how that is happening because the Fermi level in case of semiconductor is above.

So, that means Fermi level is above is here energy of electron is more than the metal. So, that means electron will flow from high energy to low energy. So, this electron will actually move here. So, what is remaining here is the positive ions. So, this electron will move to the metal and point one will be exposed here. So, you see here the amount of carry concentration it is same as the original n-type semiconductor. Here the difference between the conduction band and the Fermi level is large that means number of carriers is less.

So, that means they have moved away. So, what is exposed there is the donor ions another thing you can note here the barrier seen from the metal side. So, the barrier from metal side barrier for electron from metal side is q Phi m minus Chi and from semiconductor side this is the very right. So, this is smaller than the barrier from metal side. So, this is your q this is Phi s. So, this is Phi s minus Phi m, Phi s is less basically.

So, you have to subtract Phi m minus Phi s Phi m minus Phi s because Phi m is large Phi s is small or you can say the barrier minus this gap E C minus E F. So, this barrier minus E C minus E F or you can write q Phi s minus Chi. So, Phi s is basically level of this Fermi level the distance between the difference between the vacuum level and Fermi level and q Chi is vacuum level and thE Conduction band.

So, this is the difference q Phi minus Phi s minus Chi which is E C minus E F and that is related to the doping you recall the expression we wrote two expressions m that N is equal to N i exponential E F minus E I by kT that was one another we wrote was N C exponential E F minus E C by kT. So, if you use this expression. So, E C minus E F you can find from here that is kT by k t log N by N C and N is equal to this is the doping concentration N D.

So, this N C by N D kT log N c by N D is E C minus E F or in case of P type we will calculate this Gap E F minus E B. So, that will be that will be kT log N V by N A. So, E C minus if you take that Gap that will give you E C minus E F so, either way you can use.

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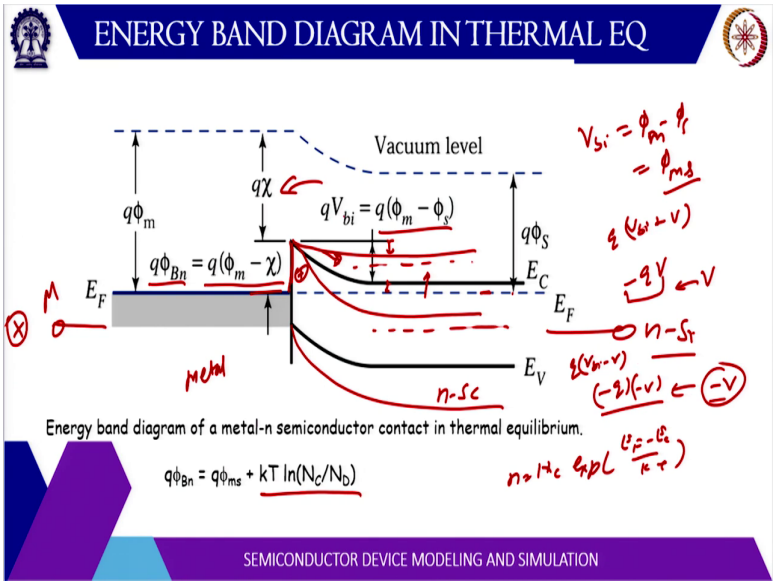

Now when we connect them together the band structure will look like this. So, this is n-type semiconductor and this is metal. So, q Phi m minus Chi is the barrier for the metal and we call it q Phi B N. So, this is one of the characteristic parameter of any metal semiconductor junction and the built building potential from the semiconductor size is q Phi m minus Phi s is also called q V VI. So, you can find from V BI from here V BI is Phi m minus Phi s this also called Phi m s and if you relate the two five b N with V BI.

So, q Phi b N is q V BI plus this small Gap E C minus E F and that is case t log N C by N D that is again obtained from the expression N is equal to N C exponential E F minus E C by kT. Now what has happened because these electrons are migrated to the metal side a point of charge is x Plus exposed here the positive fixed ions. So, this fixed ions basically oppose the further movement of electron.

So, the field is such that this will push the electron away from the junction. So, this is very similar to the phenomena that we observed in p-n Junction diode due to diffusion carriers or electron move from N side to P side which causes a field to build up which opposes the further diffusion. So, same thing is happening here these electrons diffuse to the metal side then these poetic charges are exposed here and which further restrict the further movement of these electrons to a metal side.

So, they create a field which creates a counter current from the electric field or counter drift current to counter the diffusion of the electrons now what will happen when we apply the bias because this barrier is fixed. So, by applying the bias we only vary this band structure on the

side of the semiconductor let us say this is your metal this is your n-type semiconductor now if we apply a positive bias here what will happen positive bias means energy is minus q times V this is a this bends are basically elect energies of the electron so, minus q times V. So, positive is means this energy will actually decrease.

So, what will happen this E F will go down. So, this will be E F in metal let us say this is the E F N semiconductor. So, this will basically. So, now barrier is increased. So, barrier will be q times V BI plus V applied a bigger vary is there. So, what will happen the electron that could have moved from N type semiconductor to metal will reduce. So, less number of electrons can move from semiconductor metal but the electron that can move from the metal to semiconductor is still the same.

So, it will reduce the current basically because this barrier is quite large and this barrier is even further increased. Now you consider different situation where you apply a negative voltage to this one two semiconductor side or you apply a positive voltage to the metal the negative voltage here means energy is minus q times minus V. So, this is a positive energy. So, this Fermi level will go up. So, now Fermi level is somewhere here and the barrier is like this. So, now barrier is reduced.

So, barrier is q times V BI minus V. So, that means now this electron can move from the N type semiconductor to metal. So, that means a large current can flow. So, in this case in case of metal semiconductor the forward bias is that metal is positive and N tap semiconductor is negative so that means electron can easily move from semigrade metal. So, current will flow like this from metal to semiconductor.

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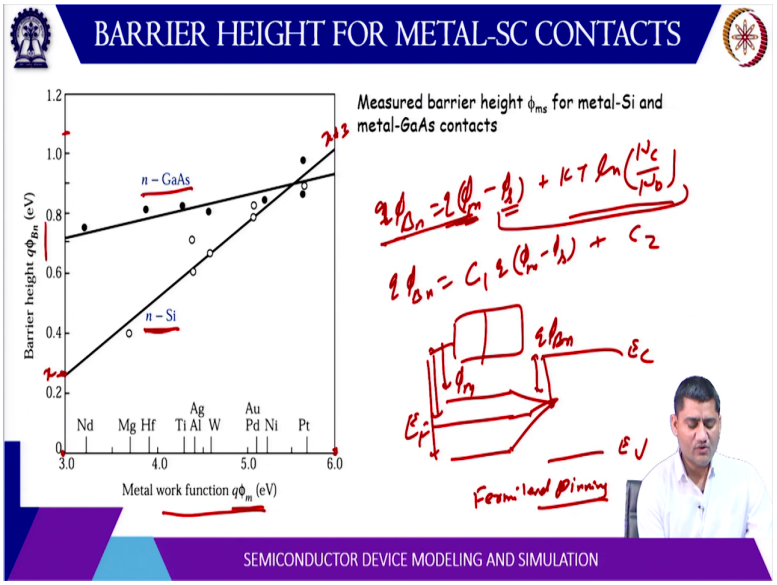

Now this is basically q Phi V N you have seen here this is q Phi V N if you look at the expression q Phi V N this is q Phi m s Plus k t log N C by N D. So, it is dependent on the metal semiconductor work function difference and the doping in case of semiconductor. So, this diagram actually shows this barrier height versus the metal work function Phi m for let us say right now through silicon. So, now doping is same. So, your q Phi b N is equal to Phi m s i m minus Phi s plus kT log N C by N S.

So, it is enter silicon it is let us say same entire silicon for all of them. So, this term is constant. So, your Phi b N should have been should have varied linearly with the work function of the semiconductor and Bug function of the metal. So, on the x axis we have plotted the work function of the metal. So, your q Phi b N is Phi m then some constant basically. So, this should have been linear basically as the Phi m increase q phi V N will also increase by the same number.

So, this should be q here yes q here ok. So, q Phi V N is q Phi M minus q Phi S Plus kT log N C by N D. So, if phi m changes by from three to six your Phi V should also change from a number certain number let us say x to X plus three but if you notice here the change is quite a small it is changing from point to something to one something this is for silica. So, that means your q Phi V N is not equal to q Phi m minus Phi s but some coefficient C times Phi m minus Phi s and there will be some other copy centers a C 1 plus C 2.

Now the reason for this we will discuss shortly. So, before that let us understand this curve is here basically. So, that means we cannot just from the material we cannot tell what will be the

barrier height. Barrier height is usually obtained experimentally. So, once you make a metal semiconductor contact you measure the current characteristic and then you can estimate the barrier height another thing you can notice here the slope is different for silicon and the gallium arsenide for gallium acid is almost constant.

So, as if this barrier height is not changing. So, if you look at the semiconductor it has some bandage structure right. So, this is E V and this is easy and for metal this is a Fermi level in the metal. So, it appears that when you change the metal Fermi level whether it is here or here. So, this is Phi m right. So, it can be here it can be here but it is somehow hinging to certain point in the bandgap year either this or this or this.

So, that your Phi V N is constant this height is q Phi V N and this phenomena is called Fermi level pinning. So, this very right are measured experimentally and they are tabulated like this where the in at least in this diagram the barrier it is shown as a function of metal work function. So, how it varies with the metal work function it the variation is almost linear but the slopes are different for different material that means the permeable pinning phenomena is more severe in gallium arsenide than silicon.

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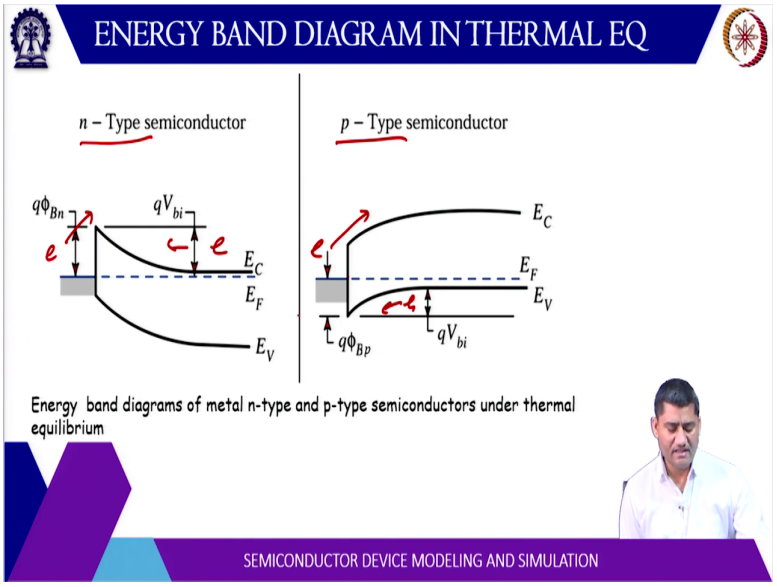

Now these are the band diagrams in thermal equilibrium for entire semiconductor and Peter semiconductor. So, for N type this conduction wind is close to the Fermi level so the band diagram will look like this. So, here you see there is a barrier for electrons created in case of P type semiconductor Fermi level is close to the valence band. So, the bands actually band

like this. So, they are pulled up the Fermi level is pulled up and it aligns and this band is also pulled up.

So, you see for the holes there is a barrier created here of course for electron also there is a barrier here electron also there is a barrier here for holes there is a barrier here from the P type semiconductor site.

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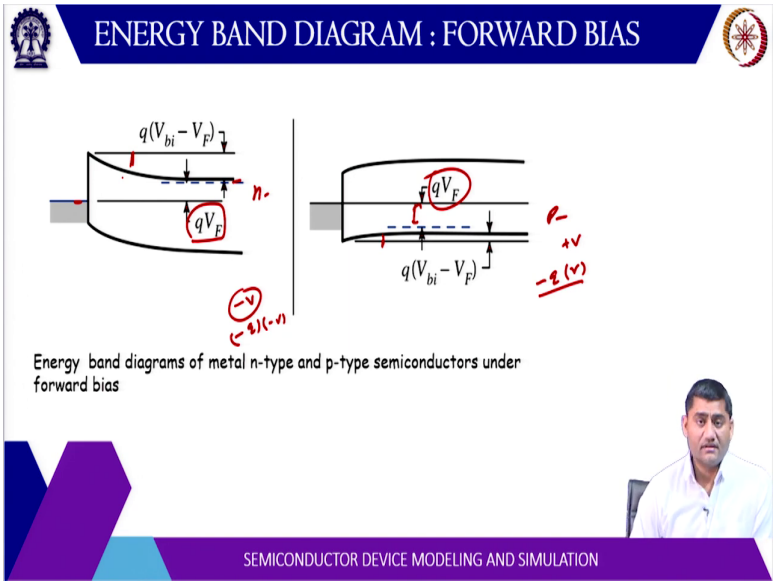

Then of course when you apply the bias these both will change basically. So, this is for again N type and this is for P type. So, this is forward bias. So, forward wise basically if we apply a negative voltage here. So, that means minus q times minus V. So, that means energy will go up so Fermi energy has now increased. So, this is the difference between the metal Fermi level and the semiconductor Fermi level is q V applied.

And in this case the forward bias will be you apply a poetic voltage. So, then energy is minus q times plus V. So, this will decrease by this q V amount. So, this is q V applied the Fermi level is and then accordingly the barrier height is reduced barrier for this electrons and holes in the P type is reduced.

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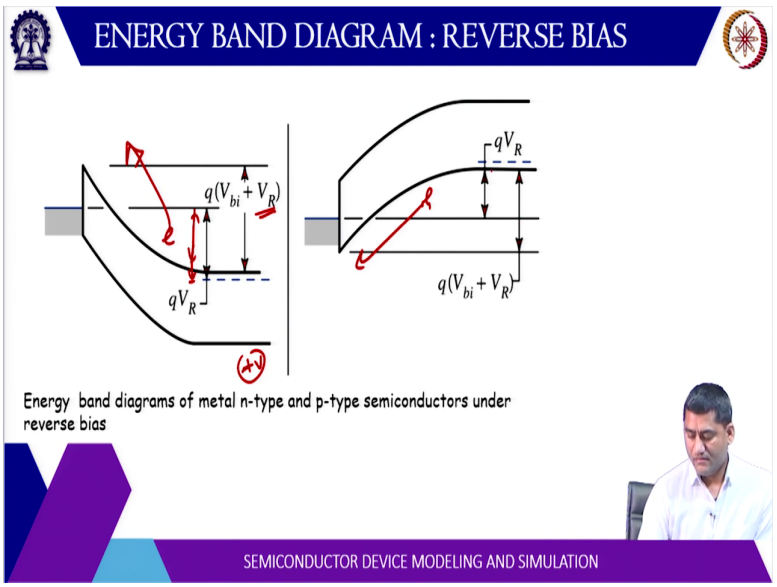

In reverse bias these various increases. So, here we have applied a positive voltage here. So, Fermi level is minus q V down. So, this is the gap V R. So, this is q V R basically up to here. So, this barrier for electrons is further increased similarly for here the barrier for also is further increased and this is q V R up to here this is the Fermi level here this is the Fermi level here. So, this is q V R reverse bias.

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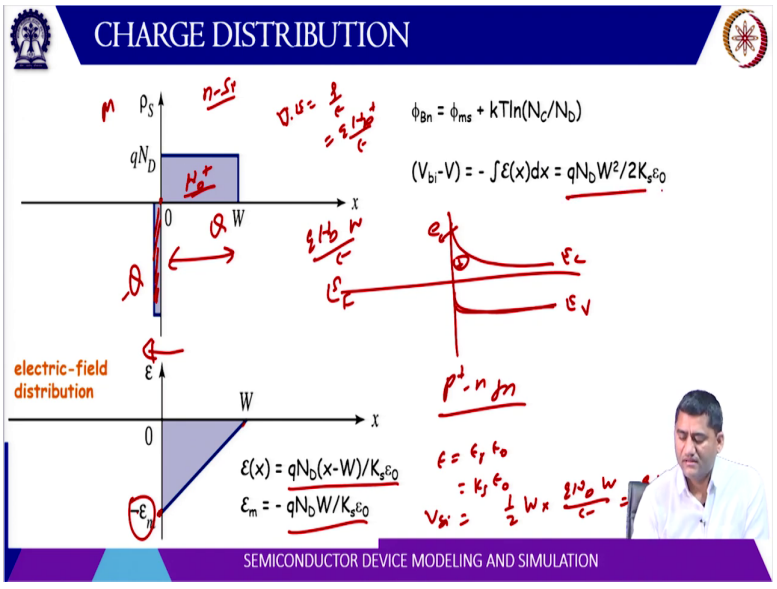

Now this is for this is N D Plus. So, this is metal and this is N type semiconductor. So, if you recall the band structure this is the Fermi level and this is e v this is E C. So, this is the band diagram you have seen and we said that because the formula was above in case of N type semiconductor. So, electrons would have moved to the metal side exposing the donor ions here. So, this is the donor ions N D plus is a charge density when this electron moved to the metal side they cannot move inside because these metal is very large three electron pool.

So, you cannot have any electric field inside the metal. So, all these carriers actually accumulated the interface of metal and semiconductor. So, the total charge here let us say this is q it will be minus q here. So, all the electrons are accumulated of the metal semiconductor interface they form a thin layer thin seed and this depletion to counter that negative charge there is a depletion charge in case of semiconductor region and this you see it is very similar to the one side of the PN Junction.

And in fact you can compare with P plus n Junction. So, when it is highly doped. So, on the P side we have this very small thickness of the depletion region but here it is zero in case of metal then mostly the depletion region falls across the low doped side. So, which is a N type semiconductor here. But then based on this charge profile again we have this depletion approximation.

Because of this constant charge profile the electric field will be linear because if you recall the Gauss law Del dot E is equal to rho by Epsilon. So, rho is q N D by Epsilon. So, your electric field is q N D by Epsilon times x. So, as you vary the x this increases. So, you can write q and d x minus W by Epsilon. So, Epsilon is basically Epsilon R times Epsilon naught Epsilon R is a dielectric constant sometime written as k s also.

So, k s means dialectic constant for semiconductor and of course the maximum will be at the interface and again the minus sign is because of the direction because direction is from plus x to minus x. So, electric field is in the minus x Direction. So, this minus is shown here and maximum will be at the metallurgical Junction. So, this width is W. So, the maximum is q N D W by Epsilon so, q N D W by Epsilon.

So, there is a maximum electric field and of course you want to find the barrier right then you take the area basically of this electric field. So, that is half E M times W. So, that will be the built-in potential will be half W Times E M that is q N D W by Epsilon. So, that is basically q N D W Square by 2 Epsilon; q N D W square by 2 Epsilon. So, that will be the barrier height and of course when V applied a zero this barrier is same as V BI.

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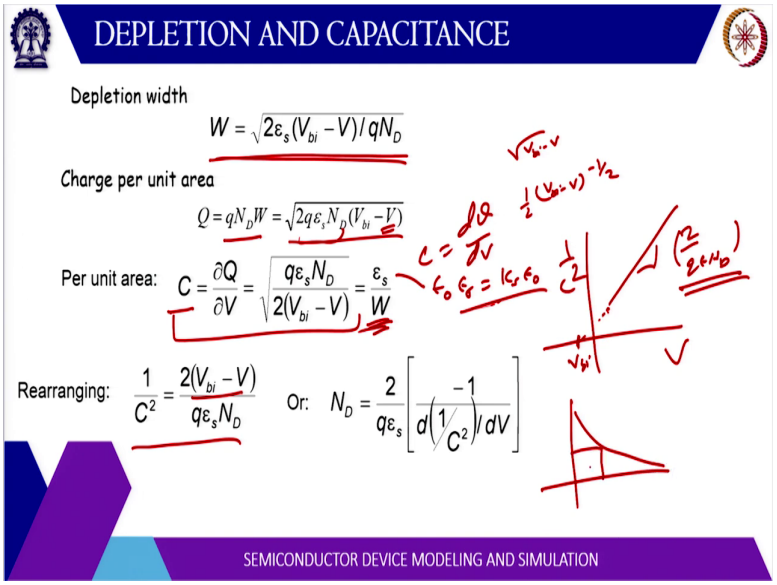

Then we can borrow the expression from the P N Junction the expression for depletion width for one side a junction. So, that you can directly write q Epsilon V Bi minus V by q N D and of course charge per unit area is q and d times w. So, this is the expression and then you can calculate the cap stance that is dq by dV. So, if you differentiate with respect to V. So, this is square root of V. So, it will come as one over square root of V. So, this is the constant. So, V BI minus V power half.

So, it will be square root of V BI minus V the derivative will be half V BI minus V power minus up. So, this two and two will cancel out. So, we have one by root two. So, and this you can rearrange and find that this is Epsilon by w. So, this is a common practice if you find out the depletion with W which is a function of a square root of voltage we generally express the cap stances Epsilon by W.

So, here Epsilon is Epsilon naught times Epsilon R or k s times Epsilon naught and then of course if you rearrange this thing you take one by C Square. So, one by C square is proportional to V BI minus V. So, from this equation we can find out that if we plot one by C Square versus voltage this one by C Square will go to zero at V equal to V BI. So, this is basically a straight line which will intersect at some point which will equal to V BI and the slope of that curve is basically two by q Epsilon N D.

So, the slope will basically give the doping profile. Now if this doping is uniform doping then this slope will be constant because if you see here it is somehow going like this. So, if the doping is uniform then the charge profile is also uniform or constant basically so this is N D

plus but if doping is not uniform then this charge profile will change and then this one by C Square Bar says V will also not be linear.

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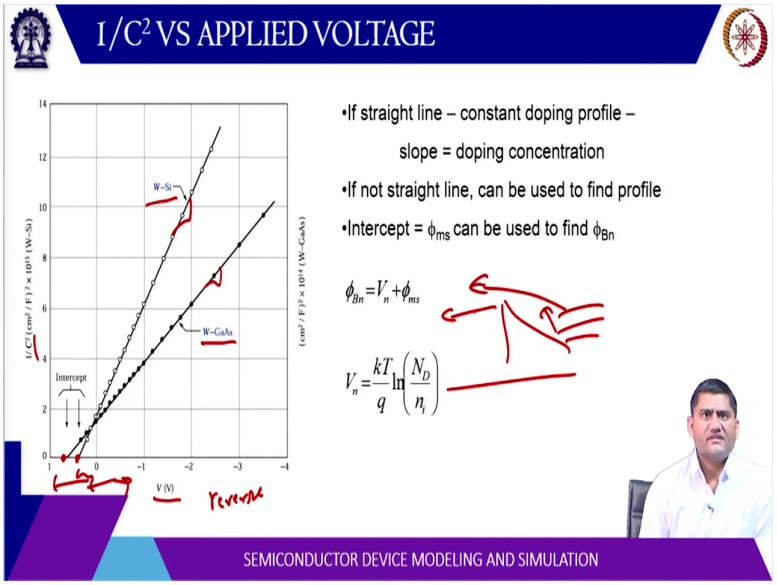

So, you can see here this is a curve this is tungsten silicon one by C Square versus applied voltage and this is tungsten gallium arsenide. So, if you take the slope of these two lines this is one by C Square versus V. So, the slope will give you the doping concentration and if you extend this line further this will tell you the built-in potential. So, built-in potential for Tungsten silicon is some number may be around point three or point four and then for Tungsten gallium side it should be around 0.6 or 0.7.

So, this is on higher voltage now this built-in voltage always on the opposite side because if you go to just say this is this side will be reverse bias because this is there was bias capacitors in forward bias the current will actually flow. So, this depletion cap stance will be small basically because now the depletion width is small. So, you will have another capital diffusion cap stance.

But in case of metal semiconductor it is a majority carrier dominated device in p-n Junction you have this diffusion coefficient because this magnetic array diffuses to the other side here generally this kind of device they are faster because it is the majority carriers only. So, once these electron cross over this barrier because it requires certain velocity for them because not all the electrons can cross over the barrier only the energetic electrons can cross over this barrier. So, once they cross the barrier we continue with the same speed. So, the speed of electron is also fast. So, these devices are faster.

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So, in this lecture we have discussed the metal semiconductor contact their band diagram and their cap stands characteristic, thank you very much.