Semiconductor Device Modelling and Simulation
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Lecture – 02
Introduction (Contd.,)

Dear students welcome to the second lecture of NPTEL online certification course, semiconductor device modelling and simulation. So, we will continue our introduction.

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In last class we discussed about the development of integrated circuit and the associated devices scaling that is continuing till now and we also discuss different stages of scaling and introduced why silicon is one of the most important semiconductor in today's world. Now, we will further continue our discussion, we have seen that silicon based devices especially the MOSFET. They are entering a regime where the dimensions are very small they are order of few nanometers and such devices are called nanoscale devices. So, in today's lecture, we will cover the concepts related to the nanoscale devices as well as the heterostructure devices.

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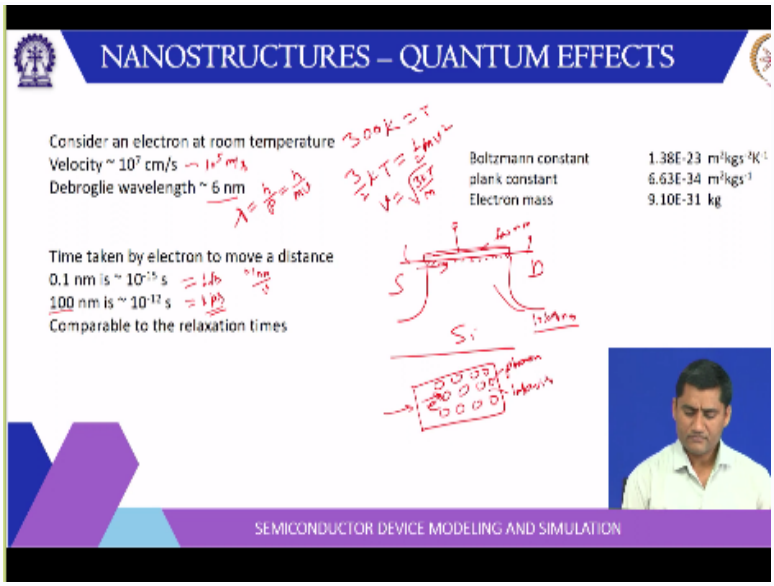

To understand the concept of nanostructured devices, let us consider an electron at room temperature which is 300 kelvin. 300 kelvin is a room temperature at this temperature, if you consider an electron so there is ensemble of electron. So, they are average kinetic energy will be 3 by 2 K T, where K is the Boltzmann constant and T is the temperature and the value of Boltzmann constant is 1.38 into 10 is to power -23 meters square kilogram per second square per kelvin.

So, the different constant we will encounter in our course, so those values of course, I will list here that, because this tells you the average kinetic energy then you can equated to half mV square and that will give you the velocity is around 3K T by m where m is the mass of electron which is around 9.1 into 10 is to power -31 kg and when you evaluate it, you get a velocity of 10 is to power 7 centimeter per second or you can write 10 is to power 5 meter per second.

Then in around 1924 Debroglie said that a particle can exhibit of the wave nature or this concept of wave particle duality came into the light. So, there is a relationship between the wavelength of a particle and this momentum. So, wavelength of a particle is given by h by p, p is the momentum. So, for electron you can write h by mV. So, where h is the Planck constant the value is 6.63 into 10 is to power -34 meter square kilogram per second and if you evaluate it, you get around 6 nanometers. So, this is the wavelength of electron at room temperature.

So, if you consider a nanostructure device and especially the modern MOSFET their dimensions are close to this region if you consider simple MOSFET a structure. So, this is less your silicon substrate, then there is a source here, there is a drain here, there is a thin oxide layer here and then there is a metal contact or polysilicon and then it is connected to a gate terminal and when we apply a voltage here, some channel is created here. And once channel is created here, channel of carriers then current can flow through this channel between source and drain.

Now, for nanostructure devices, this oxide thickness is order of few nanometers this gate length is few 10s of nanometers. So, some important phenomena will appear here when these electrons move through this channel or for that matter through any semiconductor they go through scattering. So, these scattering are due to the lattice vibrations. So, there are several atoms here and they are vibrating and this collective vibration is called phonon then in doped semiconductor there are some impurities also. So, you can have impurity scattering.

So, different scattering mechanisms are there and during those the scattering or after the scattering these electron you know they move from one state to another state the risks there. So, we have the concept of relaxation time there are 2 prominent relaxation times the standard one. One is the moment of relaxation and other is the energy relaxation time. So, if you compare this relaxation time; with the time taken by electron to cover these nanometer distances.

So, for 1 nanometer, the time is around 10 is to power -15 second also called femtosecond. So, you can say L is 0.1 nanometer divided by the velocity at room temperature. So, this is a time taken by the electron at room temperature and if the size is 100 nanometer then it is 10 is power -12 second so, you call it 1 picosecond. So, there is a typical time and your relaxation time is order of picosecond. So, for nanometers structure the time taken by the electron to crossover is order of relaxation time. So, that we scattering will be less actually and such transport we call it ballistic or quasi ballistic transport and that plays an important role in nanostructures.

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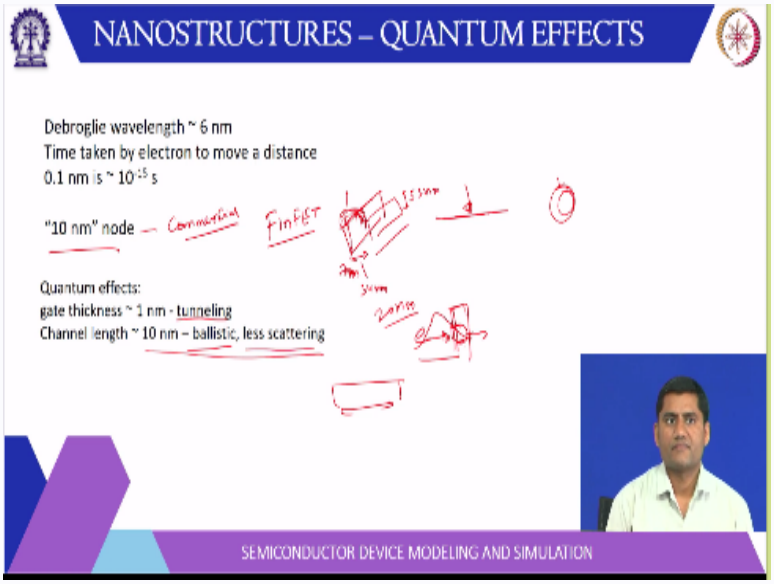

Let us consider this 10 nanometer node today's MOSFET technology. Now, these names are basically commercial once. So, this 10 nanometer node name is a commercial one length of the channel or any physical parameter. This is a convention adopted by ITRs. So, for example, for 10 nanometer node by Intel it uses actually FinFET a structure. So, it is again the FET structure field effect transistor, but instead of having a channel some fins are there which act as a channel.

So, these are vertical structures basically, these are the fins now, why they use fins for better control. So, the gate is covering it from the 3 sides. And then you can better control instead of plenary structure where there is only gate on the top. So, it is covering from 1 side, but in FinFET it is covering from the 3 side and there is a concept of gate all around also we are this is your channel and there is all around there is a gate. So, this is called gate all around the structure and then there is a concept of dual gate triple gate like that.

So, this FinFET the width of this fin is around 7 nanometers and to have more current multiple such fins are arranged in parallel form. So, the separation between 2 such fins will be around is called the pitch. So, that is around 34 nanometers and the height of these fins is around 53 nanometers. So, this is a typical dimension that we are dealing with and the gate length is of course, the length is around 20 nanometer. So, we are actually very close to the Debroglie limits.

Now, what will happen at these dimensions 2 things will happen one is because of this small thickness of the gate now gate is all around this fin. So, because oxide thickness is order of few nanometer so that tunneling will take place. Now tunneling we have discussed that it is a physical phenomena where a carrier can jump across without having the service and energy to cross the barrier. So classically there is a potential barrier. So that means there is high potential which it has to cross, but it does not have that much energy.

But quantum mechanically if the width is small, then this electron can tunnel through. And that comes from the concept of wave nature because these electrons exhibit of wave nature. So there is a probability that you know this electron wave function is penetrating this barrier. And if the barrier is thin, then there is some portion of that wave function is on the other side and that allows the electron to tunnel through.

And another is basically channel length is order a few 10 of nanometer, then because the time taken by the electron to cross over this channel is comparable to the sketch, moment of relaxation time. The procedure that electron follows or the kind of mechanism that through which these electron travel, we call it ballistic or semi ballistic transport. And of course, because it is ballistic, it does not have enough time for a scattering, there is a less scattering. So, when we simulate these structure, these physical criteria have to be considered.

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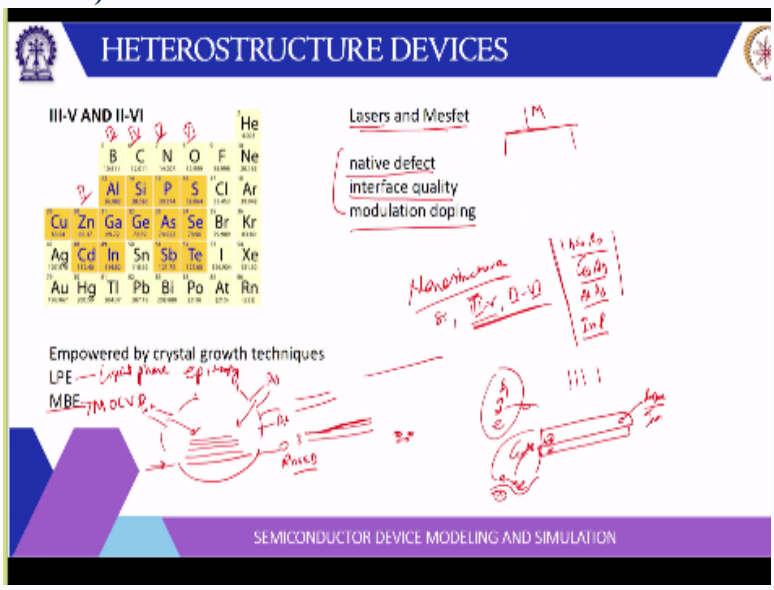

Now, nanostructure is a general concept. So, it not only applies to silicon, but other materials. So, in case of MOSFET, it is all silicon and silicon dioxide and of course, some places polysilicon for silicon nitride also used for covering nanostructure are also applicable to other semiconductor and especially the 3, 5 or 2, 6 semiconductor they are mostly application in generating the light detecting the light. So, LED lasers they are they have the application.

And these 3, 5 semiconductors they come from the periodic table group 3 and group 5. So, you can see this is let us say group 3, this is group 4, this is group 5. So, in group 4 there is silicon and germanium then 3, 5 semiconductor will be combination of any atom from group 3 and any atom from group 5 especially the highlighted one. So, you can have gallium arsenide, gallium antimonite, gallium phosphide, aluminum arsenide, indium phosphide so, different combinations.

And similarly, this is group 2 and this is group 6. So, you can have zinc selenide, cadmium telluride, so, these will be group called 2, 6 semiconductors and the semiconductor became very important once the invention of ledger and MOSFET came into existence MOSFET is basically where metal is connected directly to the semiconductor not to the oxide. So, this is a metal semiconductor junction. So, it is a metal semiconductor field effect transistor.

Now, the devices that are formed by this 3, 5 semiconductor they are called heterostructure because even among the 3, 5 multiple atoms are involved for example, you have gallium arsenide then if you want to make a device with gallium arsenide, a laser or diode LED. So, what we do actually? We have another layer so, that layer can be in gas indium gallium arsenide or you can have a layer of aluminum arsenide.

And of course, gallium arsenide and aluminum arsenide are closely lattice matched that means, they are lattice constant the concept we will discuss in subsequent chapter the spacing between the constitutive atoms is close or nearly equal. So, that when you deposit gallium arsenide on an aluminum arsenide or vice versa, these atoms do not see the difference in the configuration. So, when you grow that material, there will be no defect basically, you can grow a defect free.

Similarly, for indium gallium arsenide up to certain composition of indium you can have it you know defect free. Basically the difference in the lattice constant is not giving rise to the defects for certain composition of indium gallium arsenide and generally, this has also grown on indium phosphide. So, because these multiple semiconductors are involved with you know slightly varying lattice constant, we call it heterostructure.

And of course, they are the same lattice constant or same material, we would call them homostructures or there is a term called epitaxy, homoepitaxy or heteroepitaxy. Now, to get these devices especially the lasers, a very strict quality control on material is required that means, there should not be any defect, if there are defect what will happen then these electron and hole which are making a transient and generating the light, they will instead of recombining they will go and enter these defects here.

So, they will be captured by the defects. So, defect has to be minimal and the interface quality that has to be appropriate. So, that because interface is generally you know, defects are found there. So, if these interfaces are properly passivated and there are no stacking faults or line defects, then we will have good interface quality. So, this defect free fabrication of semiconductor it was empowered by the technique which was invented then it was called liquid phase epitaxy.

So, in liquid phase epitaxy we could get a very good material quality with almost no or minimal defect and that enables the fabrication of these devices. However, there were certain limitation here the control of the thickness was not very much possible with this liquid phase epitaxy and also the interface sharpness. So, let us say this is this your material then here let us say aluminum arsenide is growing here gallium arsenide is growing and then there may be some difference here. So, maybe the interface may be something like this.

So, it is not flat basically or there may be some diffusion of these atoms while growing. So, interface control and that thickness control they were the Susiya. So, then people resorted to techniques where you could grow atomic layer by atomic layer. So, once that technique is called

MBE molecular beam epitaxy. So, they are of course, we have this substrate here, then different sources are there and we can control the sources.

And let us say this is gallium source, this is arsenic source, there may be some aluminum source, so, we can open and close these sources and then this gallium arsenic is coming and they are growing basically layer by layer because very small amount of these atoms actually come through this opening and they are flux the amount of material that is coming can be precisely controlled and of course, there is a measurement called RHEED.

So, they are you sign this source here so, this can tell you over the surface patterns in what kind of surface we are having. So, with MBE you can have a precise control of this atomic layer. So, you can control you know, grow each atomic layer at a time and you can precisely control the hetrostructure. So, this allowed us to further go ahead with another technique called modulation doping, the modulation doping is helpful because, see, let us say this is your some material gallium arsenide.

Then, generally if you dope the semiconductor by doping the semiconductor, we can increase the conductivity of the semiconductor, but with doping comes the ions because these impurity will not only supply the electrons or holes, they will also supply the ions. So, these ions will cause the scattering. So, due to the scattering, the mobility will decrease. So, more or less and doping is basically you grow another layer beside this and such that the potential in this side layer is less so, something like this if you look here.

Then this is the potential something like this. So, then these electrons will actually go here and ions are here. So, I ions are here electrons are here so, these ions and electrons are physically separated and when they are physically separated, these electron can move at higher velocity or they experience less scattering. So, modulation doping actually allows you to get a significant increase in the mobility of the carriers.

So, that is again enabled via atomic layer deposition techniques called molecular beam epitaxy or MOCVD Metal Organic Chemical Vapor Deposition so, MOCVD. So, these techniques are actually allowed to have a better control of devices and better performance.

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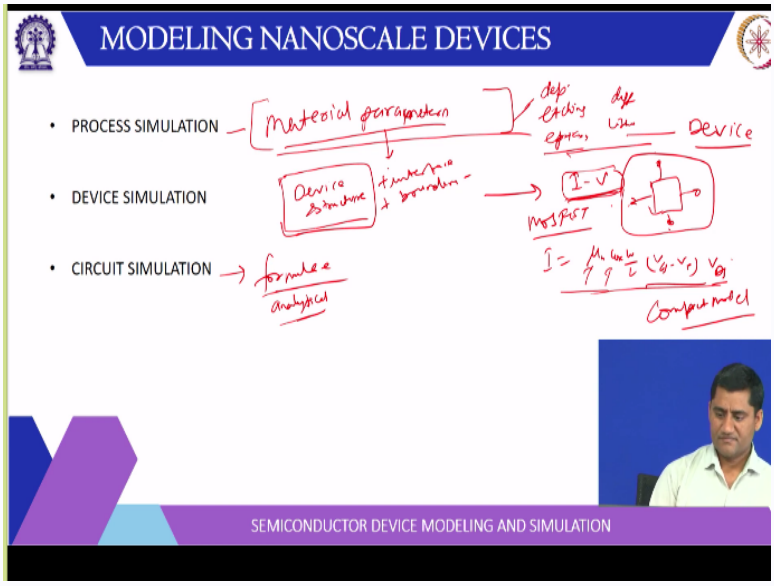

Now, to go ahead with the modelling and simulation of the semiconductor devices we will follow 3 step process it is actually done in the 3 steps first is the process simulation. So, in the process simulation, we specify the material parameters. So, material parameters include the bandgap and lattice constant then they are associated a strain which will again change the event parameters then mobilities of the individual carriers and what are the different energies associated with satellite variants what is the structure?

So, the material parameters have to be specified so, based on the material parameter again then you will deposit the material as the material. So, in process simulation what we will do? We will mostly process the materials. So, the components of the process simulation will be deposits and etching it can be chemical etching or wet etching or you can use Monte Carlo motors also for etching then epitaxy then if there is some high temperature process there will be associated diffuse and also diffusion of atoms then you can use lithography.

So, all these things will be used in the process simulation the end result will be a device. So, after all these processes we will have a device. In device simulation we will have the structure so, the device structure will be the input here and all these material parameters have individual material.

So, this will be included here plus interface conditions if there are some defects, so, there are some charges as an interface then the boundary conditions the applied voltage etch or if there is applied current.

So, different boundary conditions will be there so, they will be used to calculate the device characteristic and here the output of this device simulation will be IV characteristic. So, the terminal let us say a device is 2 terminal or 3 terminal type or 4 terminal. So, for individual terminals what is the IV characteristic? So, that will the output of device simulation and then from this IV characteristic we can extract the some models for those devices and we can compactly represent a given device in terms of some other parameters.

So if you recall this 5 simulation, so they use parameters which are obtained from the IV characteristic of the device. So, simple one that you can recall is MOSFET so, in MOSFET if you recall we use this current is represented by mu and c ux w by L V GS – V T times V DS for linear reason, and parabolic reason, this is quadir V DS square by 2. So, this is basically model parameters. So, here mu n is a mobility oxide carriage trends with length.

So, here if you do the circuit simulation, then you can instead of inserting the whole IV characteristic, you can insert these parameters and then use it the circuit simulation will actually use this formula. It will use the formula to calculate the IV characteristic. So, of course, it is analytical one and device simulation is more physical. So, being physical it has some predictive capabilities and in circuit simulation we use analytical formula so, it will not have predictive capability.

Because in circuit simulation there are a lot of devices a few 1000s to millions sometimes, especially the microprocessor there are a lot of devices, billion devices billion transistors. So, for such case to make the circuit simulation first we have to have these parameters and we call this one as compact model, a compact model of device. So, these compact models are used in a circuit simulation to get the system performance.

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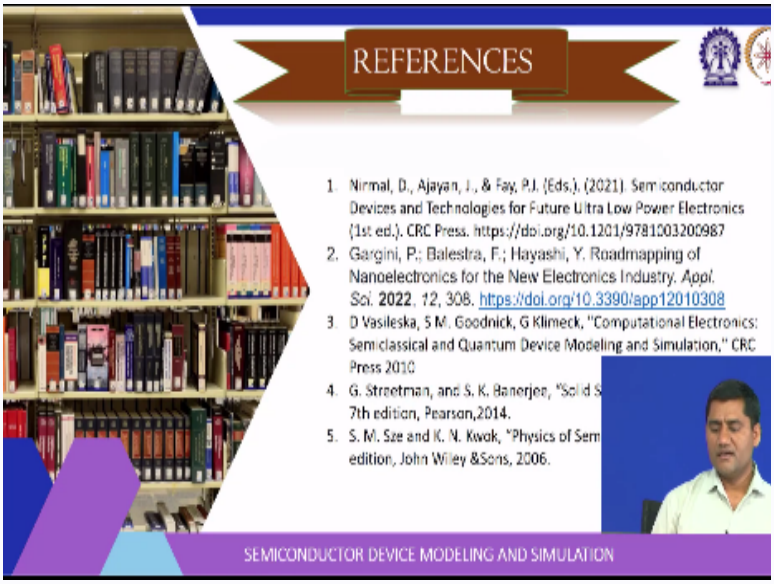

So thank you very much. These are the references here these are the textbook for the projects and then there is the main textbook computers electronics that we are following. And some of the content and pictures are taken from these references, these papers especially related to the IC scaling and all thank you very much.