Semiconductor Device Modelling and Simulation
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Lecture – 01
Introduction

Hello students, welcome to the NPTEL certification course semiconductor device modelling and simulation. This course you can register in NPTEL and on the credits which are approved by UGC. Myself, Vivek Dixit from the Department of Electronics and Electrical Communication Engineering, IIT Kharagpur. I specialize in semiconductor devices, metamaterials, photonic devices and their applications.

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There are several courses related to semiconductor devices are available. How this course is different? So, regarding the motivation, I would like to say there is a famous statement which is attributed to Benjamin Franklin and a Chinese philosopher called Confucius tell me and I forget, teach me and I remember, involve me and I learn. So, here, you will not only learn about the device projects, the working of the semiconductor devices, but you will get the opportunity to simulate these devices using your own code.

You can go through the algorithm, you can write your own code, simulate it. So, those techniques that those techniques you will learn. For example, there are several semiconductor

device simulation software's are available. But, typically, students are not aware what is going on inside some vague idea maybe there. So, to clearly explain what is going inside the semiconductor, inside the simulation software and how it is modelling the devices, what are the equations it is solving, what are the boundary conditions.

And what are the numerical techniques that are used. So, to present it in a complete package, this course syllabus is designed to help the student to capture the complete package.

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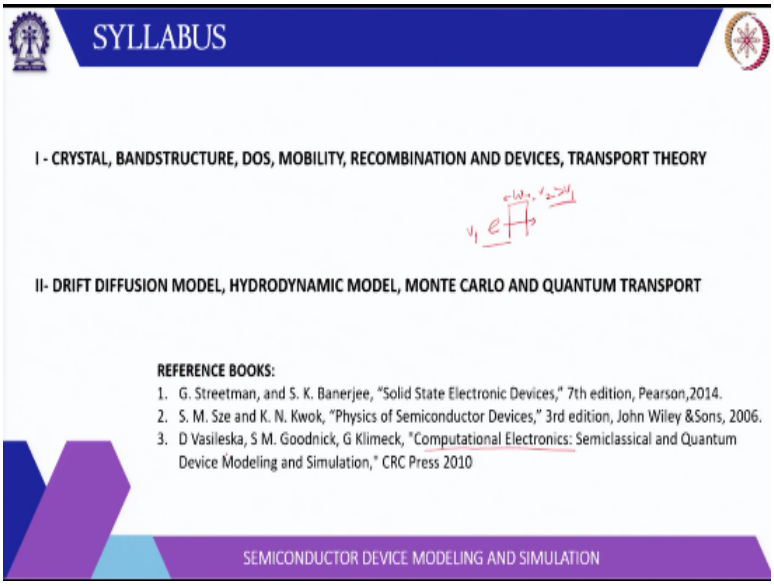

So, the syllabus of this course is first of all, we would like to discuss the crystal structure because that is a basis of any semiconductor, whether you take crystalline semiconductor more or you know, amorphous semiconductor or poly crystalline, they are different grades and they are different applications of course, crystalline being more pure and more, they have long range order, they have greater number of applications and especially they have application in the integrated circuit, where you can integrate a large number of devices.

Then, this crystalline structure gave rise to the bandstructure that means, these electrons the carriers they tend to move with certain energy levels, these energy levels are called bands, there are certain allowed energy levels, there are certain not allowed energy levels within the semiconductor. Then, in these energy levels, which are allowed, we can define that density of states is like you know, in a colony there are houses and there are people.

So, people you can compare them with electrons and houses you can compare with the states. So, inside the semiconductor also there are energy levels. So, these energy levels have certain number of atoms certain number of electrons they can host there. So, that is a states and how many states are there for a given energy level tells you all the density of a state, then whatever the mobility of these carriers, these electrons how they will move.

So, that is largely influenced by the bandstructure whether density of a state and then when these electrons move around, they tend to generate and recombine. So, electron moving in certain energy level, when it drops down to certain weakened state, then we say that you know there is a recombination, because now that electron has gone from that state to a weakened state. And when electron leaves the field state and goes to a weakened state, then there is a hole that is created in the lower energy level and the electron goes to higher energy level.

So, that is a concept of electron and hole. So, the generation and the recombination and these properties of the semiconductor control the device characteristic or others let me put it like this, we can use these properties to create a semiconductor device to model their way here and then of course, the movement of these carriers follows certain rules certain laws. So that we will describe as transport theory, then this is the first part then second part, we will consider very specific models, one is the drift diffusion model.

So, this is one of the basic model where electron or carrier transport is model through the mechanism called drift. Now, drift is basically when we apply electric field these carriers are moving along the field electron moves according to the electric field and holes move along the electric field. So, these are drift and diffusion is basically another mechanism, which is due to the concentration gradient of these carriers. So, when there is a concentration gradient, then this carrier will tend to move from high concentration to low concentration.

So, there is a diffusion. So, this is one of the basic model then we go to higher order models like Hydrodynamic Model, Hydrodynamic Model captures more physics into it, so, that we can apply it for diamonds and with even smaller so, that we can apply it to devices with even smaller

dimensions. So, that also we will discuss then Monte Carlo based simulations are basically track the individual particles or individual carriers and then based on that, we develop some statistic and define what is the current and what are the properties of the semiconductor device.

So, while going through this modelling, we trade the carrier and how they move how they are scattered by different scattering mechanisms for example, at room temperature the crystal atoms they are not you know in a steady state at room temperature, the crystal atoms are vibrating when they are vibrating they tend to scatter these carriers. Then of course, if you dope the semiconductor with certain impurity, then there will be scattering with impurity also, then they are different other mechanisms of scattering.

So, they come into the picture then by considering all these scattering mechanism and their individual contribution can be captured through simulation, we come up with you know average movement of the carriers and with the statistical averages, we can find out the device terminal characteristic. Then of course, we will also consider the quantum Transport Models when the device dimensions are very small and each semiconductor layer is thin enough.

So, that you know electron can make a jump from one material or one band to another band without overcoming the barrier. So, in typical scenario, if you see energy level, so, if electron is here and this is a barrier, it cannot go to other side. But when this width becomes small, they can go through this barrier without having the sufficient energy. So, let us say this energy for electron is v 1, the barrier height or variance is v 2, v 2 is more than v 1, then a classical electron cannot move around.

But quantum mechanical it cannot cross the barrier. Now that is enabled by the way of description of the electron. So, these discussion will be followed in the quantum transport model and reference book for this course, we will be closely following this textbook computational electronics, semiclassical and quantum device modelling and simulation by Dr. Vasileska. And of course, for the detailed discussion about the semiconductor devices and their affiliates, we will also refer to textbook by streetman and Banerjee by Sze and Kwok.

And of course, not limited there are several other good books also there like parrots and other authors also there. So, we will follow these reference books.

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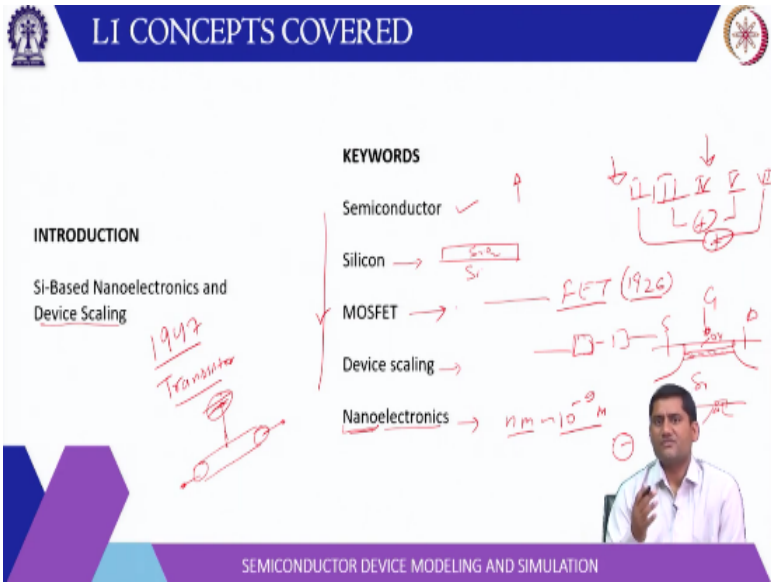

So, this is lecture 1. So, here we will discuss again it is a part of motivation that why some where should add the semiconductor devices. So, one of the primary reason that semiconductor devices have to be discussed because of their application. The number of applications that are attributed or where semiconductor devices find them useful are enormous and there is hardly any part of our life which is not just why semiconductor devices.

The time you go to sleep, you have a semiconductor device, you have some watches, clocks, smart watches, they have semiconductor devices there, then once you get up you are going to use certain let us say you go for betting you go for driving go to your work. So, you track your whole life or whole days routine, and you find out how many semiconductor devices you are using. So, that will inform us. So, that is why semiconductor devices are an essential part of our life.

Apart from being essential, they have very interesting physics also. So, if somebody is curious enough, he will find a lot of things in semiconductor devices to be fascinated by and to be inquisitive about. The one of the primary field here is a silicon based Nano electronics and device scaling. So, the history of semiconductor devices is not very old. Means, if you go to pure

semiconductor devices, you know my bits and pieces, you can go back to a few centuries, but this device is scaling it goes back to 1947 with the invention of that transistors.

Now, prior to this era people had the idea of the transistor axon now transistor axon is basically you can think like this let us say these are the 2 terminals of any system or device and the flow 3 through this terminal is controlled by that third terminal. So, very simple example you can think of is a water tip right here you have a knob, if you turn it clockwise or anti clockwise and that will control the flow of the water through this knob. So, similar thing you can do in semiconductors, you can apply electric field or there are some magnetic devices also.

So, you can basically control and that control is on the third terminal. Before this era, vacuum tubes were used, which were basically power hungry, very bulky and they had some serious reliability issues. So, with the invention of this transistor in 1947 people got a tool which can be integrated to make very sophisticated devices. In fact, people actually predicted you know, a lot of things that we are seeing today.

Just to give you example, around this time, we had some Cray-2 if you search about it, it was computer which was you know, very big size of room. And the computational power of this Cray-2 was comparable or less to the modern day smartphone. So, that is how the technological advancement that we can see over these few decades. Now, if you see this silicon based nano electronics, some terminology you know will be useful and I arrange these keywords in a sequence.

So, first is a semiconductor. So, among the different materials like metals, insulators, semiconductors. Semiconductor is kind of I would say the most useful the reason being other materials like metal and insulator, they are conductivity is more or less fixed, but in case of the semiconductor, you can vary its conductivity by varying the conductivity I mean by applying different conditions by doing different processes. For example, doping is one process.

If you change the temperature, then of course, the conductivity will change let us say if you increase the temperature. If you increase the temperature, metal will so certain decline in the

conductivity semiconductors conductivity will increase but the amount of change or quantum of change will be significant in the case of semiconductor just by doping, you can change the conductivity by order of magnitude of 10 to the power 7 or 10 to the power 9 this much change is possible.

So, you can go from something like insulator with very small conductivity or negligible conduct free to something very close to metal. So, that is the advantage of semiconductor. So, among the 3 materials we have chosen the semiconductor then among the semiconductors, they are different semiconductors are there. If you especially see the periodic table, there is a group 3, group 4 and group 5.

So, this group 4 the atoms in the group 4 they usually give us the semiconductor and we call them group 4 semiconductor because their outer orbital as 4 electrons, so, 4 and 4 combined and they make complete octave another set of semiconductors they come from the group 3 and plus group 5 atoms for example, gallium arsenide, indium phosphide so, they can also give rise to semiconductor, but now there are 2 atoms. So, we call them compound semiconductors and of course, you can combine group 2 and group 6 also.

So, they are also called compound semiconductors and they are also their users. As far as integrated circuit is concerned silicon is most prominent. Now, what is the reason that silicon is most prominent because of its native oxide initially it was difficult to control the purity of the silicon dioxide lying on silicon. So, there was some difficulty in making a useful device from the semiconductor, but as a process is improved, especially with the introduction of clean rooms we could control the silicon silicon dioxide properties.

And this led to the invention of MOSFET the full form of MOSFET is metal oxide semiconductor field effect transistor please remember this field effect transistor concept it actually came in 1926 I think. So, it was bit and date, but due to the unavailability of the pure material it could not be realized but in the form of the MOSFET now, this is the most popular one because you can integrate them and another interesting feature of the MOSFET is that you can integrate them.

So, you can put multiple number of MOSFET on same die or same wafer and they can also be scaled down. So, if you recall the structure of MOSFET it is similar to field effect transistor is in fact one of the field effect transistor. So, you have this oxide layer then there is a silicon here then you have some contact here source and we call it source and drain we call it source because it is supplies the carriers we call it drain because carriers are collected here.

You know, they drain through the drain terminal and then here we apply another voltage to create this channel here, you can create or you can control this channel here. So, if you apply certain voltage this channel will be created, if you apply the positive for it polarity, this channel will disappear. So, basically this third terminal called gate is actually controlling this channel connecting the source and drain.

So, of course, you can make it small you can make it smaller then more is small. So, you can keep on making it as small and small. So, that device is scaling is possible then of course oxide thickness also you can make it small of course, there are you know for every scaling there are some physical limitations you cannot go beyond one atom thickness. So, that is the absolute limit even you know few atom atomic layers will create for some challenges.

So, those we will discuss how the device will extend is when you scale down the semiconductor device and this all together forms the field called nano electronics. Now, nano electronics is derived from that 2 keywords nano and electronics. So, these are electronic devices with sizes in the range of nanometers. So, nanometer is again a lengthy scale which is 10 in to power minus 9 meter to get the idea of nanometer you can see this pen it is a few mm you know the size of the tip of the hair few tenths of micron.

So, if you go divide that by 1000 you get some nanometer size and if you recall the hydrogen atom the radius of the hydrogen atom is order of angstrom. So, these are typical dimensions that you should keep in mind whenever we describe a lengthy scale.

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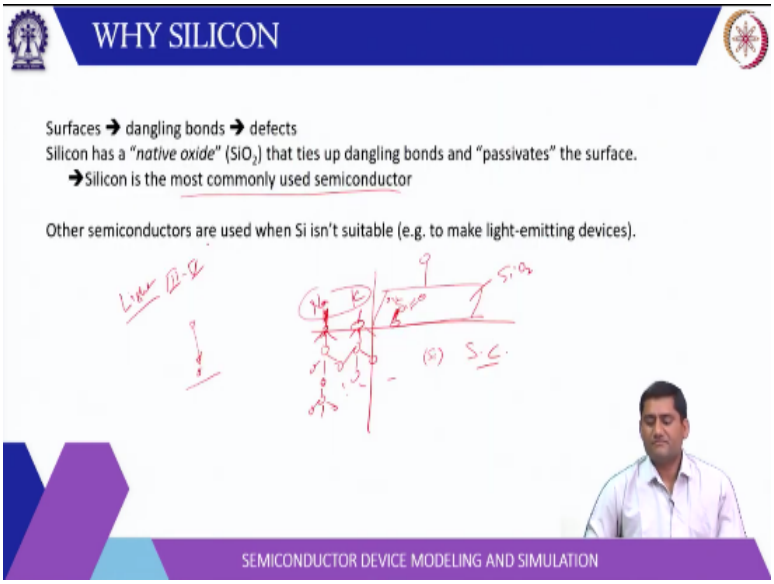

So, this thing I have already discussed why silicon. If you see any semiconductor if you go in the bulk each atom is bonded to certain other atom and this goes on basically. So, in the bulk all the atoms are supposed to be bonded to some other atom. So, there are no bonds which are free. But that is not the case at the surface. So, at the surface there will be some terminating atomic layer. So, this atom only layer is terminating and it will be bonded from one side but there is nothing there is no atom which is bonding it at the top.

So, that means there is a bond that is available for atomic sites that is available, but there is no host atom there. So, host atom is basically this semiconductor let us say it is silicone. So, now there is no silicon atom to bond the top layer. So, they will tend to command is some other atom. If there is impurity around there they will come there sit there for example, sodium can sit there potassium can sit there or any other impurity atom that can sit there.

What they will do? They will create a let us say sodium and potassium are there these are the atoms which make a metal. So, they themselves are mobile they can give extra electron. So, these impurities will alter the characteristic of the semiconductor especially at the surface. So, if you want to use peel defect axon and putting an oxide layer here will not work out because this is basically the surface of the semiconductor is having some defects.

But this defect can be overcome if you have some high quality oxide. So, the advantage with silicone is that silicone as its native oxide Si O 2 and with gels quite well with the this silicon surface when the silicon oxide gels with silicon it does 2 things one it passivates a dangling bond. So, now here is silicon here is also silicon dioxide. So, it is passivating this dangling bond on the top surface and other it is taking care of the defects.

So, that means no foreign atom can sit here and these are the characteristic of this silicon silicon dioxide layer this is not the case with other semiconductors they do not have a such negative oxide. So, that means, once you have silicon semiconductor you do not have to worry about the silicon surface you can always put a silicon dioxide there and passivated. So, this meets silicon is most commonly used semiconductor other semiconductors are used when silicon is not suitable.

For example, light emitting diode, lasers so for emitting the light a certain type of band structure is required, which we call direct band structure so, that means, these electrons and holes they make a vertical transition or they make a transition without the need for the momentum change. So, that of course, we will discuss so, for light emitting application another group of semiconductors called 3 5 semiconductors they are used for example, gallium arsenide, indium phosphide they are used.

Now, nowadays people are still trying to use a silicon for generating light by using different techniques. So, but the power that is received from these devices made up of silicon is quite low. So, they are not that useful as far as current level of research is concerned. So, let me close here we will continue the next class thank you.

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Hello student. So, last class we discussed about the introduction to this course. Now, let us continue our discussion about silicon based semiconductors and the scaling with the invention of transistor 1947 people thought how can we make it more useful? So, that gave us the idea of integrated circuit. So, instead of connecting the components on the breadboard. So, this is a breadboard and these are the different holes on that where there is a wiring in the background.

So, if you put individual devices there, you can make a very small circuit and the applicability of that or the functionality of that circuit will be limited. So, people invented this integrated circuit and the first integrated integrated circuit was invented in 1958 by Jack Kilby from Texas Instrument. It was followed by further invention by Robert Noyce from Fairchild Semiconductor, who made the first planar integrated circuit.

So, it consisted of a transistor, a resistor and a capacitor on a piece of semiconductor you can create a transistor, resistor and a capacitor just to give you the idea, if you have some p and n junction, if you reverse wises bias this P N junction, it can act like a capacitor. And piece of semiconductor if you diffuse certain dopants and then based on the concentration of dopant you can have a resistor here.

So, with this invention Intel co founder Gordon Moore made some observation and what followed was the invention of large scale integration, very large scale integration and ultra large

scale of integration. So, from 1950s, the standard technology was invented early 60s, we call it a smallest scale integration number of transistor limited to 250 and so on. So, by 1990s we already crossed a million tarnished or landmark, then this all was activated to the devices scaling.

So, devices scaling what it did we take basically the number of components per chip, it increase the number of components per chip, it reduced the power consumption per device and with increase in the chip reliability, because many founders were involved and they invested us money in them to study the reliability characteristic and overall the chip price was reduced. I can tell you my own experience in 2005, I purchased 40 GB Hard disk which costed something someone dollar then after few years, I purchased 320 GB Hard disk, same price.

After few years, I purchase 500 GB Hard Disk again almost similar price. So, what is happening for the same price, we are getting more memory or more functionality in as far as processor is concerned. So, there are 2 main things one is the memory and one is a processor.

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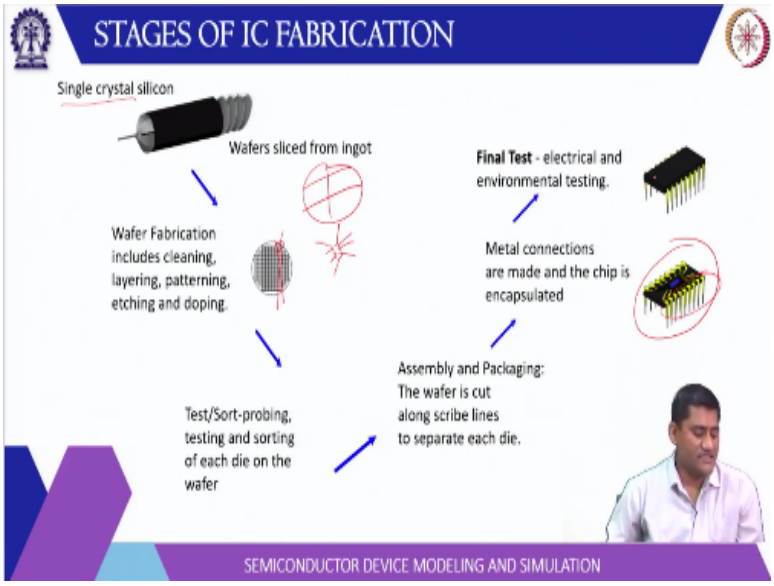

Just to give you the overview how these devices and the integrated circuits are then coming to the market. So, first of all, we start with a single crystal silicon, there are methods to grow these crystal silicon and those Wellsky method and then these wafers are sliced from this ingot and then this wafer is actually is quite big. So, you know several DICE has created out of it. So you can have one dice maybe of this size. And then each dice is tested for functionality.

Whether it is if there is any defect there then these dices are once these dices are initially what is happening, these dices are all dices are together and device processes are done such as etching doping to make these devices and then once these are fabricated and tested then these are cut away. So, along the scribe line, so, these are the scribble scribe lines basically. So, they cut away, we cut away these dices then of course, each dies a very small component, they have some mid some metal connector connections.

Now, these metal connections actually take a lot of space. So, that is why if you see any IC here the size is quite big, but inside the chip is very small. So, mostly the area is taken by these metal contacts and then of course, they are tested for electrical characteristic and the covering is there so that it is not damaged by the environment. So, then that IC comes to the market.

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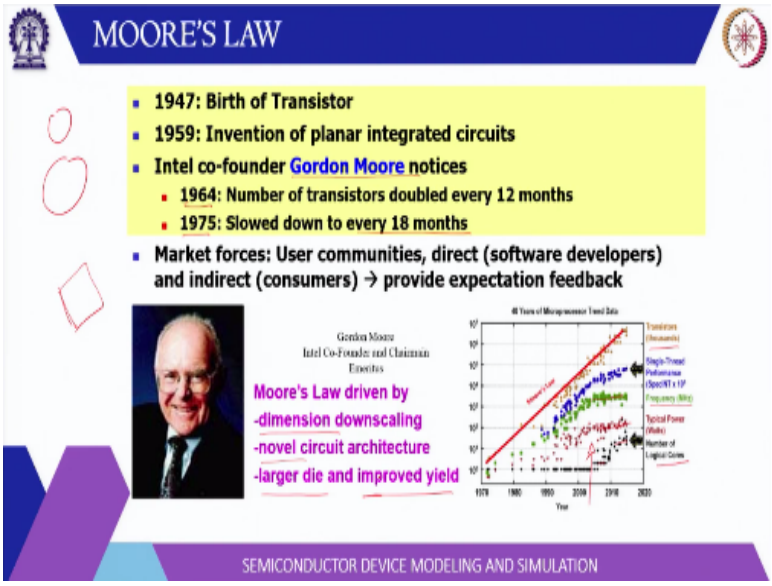

So, the observation by Intel co founder and founder Mr. Gordon Moore, he noticed in 1964 that number of transistors doubled every 12 months and that observation or that prediction continued till 1975 where he made second observation that the number of times are is doubling now, every 18 month. So, although it was based on empirical observation, but the semiconductor industry followed is observation made it a holy grail and they kept that as objective that every 18 month we have we kind of double the number of transistors per unit area.

So, this is basically the Moore's Law denoted by the red line here. And these are the different number of transistors per number of transistor that are you know, closely following this Moore's Law and this the frequency, frequency scaling and if you notice one more thing here, the frequency the typical power per chip and they are more or less constant after some 2003 or 2004. So, that means, that the type of scaling has changed a bit, that we will discuss then instead the performance is enhanced by using number of course.

So, you see here there is a step size here from each step. So, if you increase the number of course, the performance will actually increase. So, Moore's law is actually driven by 3 parameters, one is of course, the dimension, the individual device dimension that have to be reduced then, once you reduce the device dimension, then same area can have more number of devices there then we use novel circuit architecture.

That means, same functionality can be obtained by using less number of devices for less number of transistors. So, that that means, now in the same area you have more devices and even more functionality then a third one is larger die and improved yield. So, die size have also increased over the years, earlier people were using 150 mm then 300 mm and so, on. And yield is basically terms which characterize number of good dice that are fabricated from the lot the percentage of the dice.

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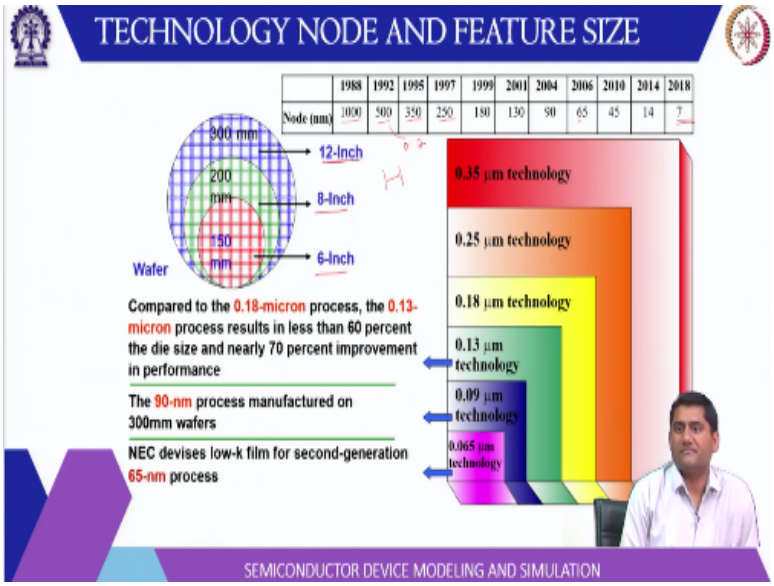

So, here you can see the wafer sizes, the 6 inch wafer which is 150 mm the 8 inch wafer and that 12 inch wafer people did not go beyond 12 inch wafer, because if you increase the size of the wafer they there are some other defects that come into the picture. So, because of this large size, they are can be going of this wafer and the defects section not be controlled. So, well they are and also processing of this large wafer is also difficult. So, this 300 mm or 12 inch standard is optimum.

Then, if you go to the scaling the node size, the node size is basically that distance between 2 closely spaced metal punch lines. So, it is basically as changed from 1988 when it was around 1 micron 1000 nanometer or 1 micron, then it is half to 500 nanometer then 350 nanometer then 250 nanometer. So, if you see here there is a scaling of 0.7 every 3 year every 2 to 3 years, then by 2018 we have already reached 2007 nanometer node. And as they scale in proceed to lower levels, the requirement of new technologies was there.

And in the process people; invented high K dielectric and some NEC devices for less low low k films. And nowadays, we already have microprocessor with 7 nanometer nodes in our mobiles.

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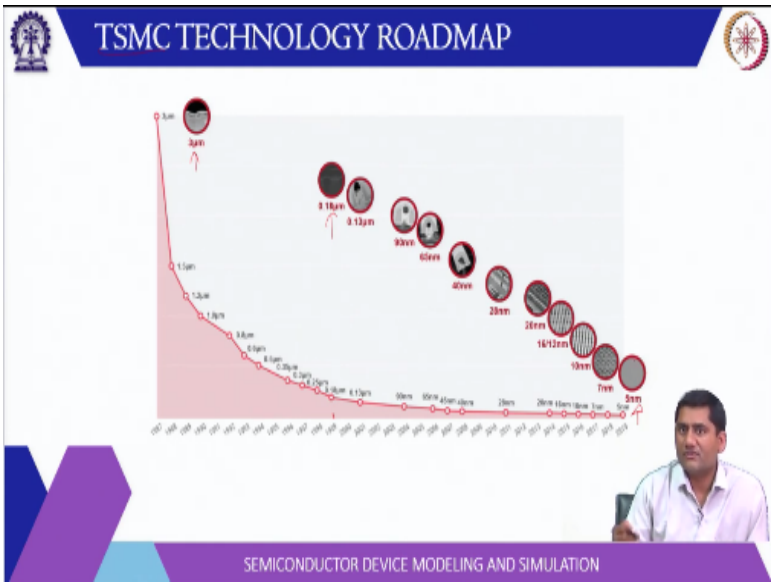

This is a pictorial representation of the technology roadmap by TSMC. So, here you see in 1988, this was 3 micron and then this is 180 nanometer in 1999 and in 2009 19 it is already 5 nanometer. So, these are the typical feature size that are scaling. Now, beyond this if you see you

know, it is already few atomic layer, so, different scaling techniques have to be used. So, as I discussed that, you know, around 2003, there was some chance and now also we are approaching a reason where it is already few atomic layer. So, there will be another change.

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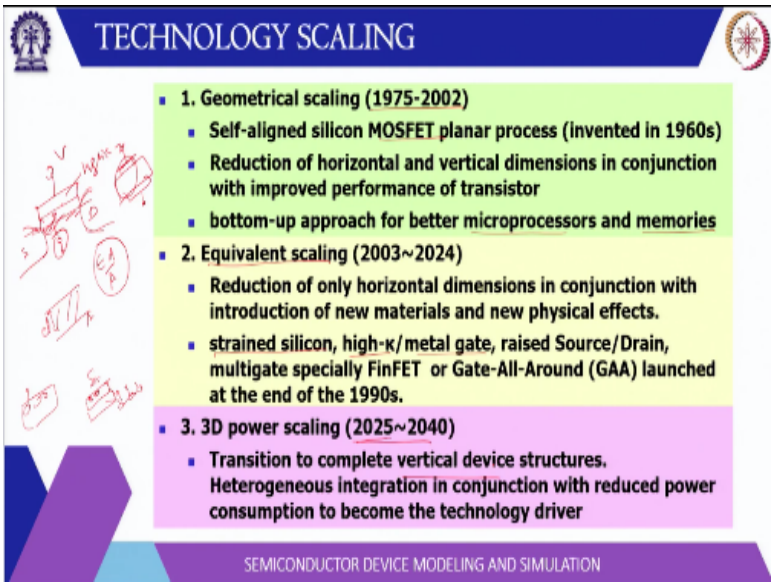

So, this scaling can be divided into 3 eras of scaling. So, one is called geometrical scaling, which was dominant from 1975 to 2002. So, in the geometrical scaling the most FET that were fabricated, they were using this self aligned planner process, which was linear invented in 1960s. And of course, the horizontal and the vertical dimensions of the transistor well reduced and this approach was called bottom up approach.

And of course, the end product for this integrated circuit was the microprocessor and the memories, so, processing power and the memory power then in 2003 this geometric scaling has already reached its limit. So, what people follow the equivalent scaling. So, for example, you have this in MOSFET here is a solo series then here is oxide. Now, if oxide is very thin, you cannot further decrease oxide thickness, because lot of other effects will come into the picture.

Because of this narrow oxide the tunneling will occur then the electrons which are very energetic can hit this reason. So, you know several secondary effects will come into the picture and adversely affect the reliability of the device. So, what people did instead of using silicon dioxide throughout this layer, they use the high k dielectric, high k dielectric. Now, if a material is high k

for example, all of you remember the capacitor a parallel plate capacitor. So, its capacitance says epsilon does the law say a distance between these 2 plate epsilon d / A is the plate area.

So, the capacitance will be more if the epsilon is more. So, we are using this high k here, so, that the Kappa stands is more here. Now, what is the purpose because if capacitance is more than for the same voltage you can have a more charge here. So, more charges there in the channel region you can achieve a higher current. So, people use the high k dielectric there then strained silicon strained silicon is basically you have the silicon material on another substrate with a different lattice constant.

So, let this constant is basically related to the space in between the conjugative atoms so, If you put silicon here on this material with different lattice constant, then the atoms in the silicon will try to aligned along this matrix here. So, then that means, they are either stretched or they are compressed with respect to their normal atomic spacing. So, that gives rise to a strain in the silicon. So, this strained silicon of course, it is a modified structure, we modify the crystal structure.

So, this property will also change. So, with the chance properties, you can achieve higher mobility. So, that is one technique, then of course, people use metal gate also raised source and drain instead of here they can be gate source and drain, then multi gate. Multi gate is basically this channel layer, so, you are applying gate here you can apply gate to the side. So, it is called dual gate, you can wrap it around. So, there are different possibilities, so, multi gate was there.

So, and the common ones that are available are dual gate, tri gate or FinFET these are the different variations or Gate All Around. So, they were all well launched in 1990s that took 8 or 10 years for the research to fructify then since 2003 they came to the production and Intel has already you know in fact, modern microprocessor they are using the FinFET a structures then beyond 2025 even this kind of scaling is difficult difficulty quality scaling. So, now, what people will have to do this is the expected scaling that they will use 3D power scaling.

So, instead of putting the devices on a plane surface, they will also put them in third dimension. So, that will be basically transition to the vertical device structure. So, that is supposed to be the 3D power scaling and let us see how it goes through in the future with reduced power and it may become the technology driver.

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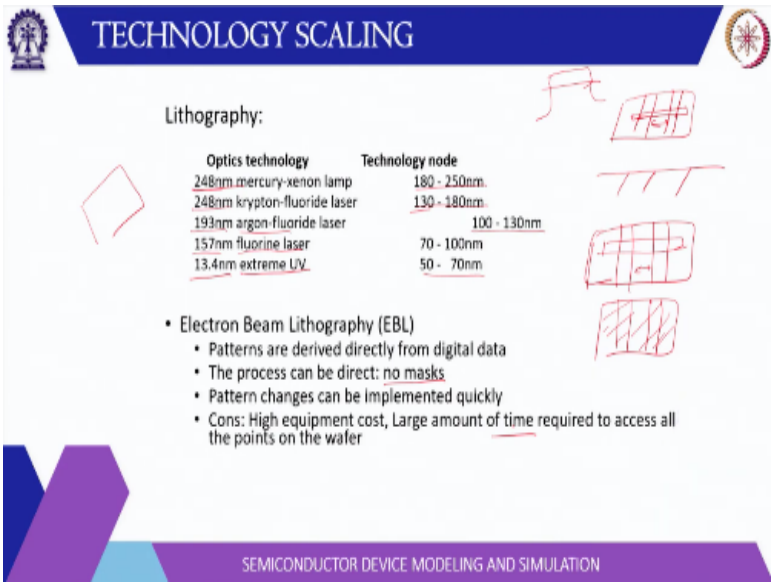

Now, this is scaling is actually M powered by the associated lithography technology lithography technology is basically controls how close to features can be so, what lithographic does basically let us say you have a piece of some wafer or dies then here you want to draw some MOSFET now, what I showed you was a cross section of the MOSFET right this was the cross section of the MOSFET right, but if you look from the top what you will see, we will see some doping layer by layer like this some other doping layer like this.

And then on that there will be something really deposited here. So, the distance between these 2 metal lines is kind of note and how to create the structure on the semiconductor surface. So, for that what is done? If you take a piece of semiconductor you deposit some organic material, which is a photosensitive material then you etch away that material and once you etch away that material this aging process is done through lithographic. So, how do occur some kinds of masks are met.

So, masks are basically some structure, which will block the radiation in certain region and allow the radius in certain region. So, these masks you have to prepare and these masks are put on the semiconductor surface to create the structure desired structure. So, when you edge it away, we use some light sources and the resolution is limited by the wavelength of the light. If the wavelength of the light is small, then we can get a higher resolution.

If wavelength is large, then of course resolution will be limited. So, in early 90s people were using this mercury xenon lamp and that was used for a technology of 180 to 250 nanometers. So, because the wave length of this light is 248 nanometers. Then of course, some other you know, with the mask, we could have some other computational resources to account for the diffraction optical diffraction again using the same laser or the lamp technology note 132 180 nanometer that was realized.

Then to further reduce it, people have started using this argon fluoride laser whose wavelength was 193 nanometer and then we had the technology node 100 to 130 nanometer then came the fluorine laser with where the wavelength is around 157 nanometer. Then nowadays in industry they use extreme UV laser whose wavelength is 13.4 nanometer and they are we have this feature size around 50 to 70 nanometer and beyond.

So, this is used for electron beam lithography because these electrons are the particles which behave like a wave and here the wavelength can be really small. So, these patterns are basically obtained from the use of this electron beam lithography, but of course, you cannot do it manually. So, this electron beam lithography has to be programmed and once it is programmed, then this electron beam will move according to the predefined coordinates to create a direct writing on the semiconductor surface.

So, you know mass are no longer required in this technology and the pattern changes can also be implemented quickly. The only issue with this one is it takes a lot of time last time that is the code because now it is writing point by point. So, that is the main concern here and of course, these comments are high end and usually involve a high cost.

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So, basically we have discussed in this lecture, A Brief History of IC evolution the driving forces, different regions of scaling and various terminologies that are used thank you very much.