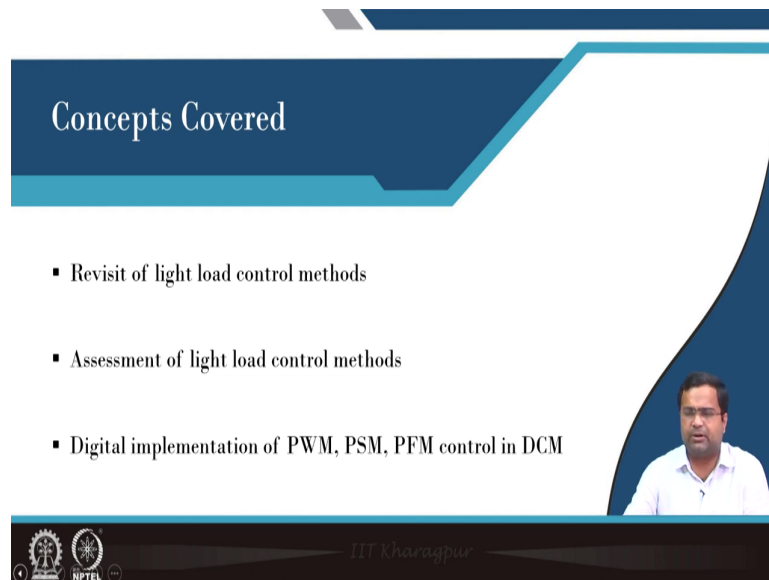


Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
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Department of Electrical Engineering
Indian Institute of Technology, Kharagpur

Module - 10
Steps for FPGA Prototyping of Digital Voltage Mode and Current Mode Control
Lecture - 99
Assessment of Digital Control Techniques for Light Load Control DC-DC Converters

Welcome. In this lecture, we are going to consider the Assessment of Digital Control Technique for Light Load DC-DC Converters.

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Concepts Covered

- Revisit of light load control methods
- Assessment of light load control methods
- Digital implementation of PWM, PSM, PFM control in DCM


The slide features a dark blue header with the title 'Concepts Covered' in white. Below the header is a white area containing a bulleted list of three items. In the bottom right corner of the slide, there is a small video inset showing a man in a white shirt speaking. At the bottom of the slide, there is a dark blue footer containing the IIT Kharagpur logo and the text 'IIT Kharagpur'.

So, here we will first talk about we want to revisit the light load control method and we want to make a comparative assessment then finally, we want to show some digital implementation of PWM pulse skipping modulation and then pulse frequency modulation, particularly for discontinuous conduction mode.

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Switching Loss in DCM

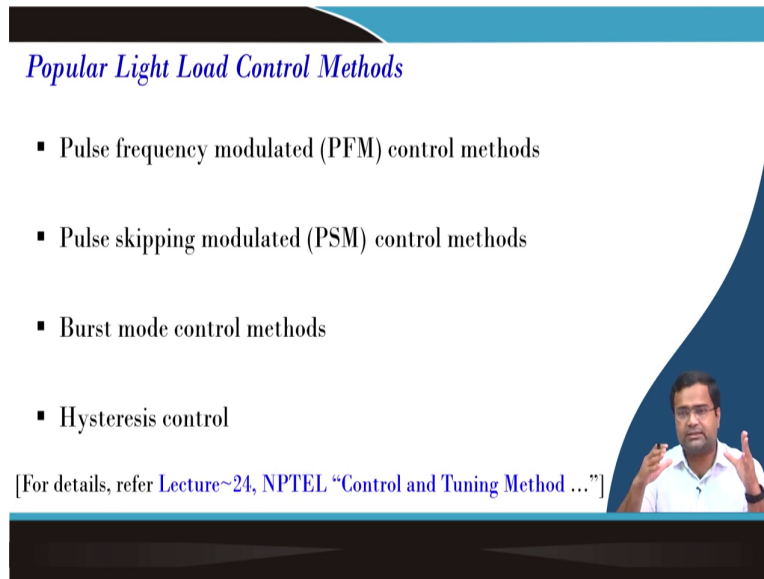
- Efficiency $\eta = \frac{P_{OUT}}{P_{OUT} + P_{CON} + P_{SW}}$
- All switching losses \rightarrow frequency dependent
- Under light load
 - Switch loss P_{SW} dominates at higher f_{SW}
 - P_{SW} can be reduced by decreasing f_{SW}



So, here if we talk about the discontinuous conduction mode as the load current decreases then if you take the efficiency. So, this switching loss particularly the driver loss becomes fixed as a result of the output power decreases. So, this power becomes dominant. And all switching frequency switching losses are basically frequency dependent and under light load conditions this switching loss dominates because the output power is getting reduced. So, as a result, effective switching efficiency will go down.

So, what is the way; that means we need to reduce switching loss by simply reducing the effective switching frequency and there are many ways to do that.

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Popular Light Load Control Methods

- Pulse frequency modulated (PFM) control methods
- Pulse skipping modulated (PSM) control methods
- Burst mode control methods
- Hysteresis control

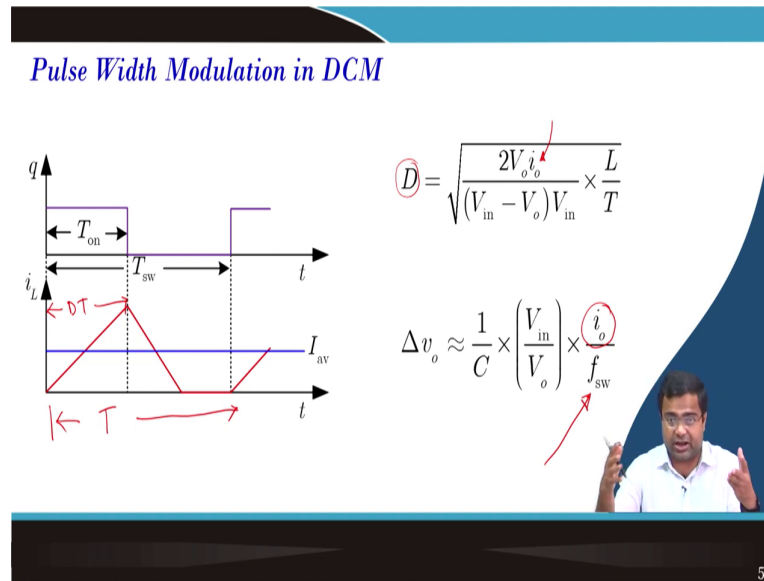
[For details, refer [Lecture~24, NPTEL “Control and Tuning Method ...”](#)]

The first way is the popular light load control method and pulse frequency control method. You know maybe constant on time is a good example then adaptive on-time control also the hysteresis pulse comes under pulse frequency.

Whenever the frequency varies you know with the operating condition then we call we talk we call them to pulse frequency modulation. Another popular control technique is pulse skipping modulation. Where the number of skip cycles changes, as the load current changes, and that way if the load current decreases the skip cycle will increase. So, the effective time period will increase as a result the switching frequency will reduce.

And the burst mode is another popular control method as well as hysteresis control. So, all these details of this particular technique and as well as their MATLAB implementation are already presented in lecture 24, in our earlier NPTEL course.

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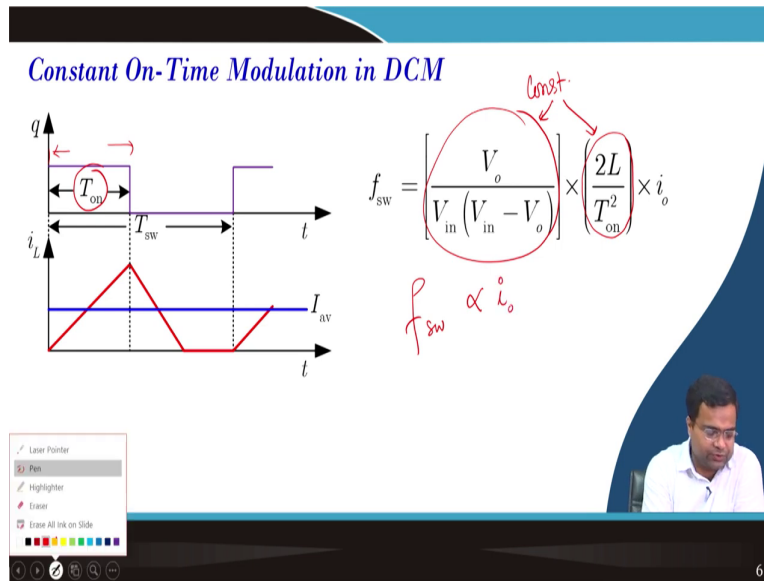


So, here if we talk about pulse width modulation under; that means, we are talking about the frequencies fixed. So, this is on under fixed switching frequency and this is our duty ratio D into T that is the on time.

Now, if we consider the duty ratio unlike in continuous conduction mode in a buck converter. In the ideal condition, we know the duty ratio is nothing, but the ratio output voltage by input voltage, but in the case of discontinuous conduction mode it is a non-linear function and it is also a function of load current. So, if the load current decreases for a given input-output voltage, the duty ratio will decrease this is clear from this expression and it will change the square root fashion.

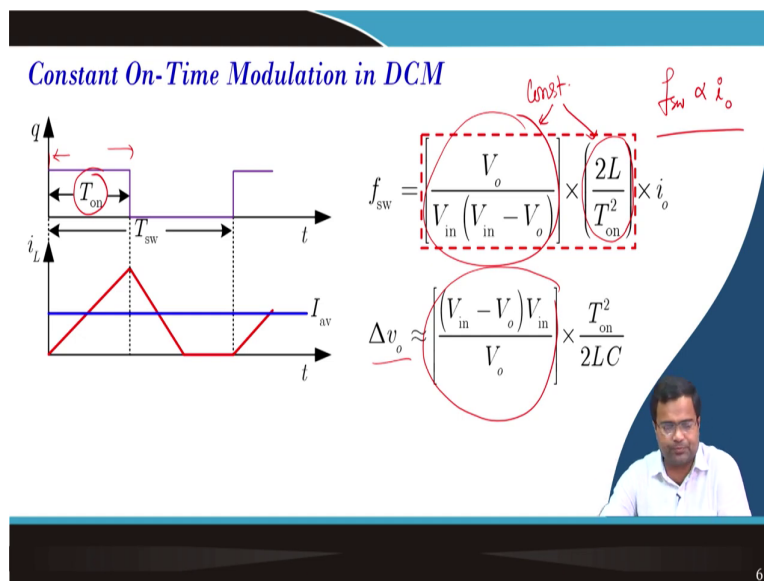
But at the same time under pulse width modulation if the load current decreases then it can be shown approximately the output voltage ripple also linearly decreases, but we do not need a very very small ripple voltage, because as long as the output voltage ripple is within the acceptable range. Then we do not need to further reduce, because what we are losing here is the switching frequency is fixed and that is not desirable, because it will result in a higher, particularly the driver loss.

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So, to do that people go for constant on-time where this on time is constant. You can see this on time is constant this is constant and if we keep the on-time constant and if the inductor is constant, which is generally constant then for a given input-output voltage this quantity is also constant. So, this quantity is all constant quantity then it can be shown that switching frequency is linearly proportional to load current.

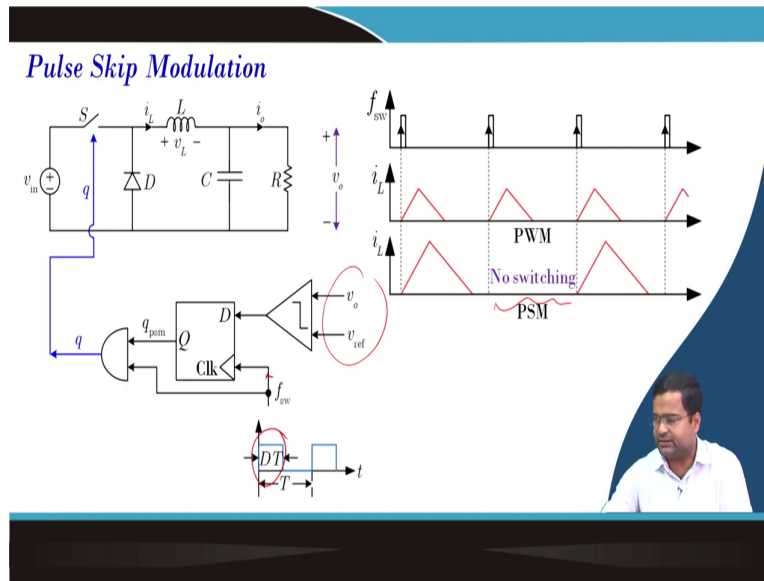
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So, we can take the switching frequency from here it is clear. The switching frequency is linearly proportional to the load current and; that means if the load current decreases

switching frequency will decrease as a result the efficiency will increase. And it can be shown in this method again if the input voltage and output voltage are constant then the output voltage ripple is more or less insensitive to you know the load current and this is particularly true when the converter operates under a light load which is deep into discontinuous conduction mode.

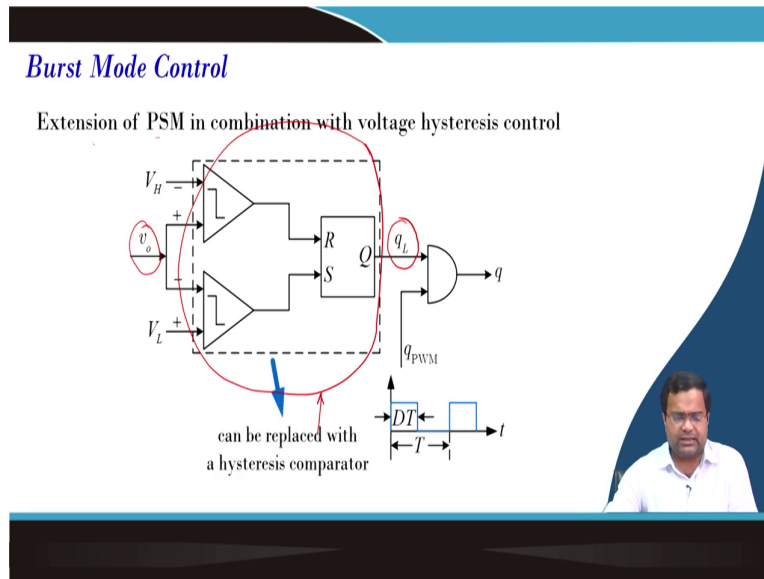
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And the pulse skipping modulation also we have discussed and in fact, we have considered you know pulse skipping modulation digital implementation. And in this particular method in the analog case, if you take the clock edge of this signal and it will compare if the V_0 is greater than V_{ref} it will skip the pulse, otherwise it will take this pulse width and it will pass.

And this method we have already explained and as the load current decreases for a given duty ratio, the number of skip cycles increases as a result of the time period increases and the switching frequency decreases.

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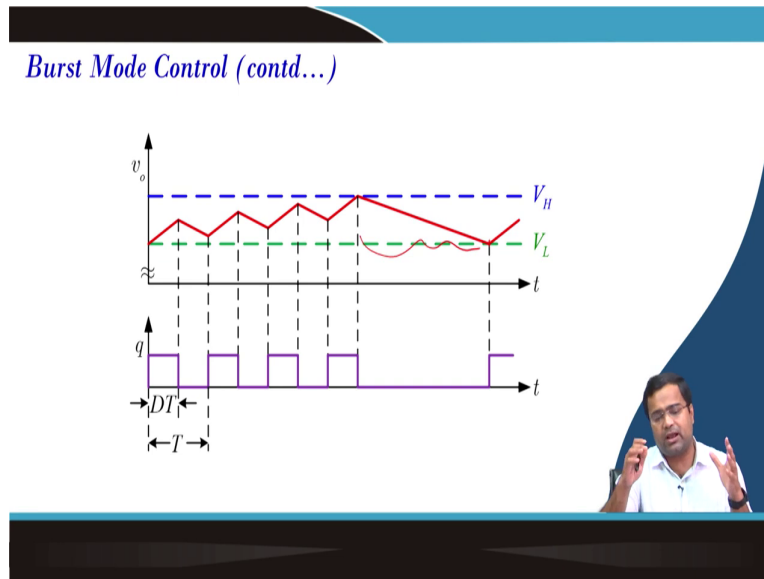


So, this is also a very popular method. The burst mode control method is an extension of pulse skipping modulation, because here also this is effective like pulse skipping.

But in addition to that earlier we have only compared output voltage ripple output voltage with the reference voltage. That was a pure comparator. Now instead of a pure comparator, we have introduced a hysteresis comparator, which can be approximately realized by this method. So, the difference here it is a pulse-skipping modulation, but with an analog hysteresis band and this will make the operation asynchronous.

Unlike regular pulse skipping which will always sense skip or charge pulse based on the edge of the PWM clock, here it depends on your band.

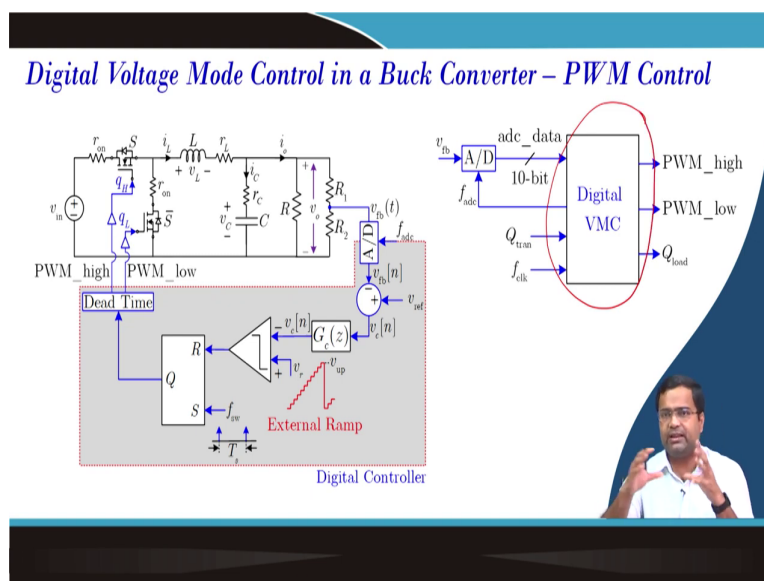
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If the inductor current hit the upper band irrespective of the clock it will simply turn off. And again it will turn on when it hit the upper limit. So, this particular duration operates asynchronously.

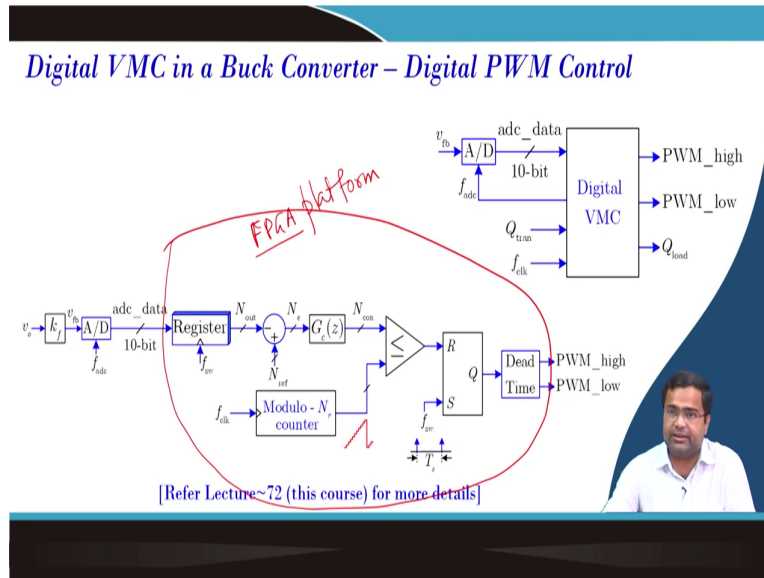
That is why in some cases the burst mode control it is very difficult to predict the power spectral density. So, that is one of the drawbacks. Otherwise, this is the popular control method.

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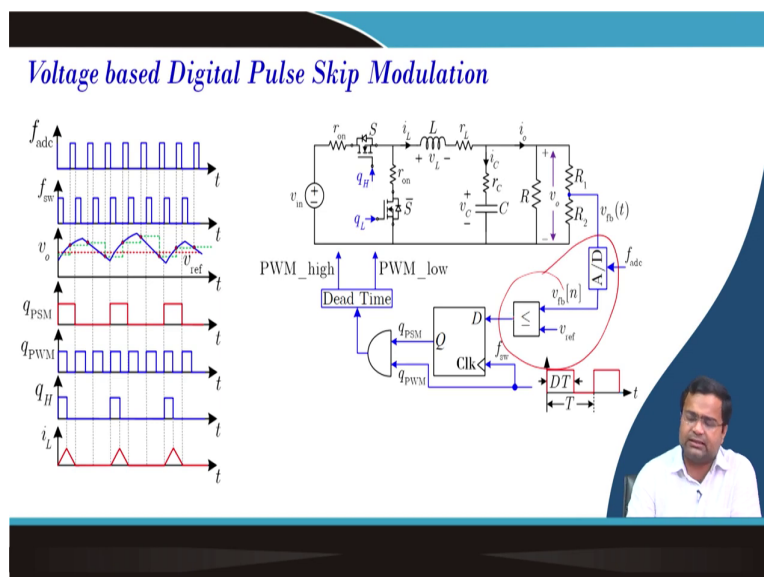
Then we discussed the digital implementation of PWM control and we discussed how to write the Verilog code of this and we synthesized for implementation into FPGA-based prototyping.

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And we have discussed the inner circuit detail of this which is there inside the FPGA and we have implemented this inside an FPGA platform we are not going to discuss this. So, this thing we discussed in week 8th in detail and particularly lecture number 72 we started, and we have continued till 75.

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Then we have also discussed digital voltage-based pulse-skipping modulation.

Here again, we are using a 2D. So, now, there is as if no comparator is needed because this itself will act like a comparator.

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Digital Implementation of Digital Pulse Skip Modulation (DPSM)

[Refer Lecture~80 (this course) for more details]

And we have discussed in detail lecture number 80, how to implement this digital pulse skipping modulation and we have used we have also shown the Verilog HDL code for implementing this control logic.

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Voltage based Constant-On Time Control

[Refer Lecture~95 (this course) for more details]


We have also discussed the voltage-based constant on-time control, which is a fixed variable frequency control where we are keeping the on-time constant and the switching frequency will vary linearly with the load current we have discussed in lecture number 98, and 95 how to implement this voltage based digital constant on-time control using Verilog HDL. How to program it? And we have also implemented using an FPGA device.

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Steady State Characterization of a Buck Converter in DCM

Modulation Technique	Voltage ripple (Δv_o)	Switching frequency (f_{sw})
Pulse width modulation	$\Delta v_o \approx \frac{1}{C} \times \left(\frac{V_{in}}{V_o} \right) \times \frac{i_o}{f_{sw}}$	Fixed f_{sw} , but varying duty ratio $D = \sqrt{\frac{2V_o i_o}{(V_{in} - V_o)V_{in}}} \times \frac{L}{T}$
Constant on-time modulation	$\Delta v_o \approx \left(\frac{V_{in} - V_o}{V_o} \right) \frac{V_{in}}{2LC} \times T_{on}^2$	$f_{sw} = \left[\frac{V_o}{V_{in}(V_{in} - V_o)} \right] \times \left(\frac{2L}{T_{on}^2} \right) \times i_o$

Ripple voltage increases with increasing input voltage



So, if we do steady state characterization of the pulse width modulation the ripple voltage decreases load current which you do not want, but it results in a higher driving loss at light load, because of using a higher switching frequency, but if you go to constant on time the switching frequency linearly varies with load current if the input-output voltage is constant and we are keeping on time is constant anyway.

And it is interestingly the output voltage ripple is more or less independent of load current which is why it is a very popular control method. Majority of the commercial product goes by the constant on time this is a category of PFM Pulse Frequency Modulation, but one of the drawbacks is that if the input voltage increases then this quantity increases as a result the ripple voltage increase and it may exceed the ripple specification.

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Adaptive On-Time Control

- Peak current based approach

For a buck converter,

$$\Delta v_o \approx \frac{T_{on}^2}{2LC} \times \frac{(V_{in} - V_o)V_{in}}{V_o}$$

Substituting $T_{on} = \frac{Li_{peak}}{V_{in} - V_o}$

$$\Delta v_o = \frac{Li_{peak}^2}{2C} \times \frac{V_{in}}{(V_{in} - V_o)} = \frac{Li_{peak}^2}{2C} \times \frac{1}{(1 - K_v)V_o}$$

For smaller voltage gain, i.e., $K_v \ll 1$

$$\Delta v_o \approx \frac{Li_{peak}^2}{2CV_o}$$

Handwritten notes on slide: $V_{in} \rightarrow \text{fixed}$, $m_1 \rightarrow \text{fixed}$, $T_{on} \rightarrow \text{fixed}$

Lec. 24

And that is why you know we go by we have also discussed adaptive on time where instead of giving an on time by a timer we can generate this on time using a peak current limit. And this is based on analog peak current which we have discussed in our earlier NPTEL lecture I think lecture number 24 lecture 24 in our earlier course; means, control, and tuning method. That it can be shown in this method if the input voltage is fixed then m_1 is.

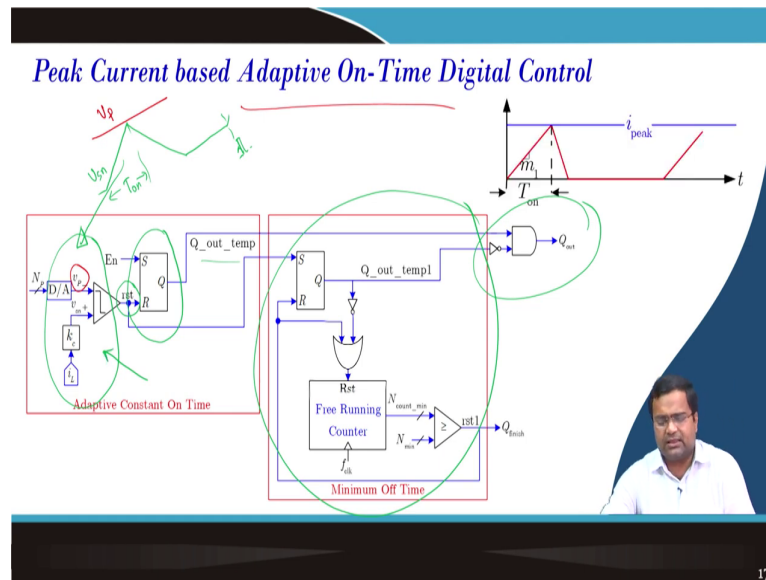
So, if V_{in} is fixed, V_{in} is fixed then m_1 is fixed, if m_1 is fixed this is anyway fixed. So, you're on time is fixed. If the on-time fix then it is like a constant on-time control then it retains all the features including the switching frequency variation with load current that is already there, but what was the major concern? The ripple voltage varies with input voltage now if you substitute this on time as a function of the slope and the peak current then it can be shown that approximately the ripple voltage is a function of peak current output voltage then capacitor and inductor.

So, now it is independent of input voltage and at the same time, we know that the output voltage ripple is already independent of load current in PFM. So, this is called adaptive on time where the on time will be automatically adapted because we are fixing the current ripple. So, when the input voltage increases then as if this will go like this again it will hit it will come back it will come back, and then.

So; that means, the on-time will get automatically reduced and the ripple band will be more or less the same. If the input voltage decreases then it will hit like this. So, it will

automatically increase on time. So, as a result, the ripple voltage will be more or less the same. And you will retain the same feature of constant on time and it will automatically adjust the T_{on} to optimize the efficiency because we want also high light load efficiency.

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And we have discussed in lecture number I think we are going to discuss you know in the next lecture the implementation aspect detail implementation aspect and Verilog implementation of this adaptive on-time digital control, but here is what we are explaining here. So, we are considering; that means, this as our peak current. If you take the analog and this is our sense inductor voltage; that means, sense voltage means the v_s which is the sensed inductor current and it is a voltage form. So, then when it hit then continue to operate in DCM like that again goes.

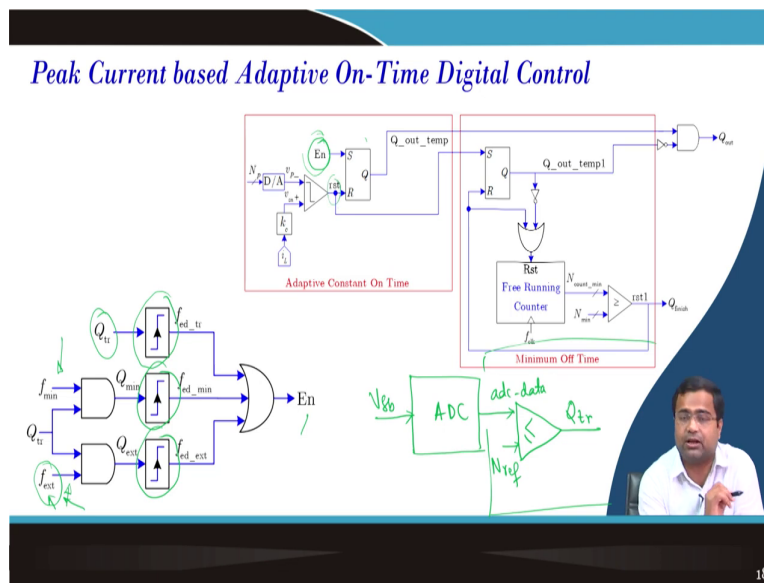
So; that means, this is our T_{on} which is coming out of the current loop and it will be adapted automatically. So, if we recall our traditional constant on time there is a difference here we are retaining the same r s flip flop which will decide the on of this Q out, but there we have generated this reset pulse from a counter. Where we have given a fixed timer to count the on time and then it will reset that r s flip flop.

But here the reset is generated by using an analog current loop. That is why it is a mixed signal implementation, but the voltage loop is still there which decides the triggering of the on the pulse which means when to trigger on the pulse that will be coming from the voltage

loop that is in digital, but once it is triggered how much will be the on time this will be decided by this loop.

So, the on-time will be decided by the current loop, but the triggering of the on the pulse will be decided by the voltage loop we have also discussed that any constant on-time commercial product will have a minimum off time and this we have discussed in detail in lectures 95 and 96. So, we are not going to discuss all this we have discussed. The only difference here we have replaced the counter with this current loop.

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And this is the implement waveform and here we have generated this trigger path because enable has to be generated and how it works we have discussed. This Q trigger is coming from the voltage comparator because we have taken an ADC, ADC, and ADC was taking the feedback voltage and we know the ADC data since we do not have an analog comparator. This was compared with our Nref which is the reference voltage.

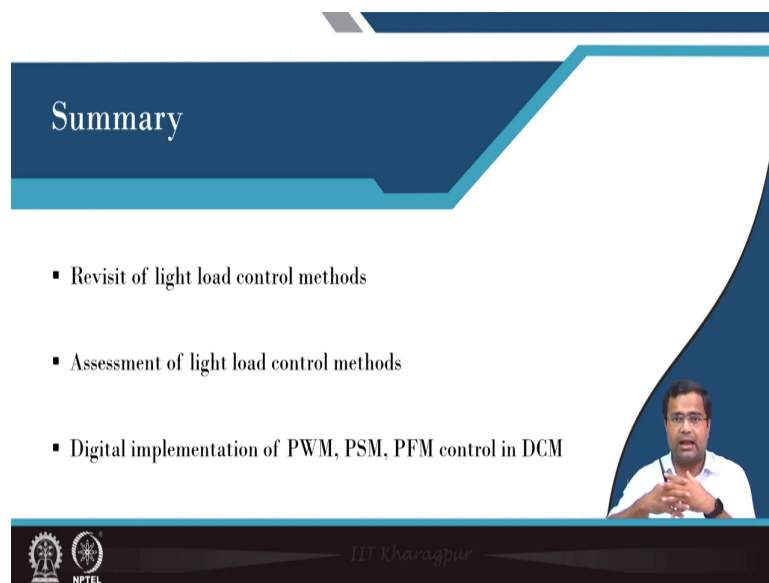
That is the reference command in digital because this portion is digital. This portion is digital. Then what was the logic? If ADC data goes below Nref; that means, that means whenever the output voltage falls below the reference voltage then you need to trigger this count on constant on time. So, this is your Qtr. Now, this Qtr is based on the different possibilities that we have discussed.

We will generate these all are s trigger circuits to detect the positive edges, but we know constant on time will also have a minimum off time that is also here logic and also during the start of the circuit. If the circuit does not turn on for a long time then there will be a periodic external clock that will check the status. If the Qtr is high; that means, if the output voltage is below the reference voltage and we have not yet started the constant on-time operation then this clock will force us to enable the constant on time.

Once it is enabled then it will go automatically. So, that is why this is for you now checking the status and forcefully turning on the switch if the Qtr is high. And we know once the constant on time is enabled then this enabled pulse can come multiple times it will not respond as long as the current inductor current reaches the peak current limit.

Because this will only get reset when this will come and this thing we have discussed.

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Summary

- Revisit of light load control methods
- Assessment of light load control methods
- Digital implementation of PWM, PSM, PFM control in DCM

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So, in summary, we have revisited the light load control method we have discussed some assessments of various light load control methods and we have shown some digital implementations of PWM, PSM, and PSM control methods in DCM, which we have already presented different lectures in previously lectures

And in the next lecture, we are going to show the Verilog implementation of adaptive on-time control that is it for today.

Thank you very much.