Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 10
Steps for FPGA Prototyping of Digital Voltage Mode and Current Mode Control
Lecture - 98
Stability Comparison of Fixed and Variable Freq. Digital CMC with Experimental Results

Welcome to this lecture we are going to talk about the Stability Comparison of Fixed and Variable Frequency Digital Current Mode Control with some experimental case studies.

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So, here we are going to talk about we want to revisit the Mixed signal fix and variable frequency current mode control method. Then we want to show experimental results of stability status with a close current loop and we want to show some assessment. We want to make a comparative assessment of the fixed and variable frequency control methods current mode control method.

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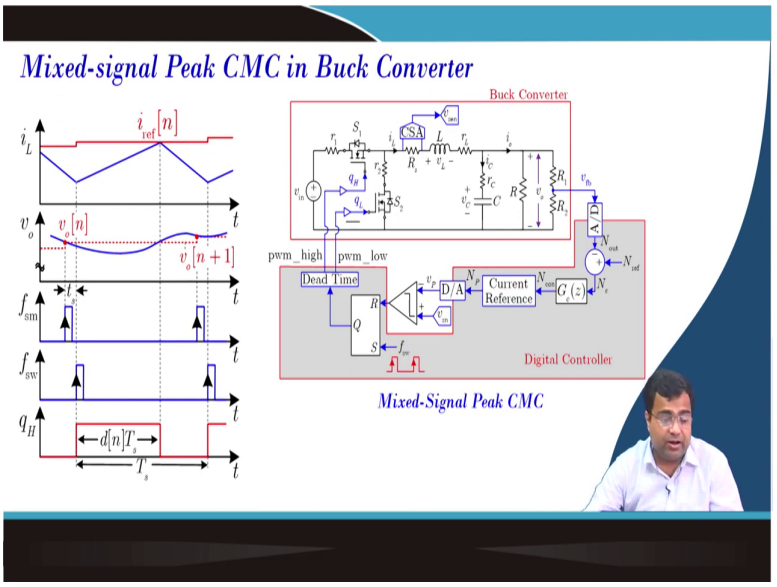

So, you already have discussed mixed signal peak current mode control. So, we are not going to spend time on it. And we know you know the functional waveform.

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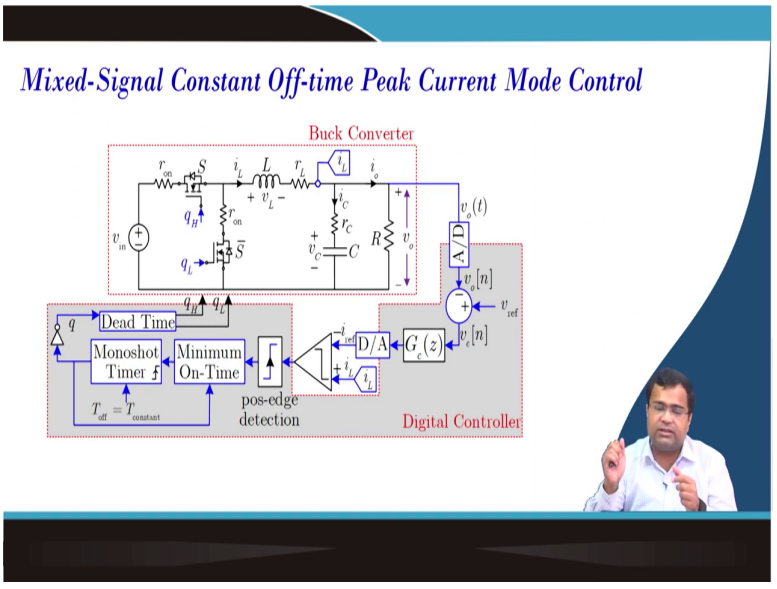

And we also know the mixed signal constant off-time peak current mode control the only difference between the fixed frequency peak current mode and this peak constant off-time peak current mode. Here the off time is fixed and the fixed frequency time period is fixed.

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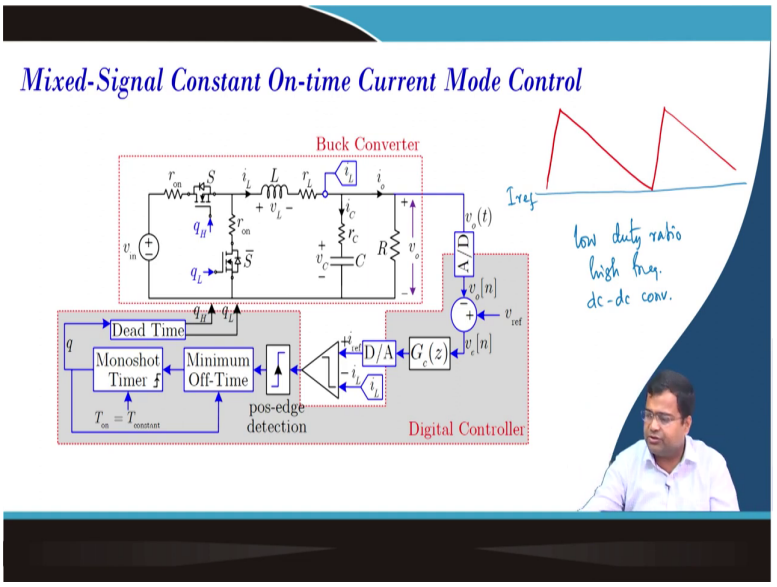

But both have the peak current-based architecture in case of constant on-time current mode control. It is a valley current mode control, where on time is fixed and it is the valley current mode control and we are not going to show valley current mode fixed frequency control this is not.

So, popular, but this constant on-time current mode control is very popular because if you are talking about you know data center application even for low duty ratio pol application. Where the on time is small and for that on time peak current mode fixed frequency will be stable, but it will be difficult to implement when you go for high frequency.

Because you have to take care of the comparator action everything, but this constant on time is very popular for low duty ratio operation because the on time is just the timer. And during the off time, you will get a large time. So, I am talking about the scenario when the duty ratio is very large and you will get like this. So, in such cases, this constant on time is a very popular architecture where this is your reference current.

So, this is particularly for low-duty ratio high-frequency dc-dc converter ok. And we have shown in the earlier lecture that this valley current mode is constant on time and peak current mode is constant on time. Both are inherently current loop stable irrespective of the duty ratio. Whatever the duty ratio the current loop is stable.

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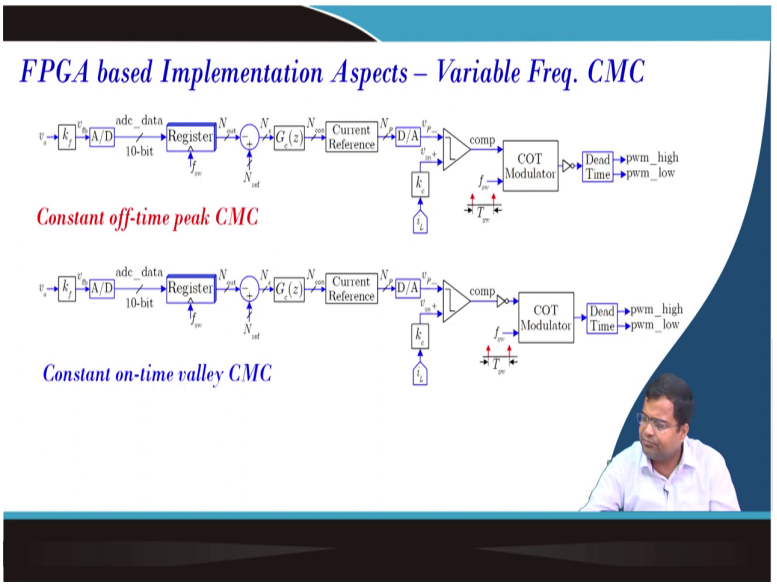

So, now, we have discussed the FPGA implementation aspect of variable frequency current mode control like a constant off-time peak current mode control as well as constant on-time very current valley current mode control and we have also discussed the fixed frequency peak current mode control in detail in lecture number 75, 76.

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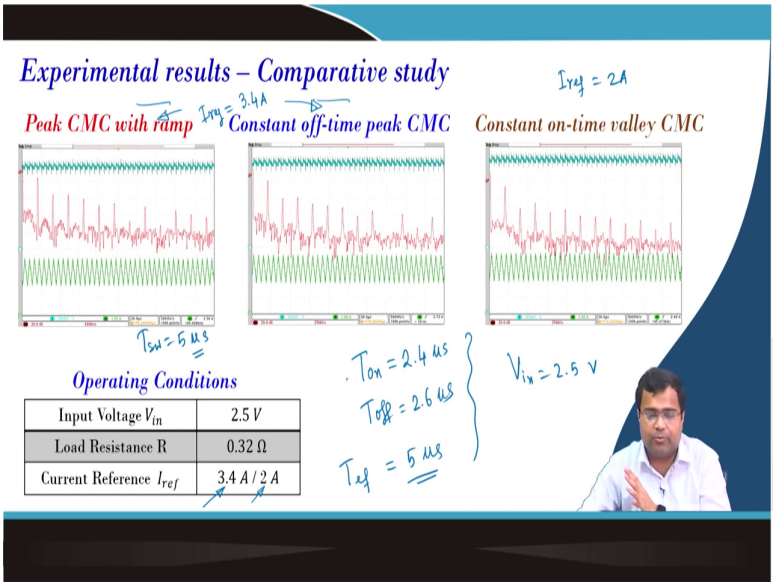

So, we want to show the experimental case study.

So, at 2.5 volt input for peak current based architecture, which is the case of peak current mode control here with ramp. We are talking about and here we are considering 2 ampere for the valley current mode control; that means, for constant off time. So, these 2 are peak current mode control and we have considered 3.4 ampere as the Iref.

So, for both this cases for this case as well as this case, but for constant on-time control, we have considered the Iref to be 2 ampere because this is a valley current mode control. And at 2.5 volt input, we have selected the on time and off-time in such a way. So, Ton is found to be 2 point 4 microsecond and Toff is found to be 2.6 microsecond. So, they are very close to the 50 percent duty ratio, because the effective time period we want to be 5 microsecond ok. So, this switching period is 5 microsecond, because we are using fixed frequency control ok.

Now, when you decrease the input voltage from 2.5 to 2.25 so, we have selected Ton Toff for this case where the input voltage; that means, these all are designed for Vin equal to 2.5 volt, but these are all closed current loops we have not closed the outer loop.

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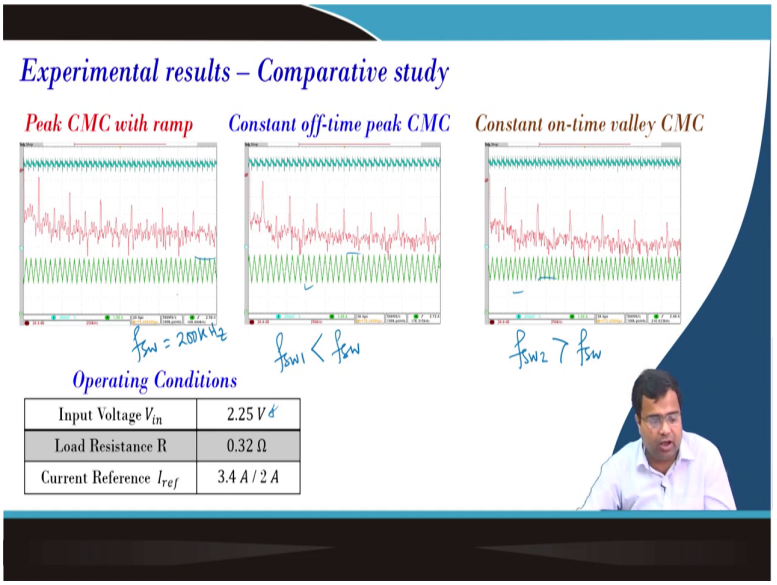

Now, what will happen if suddenly decrease the input voltage? So, naturally for this case for constant off time the time period; that means, we have fsw which is 200 kilohertz here fsw1 we know it will be smaller than fsw and here fsw2 will be smaller than fsw, and here peak currents are fixed valley current is fixed, but these 2 are perfectly stable and here it is stable by using ramp compensation. Otherwise, it was unstable we saw in lecture 193.

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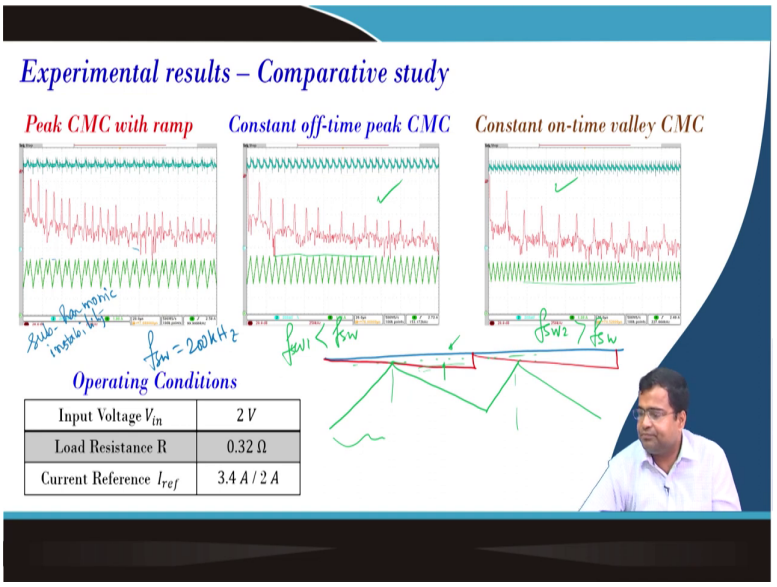

Now, if we reduce that input voltage to 2 volt then fsw is still 200 kilohertz, but you will have a subharmonic instability. Even with ramp compensation, because we have not considered a large ramp we have just considered a ramp that is not enough to fully stabilize the current loop. So, you need to increase the ramp we have discussed this ramp and you can see the rent references for each case are not identical.

Why? Because if you consider this is without ramp now with the ramp we will have something like this. Now, you have a current loop instability problem here. Here let us say. So, since these 2 points are different. That is why the subsequent points one is higher one is lower because it is because of the ramp and ramp if your hitting point; that means, this timing is different then naturally these values will be different and as a result the effective peak of the inductor currents are different.

Even though you set a reference current this is because, because of using this ramp. So, the actual inductor current will not be fixed. Because the ramp will change and if the sub-harmonic is there ramp will be different this is one of the problems of ramp compensation, because if you want to precisely control the current reference or peak current even for a high-duty ratio operation.

Then if you add a ramp to this precise current you know control of the peak current is not possible, because the ramp will set the revised current reference or updated current reference which is not which is smaller than the actual peak reference current. And that is why, but if

you consider constant off time they are fixed and if you consider constant on time the valley current is fixed, but the drawback here fsw1 is smaller than fsw and fsw2 is much larger than fsw, but they are all stable for these 2 cases stable without any ramp.

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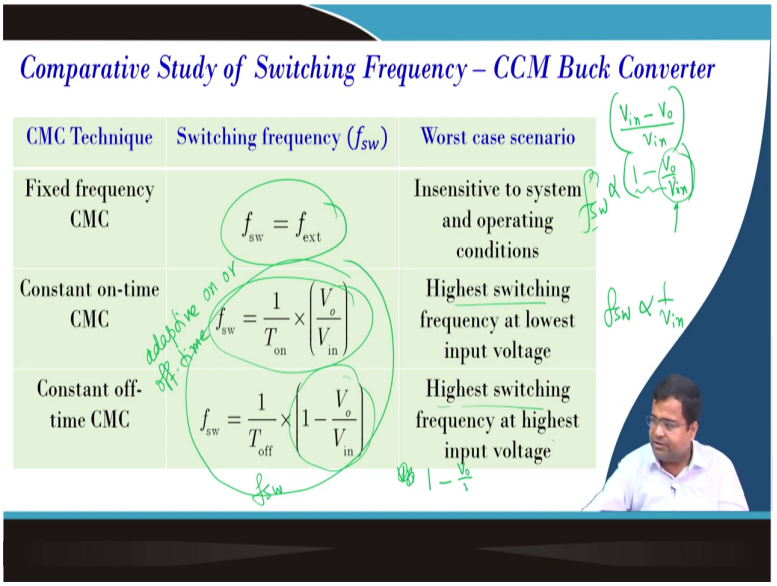

So, in summary, in fixed frequency control, we have frequency fixed, but in constant on-time current mode control we saw that frequency was increasing with decreasing input voltage and this is exactly what. So, the switching frequency is inversely proportional to Vin.

So, mathematically we have discussed. Here if you see the switching frequency it is not directly proportional, but if you take an incremental factor; that means if you take what you say you have Vin; that means if you take this guy; that means if you say 1 minus V0 by Vin. I would say Vin minus V0 by Vin.

So, this is the term we want to take we want to relate to how this input voltage is related. So, what we will get you will get; that means, you know I can take V0 out. So, if you take. So, 1 minus V0 by Vin, and; that means if you see switching frequency is proportional to this factor; that means if Vin is decreasing this guy will increase and this effect will decrease. So, the switching frequency decrease. So, the switching frequency. So, it will be highest at the highest input voltage, but at the lowest input will be the lowest. So, here it will be highest at the lowest input voltage.

But all these problems can be overcome if we can adapt you can make adaptive on or off time based on whether it is a constant on-time control or off-time control and in digital it is very easy even if we do not need a whole lot of digital control for the outer voltage inner curve. They can be purely analog, but your timing signal will be the digital domain where you can play with this adaptation in timing parameters. So, that you can maintain the switching frequency.

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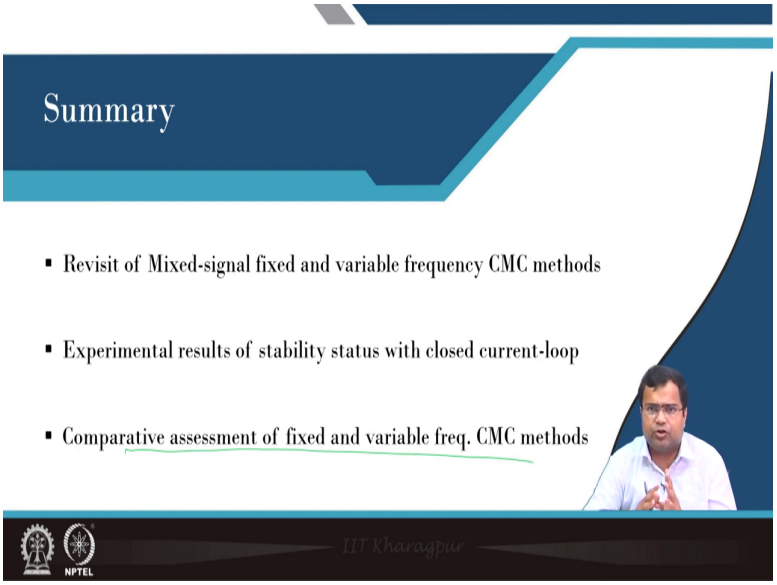

So, in summary, we have discussed various both mixed-signal fixed frequency and variable frequency control we have revisited. We have shown some experimental results regarding their stability status for fixed frequency we have considered ramp compensation and we saw that the ramp compensation was not enough when you further increase the duty ratio. Then you need to increase ramp composition and that may slowly take the current mode control to become voltage mode control by adding more and more ramps.

But we saw that in the case of constant on time off time there is no problem with the current of stability and we also saw some comparative assessment, but they have a problem in terms of frequency variation, which can be anticipated by the means of timing adaptation. So; that means, we have shown some competitive assessment between fixed frequency and variable frequency current mode control. That is it for today.

Thank you very much.