Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 10
Reference Design of an FPGA-based Digitally Current Mode Controlled Buck Converter
Lecture - 97
FPGA Implementation of Constant On/off-Time Mixed-Signal CMC

Welcome. In this lecture, we are going to talk about the FPGA implementation of constant on-off-time mixed signal current mode control. And we will also demonstrate a short video live demonstration of our hardware prototype.

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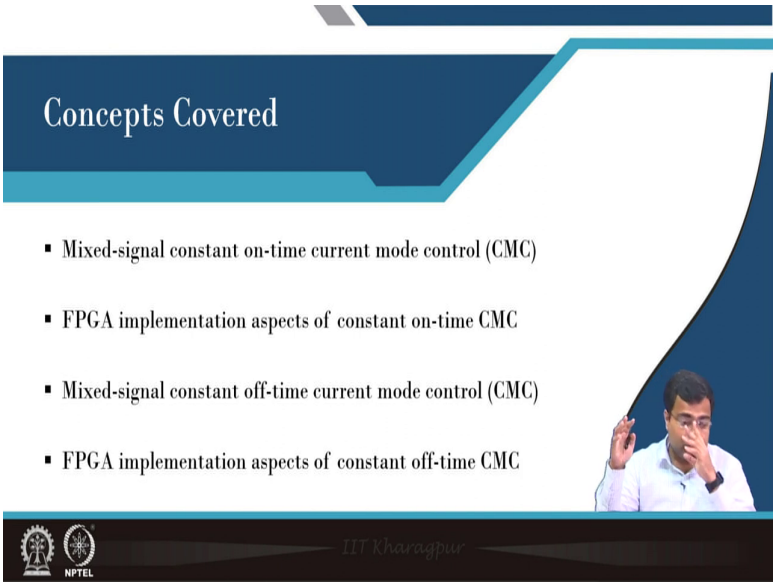

So, here we are we will first talk about the mixed signal on time current mode control and FPGA implementation aspect of the same. Then we will talk about mixed signal off-time constant off-time current mode control and then the FPGA implementation aspect.

So, here both cases we will be considering fixed current differences. So, we are not going to close the loop and then we want just want to justify what is the current loop stability aspect using experimental results.

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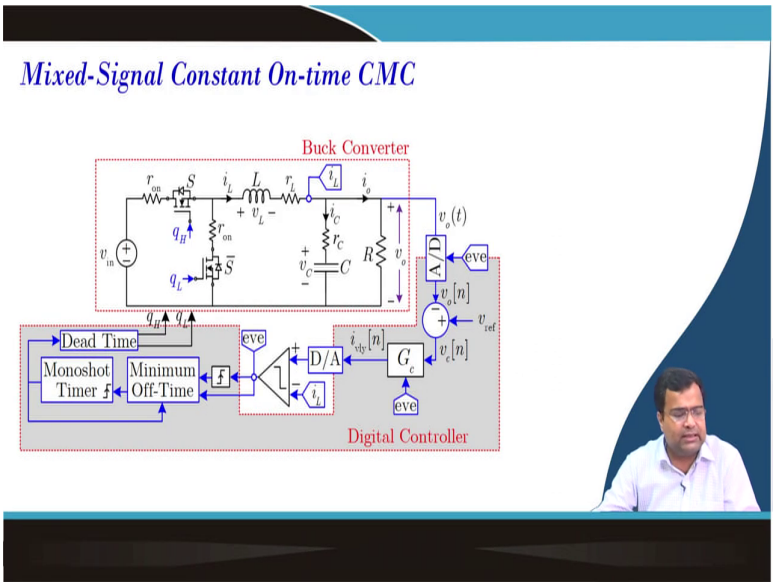

So, if we talk about mixed signal current mode control this we have discussed I think in week 2 in the architecture as well as week 3 where we have made the MATLAB simulation.

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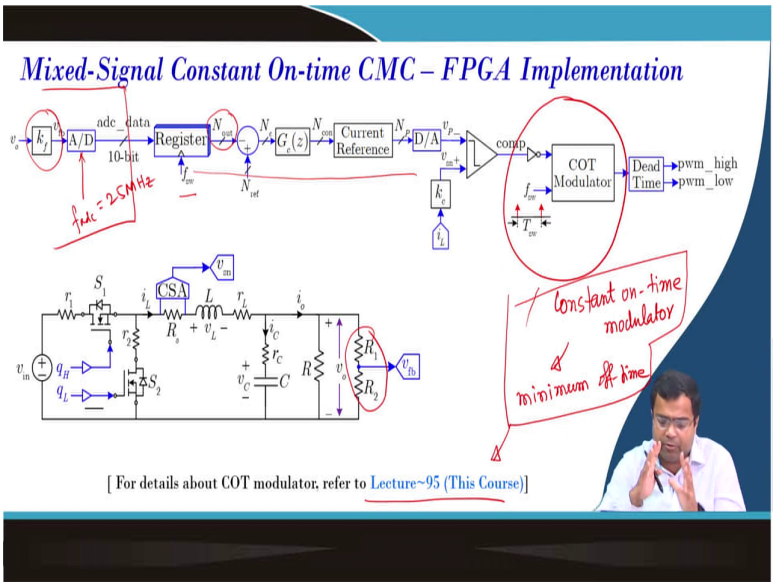

And if we consider this DC-DC converter in the buck converter then we have discussed that this part is our ADC voltage feedback gain, because we have this resistive divider. Then ADC data is sent here we are using an ADC clock which is a 25 megahertz clock. This is a very high-frequency clock I would say.

But you can reduce it. And we are taking the data at the rate of the switching frequency; that means, at every edge of the switching frequency we are capturing the data and that resistor output is our output N. This thing we have explained in the context of fixed frequency current mode control. All these terms are common. The D to A all these things are common.

If you go to I think lecture numbers 75 and 76, I think 75, and 76 we have explained peak current mode mixed signal current mode control where we have used fixed frequency control. Here the difference is that will come. So, this will be different. Sorry, the only difference will be coming here. So, here is the difference.

So, in fixed frequency peak current mode control, we have used here trailing edge modulator, but now here we are using a constant on-time modulation. The constant on-time modulator in which we are also considering minimum off time is ok. Now, how does it work? And if you go to our lecture number 95, we have already discussed in detail, how to in implement constant on time with minimum off time using Verilog code. And then we have also you know synthesized using for FPGA prototyping ok. So, we have already discussed this in lecture number 95.

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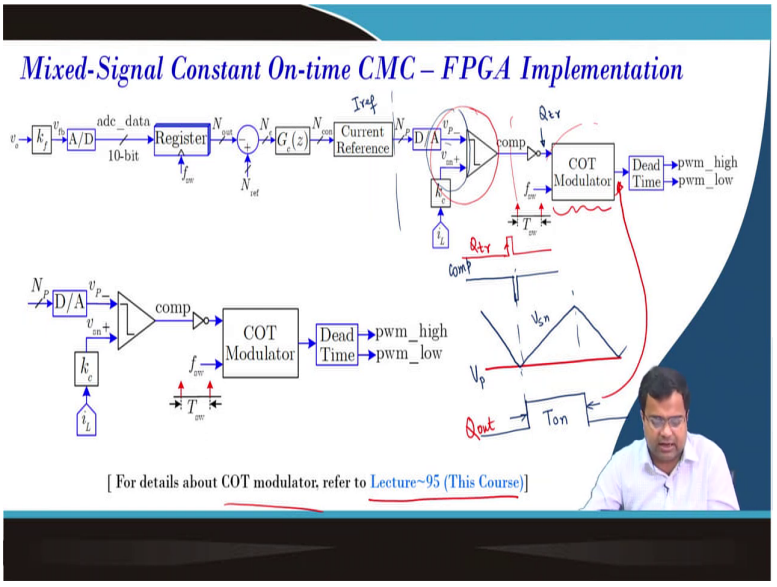

So, what is in this case I mean if you consider the constant on-time control. How does it work? So, suppose we have this current reference and this is our inductor current. When it hit the current reference then the on-time is started. Once the on time is elapsed then starts falling and this is the methodology.

So, here your on time will be triggered, it will remain on and so on and this is our Ton duration. This is our Iref. So, we are using a fixed current reference; that means, here we may not close we are not going to close the loop. So, we are using a fixed value; that means, we are using Iref to be a fixed value and which is going as a data input to the DAC. And this is my Iref. Next what will happen?

Since our comparator is set like this; that means, whenever this is my Vsense and this is my let us say we are talking about the comparator symbol here. Then what is our this is our Vp. Whenever Vsense is try to go below; that means, if you see that Vsense is higher than Vp then your comparator will be turned on the right.

So, as long as Vsense is higher than Vp the comparator is always on, but when Vp goes below Vsn then this comparator should be off. So, we are trying to detect here; that means, what is the comp output? If you take the comp output the comp output since Vp Vsn is always above Vp. So, comp output is always high ok. It will go low for a very short duration then come back.

So, this is a comp output. That is why we have inverted. So, this is like your you can say Qtr, then what is Qtr? If I take the inverted logic, it will be just this thing and take ok and this is what we expect for triggering the mono shot timer; that means because we cannot change the hardware whatever is set the comparator positive and negative terminal which can be used to implement constant off time, constant on-time fixed frequency anything.

So, only we have to adjust the logic of the comparator output. So, we have said this is my Qtr. So, whenever Qtr goes high then the mono shot timer will be triggered. And we have already discussed the inside block of the control on the time modulator and it also has a minimum off time this is your Qout and which is going to the input to the dead time circuit and dead time will generate your PWM high and low.

And we have discussed the synthesis of constant nt on-time modulator in lecture number 95. So, one can go into detail about that 95 lecture.

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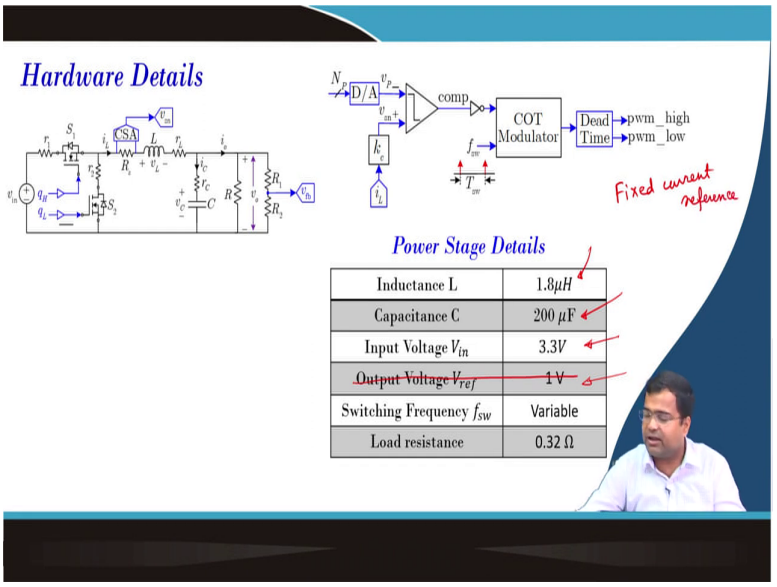

So, now we are going to consider some hardware results. So, in this hardware result, we will take the power stage and we have an inductor this thing we have discussed multiple times. The input voltage will vary to show, the output voltage we are using as a fixed reference.

So, there is no point output voltage, because it may not be regulated we are using a fixed current reference, fixed current reference. And we will discuss what is the exact value of the current reference.

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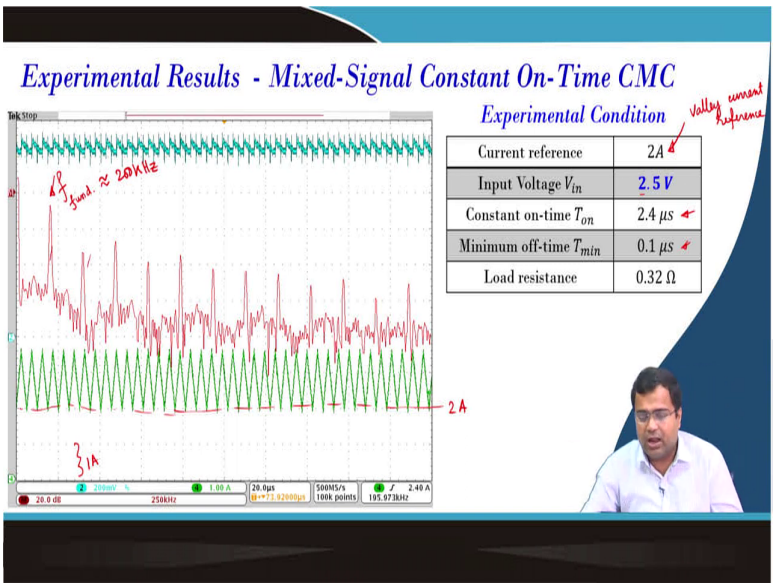

So, if we now go to the next, first we are taking the current reference to 2 ampere because it is a valley current. It is a valley current reference because it is constant on-time control and this is the experimental result.

So, you can see this is 1 ampere. So, this line is sort of it is like 2 ampere. So, the valley current and because there is a cooperated delay. Let us say it may cross a little bit, but at 2.5 volt input and we have set a constant on-time Ton to be 2.4 microsecond and we have set a minimum off time of 100 nanosecond which is 0.1 microsecond.

So, it is clear from here. That we have set the 2.4 in such a way if the voltage goes to 1 volt or it is just above, it is very close to 250 kilohertz sorry 200 kilohertz. This is this peak I will say this fundamental component is like your fundamental yours will be approximately equal to 200 kilo it is not exactly, but approximately 200 kilohertz. Nevertheless, it is perfectly stable because you can see the fundamental harmonics coming.

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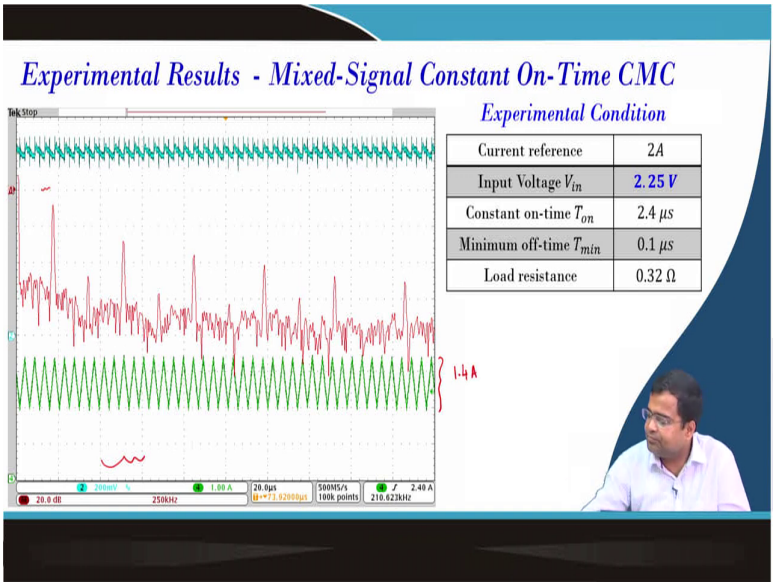

Now, we decrease the input voltage from 2, 2.5 to 2.25. What you will find? That your valley currents remain the same, and input voltage has decreased, but what has changed? You see the frequency is slightly changing because it is no longer 200 kilohertz. It has slightly because this division in the frequency is 250.

So, each division will be 50. So, it is just slightly above 200 kilohertz. Maybe 210 or something like that, but it is perfectly stable.

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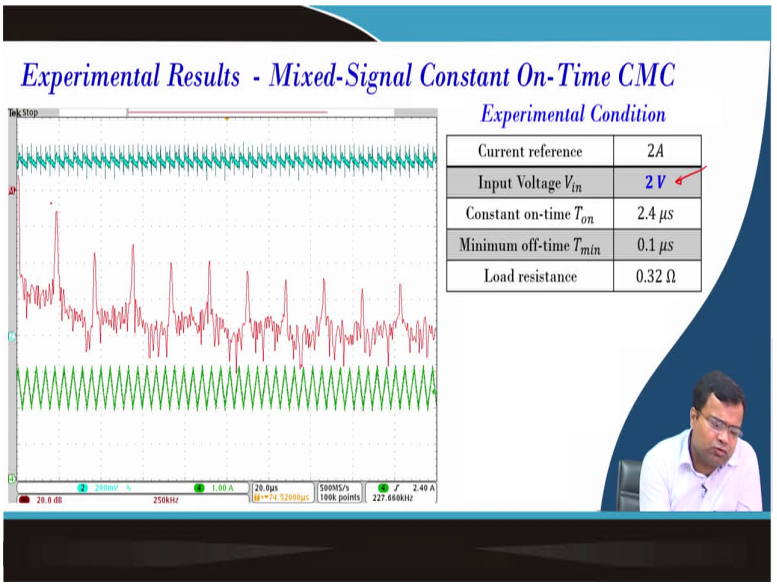

And then we have further decreased to 2 volt; that means, your input voltage is further reduced, but the duty ratio is large, but you see the frequency is now slowly approaching 250 kilohertz.

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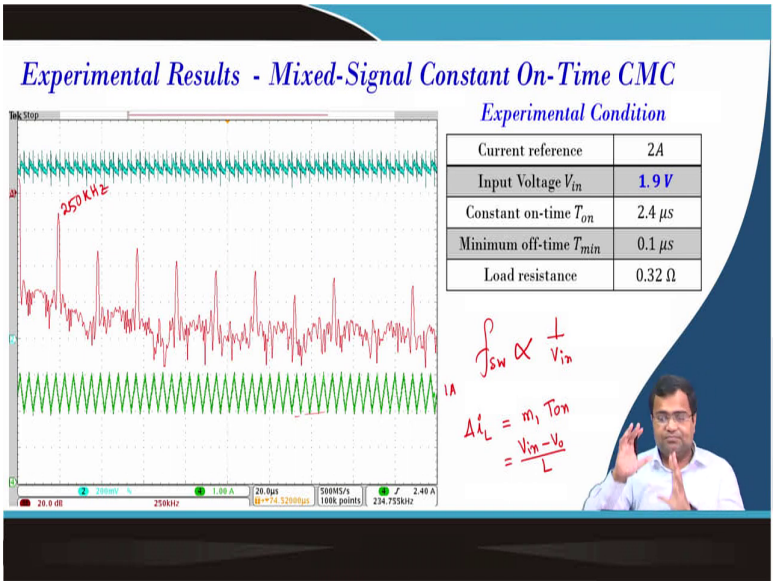

And if you make it at 1.9, it is more or less 250 kilohertz is your switching frequency.

This means we found the switching frequency is sort of inversely proportional to Vin; that means if Vin decreases switching frequency increases, but in all cases, reference valley

current remains the same, but the switching frequency is changing and as a result, ripple is changing here, because it is if you remember what is the current ripple under constant on time it is m1 into Ton, Ton is fixed.

What is m1? Vin minus V0 by L. Since, we kept the valley current the same and we have certain load resistance. So, naturally, as you know the ripple will vary because the output is decreasing. So, ripple will if the output decreases then the ripple will decrease and that is what.

So, if you compare the first ripple. So, this is the highest ripple. You can see the ripple is almost around this 1 ampere it is roughly around 1.4 ampere current ripple. But here it is almost 1 ampere. So, the ripple is decreasing.

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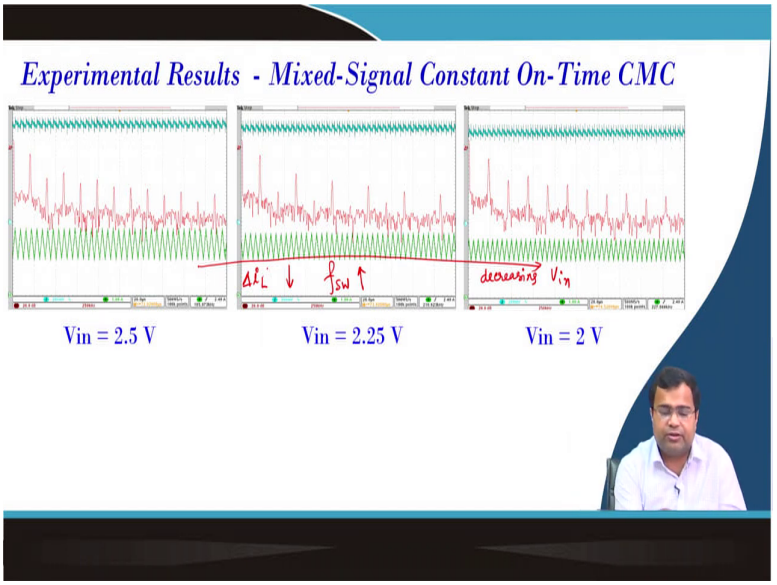

Now, we want to compare 2.5 volt 2.2 volt, and 2.2 volt. So, you see the current ripple. So, the delta is delta iL decreasing in this axis if the input voltage and since delta L is decreasing. So, the frequency is also increasing, and what is decreasing? So, here input voltage is decreasing.

So, it is a decreasing Vin ok, decreasing Vin. So, in this direction, the input voltage is decreasing, but in all cases, it is stable since we are using only a valley current fixed reference and no closed-loop control. So, that is why you can see the voltage regulation is affected.

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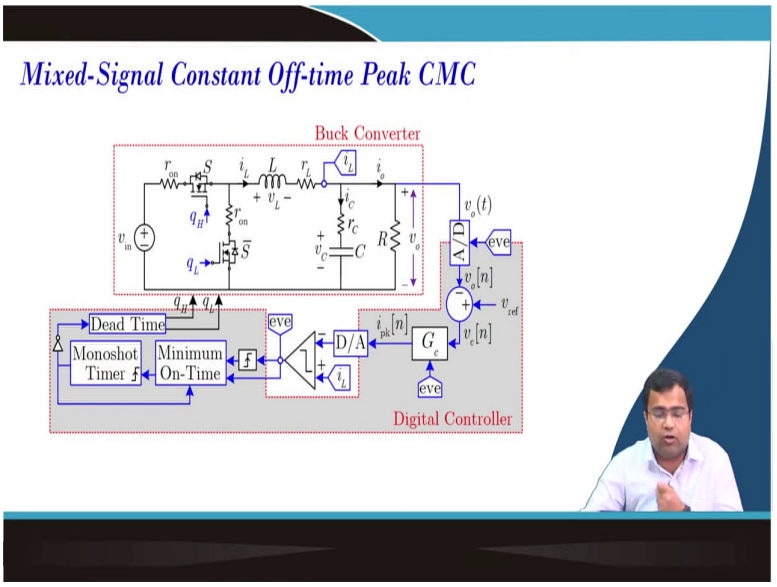

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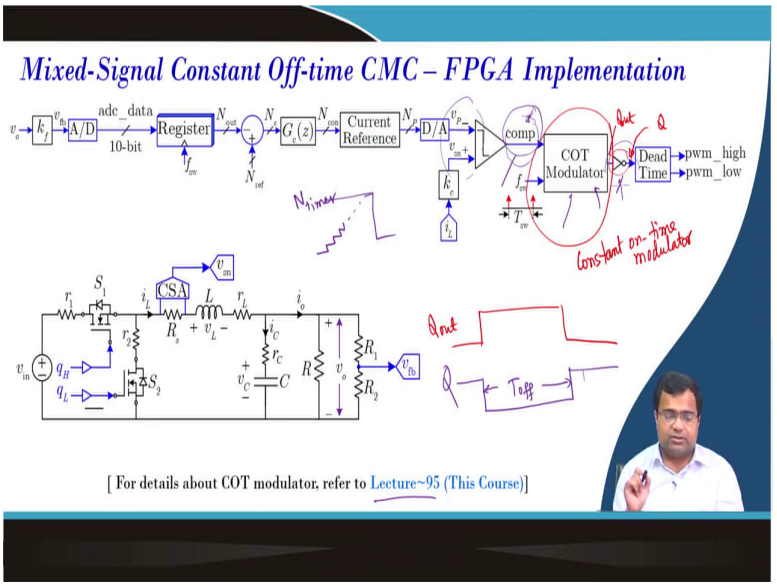

Now, if I go to constant off-time control then we know about this architecture which is explained in week 2 as well as week 3 in MATLAB simulation.

Then again if we go you will find that there is a current reference. So, this is similar to a peak current mode control, but it is a peak current mode control, but instead of fixed frequency you have a constant modulator. Now, here we are using a constant on-time modulator only. Constant on-time modulator which has a minimum off time, but we are inverting the logic.

So; that means if this output is Qout; that means, Qout goes high. So, we want this Q. So, our Q should be; what is the Q? So, this Q should be high it will be low. And this is our off time. So; that means, whatever modulator we are setting on time the time duration is nothing but the constant off time ok. And if we maintain a minimum off the time it will become a minimum on time or constant off time.

So, everything is perfect. And earlier we saw we took the inverted logic of comp and directly pass Q, but here it is just the opposite. We have to take the comp output directly as the input because our polarity remains the same, but we have inverted the output logic, but we are using the same modulator. So, that is the beauty; that means, you know the same modulator using.

So, if you want to move from constant on time to constant off time in your hardware in your digital circuit, you have to just complement this signal and this signal. And you may upload the parameter of the timing parameter accordingly because in lecture number 95 we have discussed how; that means, to generate this timing parameter, we need what? We need a timer. So, this value if you update then accordingly your on-time and off-time can be adjusted in real-time because it is just you update the value in the counter,

So; that means, it will happen immediately and you can reconfigure from constant on time to constant off time just by changing this comp you directly pass and invert this logic and in constant on time we will invert comp, but pass this logic that is it.

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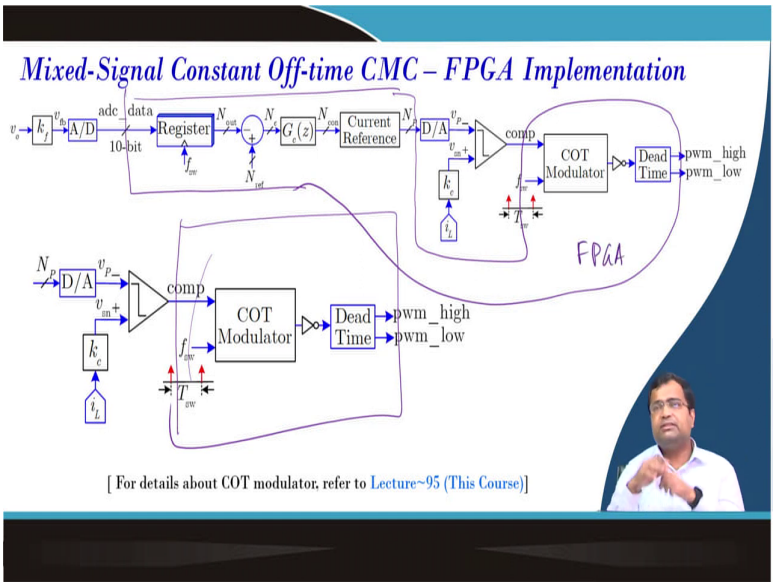

So, here again, you know if you recall the same logic I mean we are talking about and we have discussed in lecture number 95.

So, this part will be in our FPGA this will be coming outside here also this whole part will be FPGA. So, this part then this part this whole part will be in the FPGA. So, this will be in FPGA and we will synthesize using Verilog.

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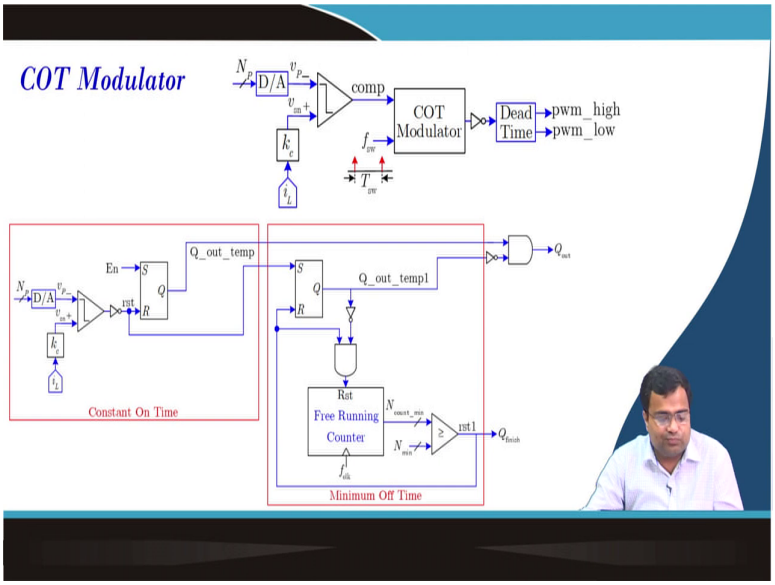

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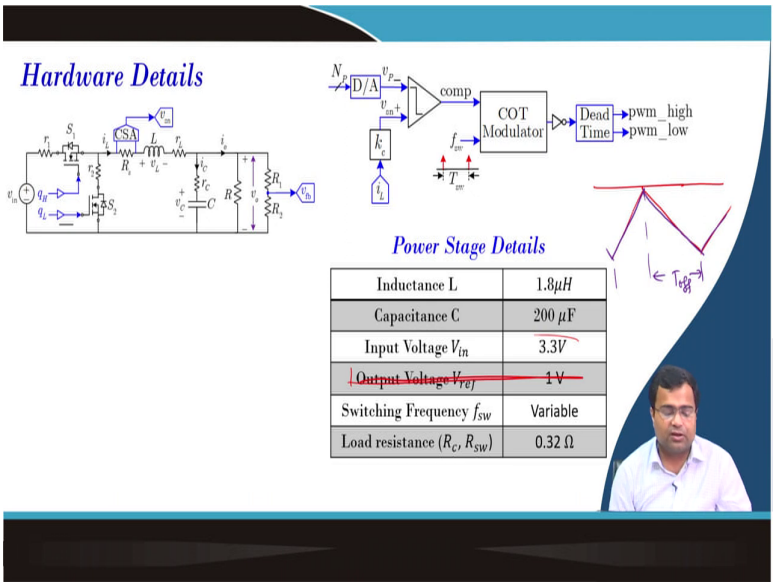

So, now we are going to show hardware results. So, again this hardware result we have considered the same converter, but the input voltage will vary.

We are not going to regulate the output voltage, because we are setting a fixed current reference. And it is constant off-time control. So, if I show the waveform this is constant off-time control. So, then what we are doing compared to them; so, this is ours. So, we are fixing this time to be off to be fixed ok.

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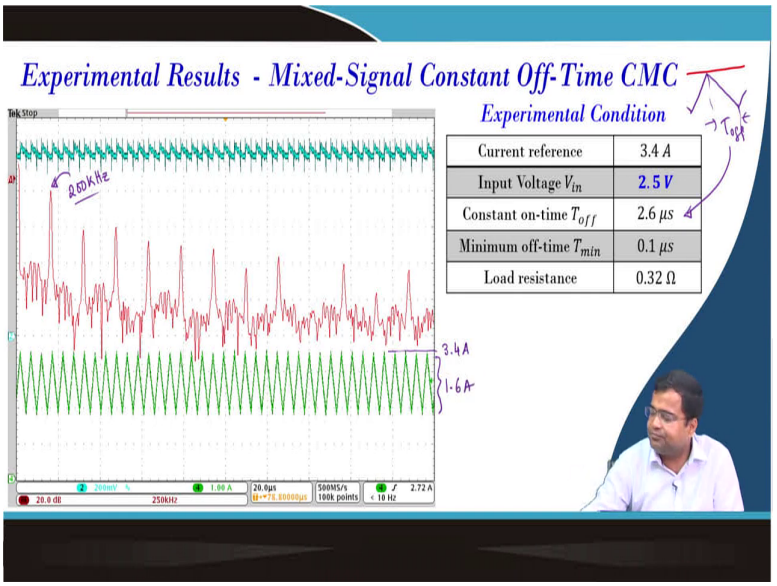

Now, we are going to show the experimental result using mixed-signal constant off-time control. And you know this is a peak current mode control, where we are fixing the peak current and this is our peak current mode control.

And we are fixing this constant off-time Toff and we are considering Toff to be 2.6 microsecond. Now, this is an experimental result with 2.5 volt input and this peak current is 3.4 ampere you will see the stable perfect behavior and it is more or less coming to be around 200 kilohertz. So, it is coming more or less at 200 kilohertz.

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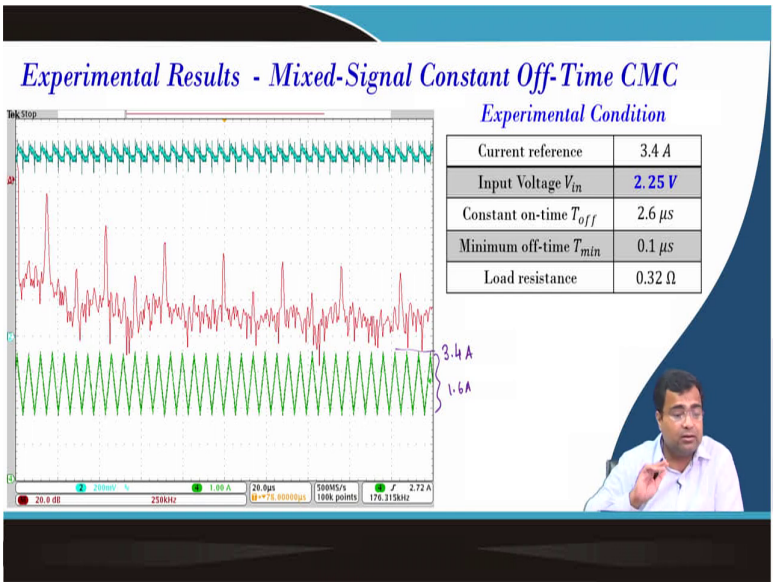

Now, if we decrease the input voltage to 2.5, it remains at 3.4 amperes and interestingly you will find that this ripple remains the same, because if you go here if you see the ripple it is around how much it is coming. Around 1 I think 6 ampere. Here also you will get 1.6 ampere. Ripple remains the same, but what you will find here the peak was coming in the second dot.

Now, here we will see. It is slowly shifting, but not pure and perfectly visible.

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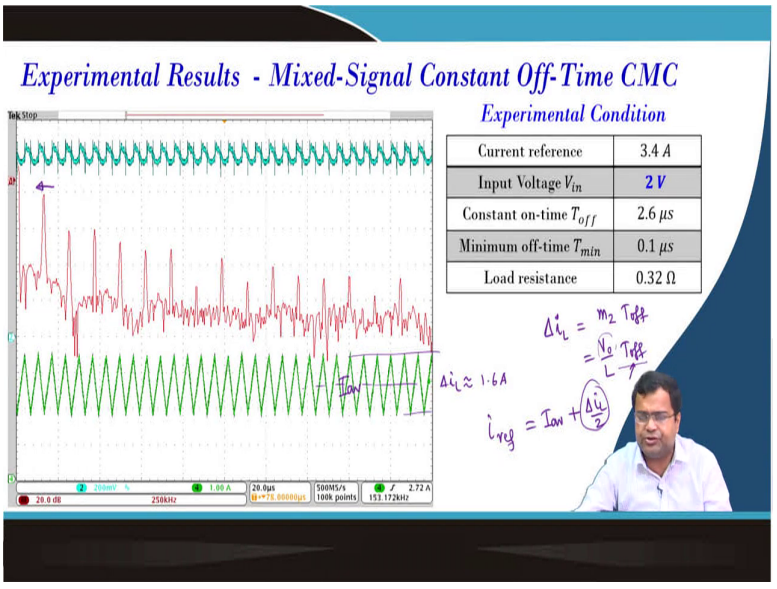

But, if you go next this peak is shifting towards this side, which means the frequency is decreasing; that means because we have further decreased the input voltage. It was 2.5 then, but it is perfectly stable, but if you go to 2 volt it is also perfectly stable peak current reference same and the current ripple also remains more or less more or less 1.6 ampere.

But the frequency is decreasing. So, what we learn is if the output voltage is more or less maintained, what is delta Il? It is nothing but m2 into Toff and what is m2? It is V0 by L into Toff. So, if you maintain the fixed current difference and if your off-time is fixed inductor is fixed then it will try to regulate the output voltage even though the input voltage is changing. So, that is the beautiful thing about constant off-time control.

Because if you are going for a precise current regulation you know and you have let us say a driving-led driver or you are talking about a battery charger. So, you can just use a constant off-time control if you want to set it. Suppose this is my desired current reference average. So, I will set the reference current to be I average plus delta iL by 2. Since the delta is by 2 depends on your what is your desired output voltage and you know the inductor value.

So, you accordingly set the off time and then you can precisely control this. Suppose you want to vary you know because you need to regulate some switching frequency then you have to accordingly adjust the reference current. So, these things can be adjusted in the digital domain very effectively, and the beautiful thing you can have a very wide duty ratio operation.

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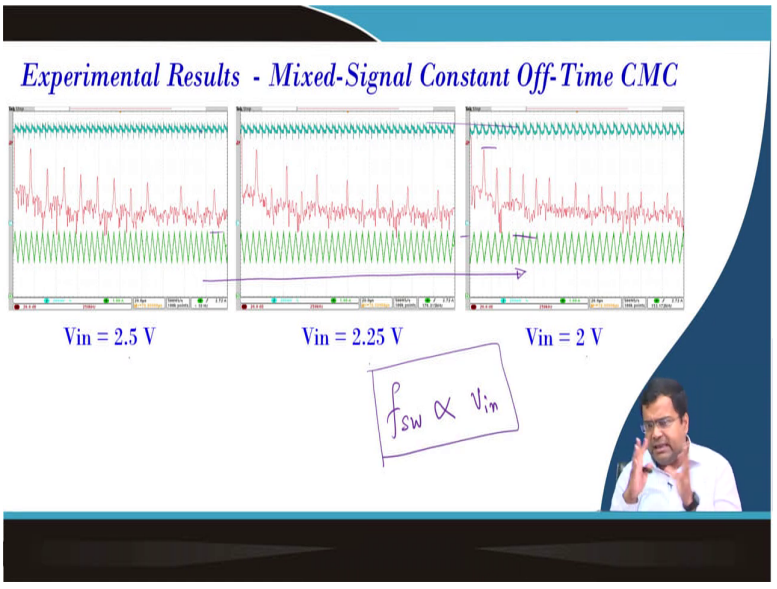

Because if you see from 2.5 to 2.25 and 2 volt 50 percent your current loop is perfectly stable. Since we are using constant off-time control where the ripple current is more or less the same. You see the 3 cases. So, the output voltage you can see they are more or less regulated.

Even though we have not closed the outer loop it is just a peak current reference. The outer loop is open, but this was not the case of constant on time which will be the case of constant on time for a boost converter or for a buck converter for constant off time the output voltage will be more or less regulated indirectly even without closing the loop.

But you still need feedback to know disturbance rejection, even accurate current regulation, but here it will make your integrator job very easy and it is stable for all periodic behavior, but what is the drawback you can see that for decreasing input voltage the switching frequency is shifting. So, this guy is shifting and that is why you know if we when go to the comparative study we will see what is the impact.

That means, in the case of switching frequency is proportional to some way input voltage; that means, the input voltage decreases switching frequency decreases. It may not be linearly proportional, but in the incremental sense, they have some linear relationship.

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So, now, we will we are going to consider a live demonstration of a hardware implementation of constant on-off time control ah, mixed-signal current mode control. Now, we are going to show mixed signal current mode control constant on time as well as constant off-time control.

So, in this program you know I have already demonstrated the process of dumping the code. So, I am not going to show it again. This code consists of both because we have already demonstrated constant on-time modulator everything in detail. So, here we are using a current reference fixed; that means, the only closed inner current loop, the outer loop is open.

So, we are using 2 configurations. In the class, you know in the lecture we have demonstrated that one is constant on time where we are using a valley current difference of 2 ampere. Another is a constant off time where you are using a peak current reference of 3.4 ampere. And first, this code is made whereby by changing the switch position we can move from constant on time to off time. So, we do not need to run the code once again.

So, this code we have already run we have generated the program file and we have dumped this code into this FPGA. Now, we are directly going to the hardware setup and we want to demonstrate whatever we have studied in today's class.

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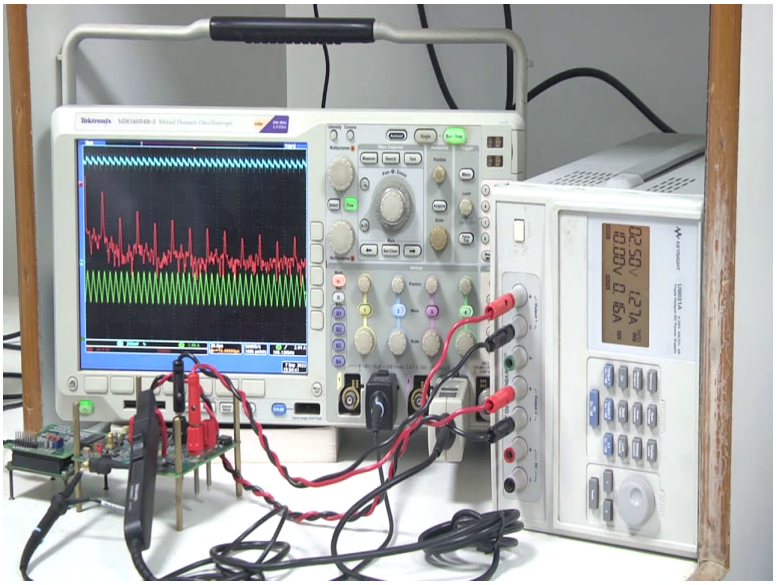

First I am turning on this power supply. So, this is the main power supply and we are starting with the 2.5 volt input that we have demonstrated. So, here you can see that we are first talking about constant on-time valley current mode control; that means, your mixed signal

current mode control where the current loop is closed and we are using a valley current reference of 2 amperes and you can see that this division is 1 ampere. So, this 2 ampere is the valley current. So, we are fixing the valley current.

Now, we are changing the input voltage. At 2.5 volts you can see this frequency is more or less 200 kilohertz because the first peak is coming from the fundamental component here. This is the average current that the harmonics are coming. Now, once we go to 2.25. You know 2.25 input voltage you can see it is perfectly stable and the frequency is slowly moving towards this.

That means if I show the process of movement 2.5 you know slowly that the peak is shifting. So, you can see the peak is shifting to 2 this is 2.5 and this 2.5 the peak is coming slightly. It is now coming in between 200 to 250 kilohertz. So, maybe it is around 210 ten kilohertz or so, and, but it is perfectly stable because the duty ratio is quite large.

And you can see, but what another point you will see the ripple has got reduced. So, as a result, the frequency is increasing. If we further decrease; that means, from 2.25 to 2.2 which we have demonstrated in class. We are now coming to 2. So, at 2 volt input now the frequency is coming close to almost 250 kilohertz. It is around 240 and you can see it is perfectly stable the valley current is maintained.

But then a ripple is changing, because we have learned in valley current mode control or constant on-time control that for a buck converter if you decrease the input voltage the ripple current reduces, and your switching frequency increases. So, the switching frequency is inversely proportional to the input voltage, and as a result, the peak is shifting, but it is perfectly stable if you go to 1.9.

So, it is also perfectly stable and frequency is further increased. So, now, it becomes to 250 kilohertz is the effective switching frequency. So, what we learned there is in constant on-time current mode control the valley current is fixed and the current loop is perfectly stable irrespective of the duty ratio, but the frequency is varying as well as the ripple is varying.

Now, under the same condition, we are moving to constant off-time control. And this is a switch if you change this button now it moves to 2 points constant off time, where we have maintained the peak current reference and this peak current is maintained at 3.4 ampere.

Now, we are starting with 1.9 volt input. That is the least input voltage and you can see this condition when you switch from constant to time.

That constant on time the frequency effectively was roughly around 250 kilohertz, but when you go to constant off time the frequency now has become, because it is 50 kilohertz. So, it is like 150 kilohertz; that means, it is lower than 200 kilohertz which is the nominal frequency that you set, but the current loop is perfectly stable and there is a large duty ratio there is no instability peak current is fixed.

Now, you are increasing the input voltage to 2 volt. So, we get to 1.9 volt to 2 volt the current loop is still stable, but the frequency is now slowly increasing, but another point you know is when you go to 2.25; that means, further increasing 2.25 current loop is perfectly stable frequency has now reached to 200 kilohertz close to that.

But, you will also find the current ripple is remain more or less the same because if you talk about constant off time since the off time is fixed and thus falling slope is V0 by L and since the V0 is more or less maintained. So, the ripple is maintained. So, the ripple is not changing that is why we discussed that this will be a very good example of you know led driver or etcetera where you want a precise current regulation.

Now, if you go to 2.5 ampere, 2.5 volt input then it is perfectly stable and the switching frequency is slowly it is slightly above you know that 250 kilohertz. So; that means, 200 kilohertz. So, maybe this may be the reason that you know we have not set it properly. So, we need to be okay; that means, this offset is slightly secret otherwise this is designed at 250 kilohertz.

So, we saw that in case of constant off time, the ripple is more or less constant if the output volt is maintained even though you vary you know input voltage, but the switching frequency varies because with higher input voltage here the switching frequency is increasing ok. This is the opposite which was the opposite for constant on-time, but for both constant on-time and off-time, you do not need any ramp compensation the current loop is perfectly stable. Now, we will move to our lecture.

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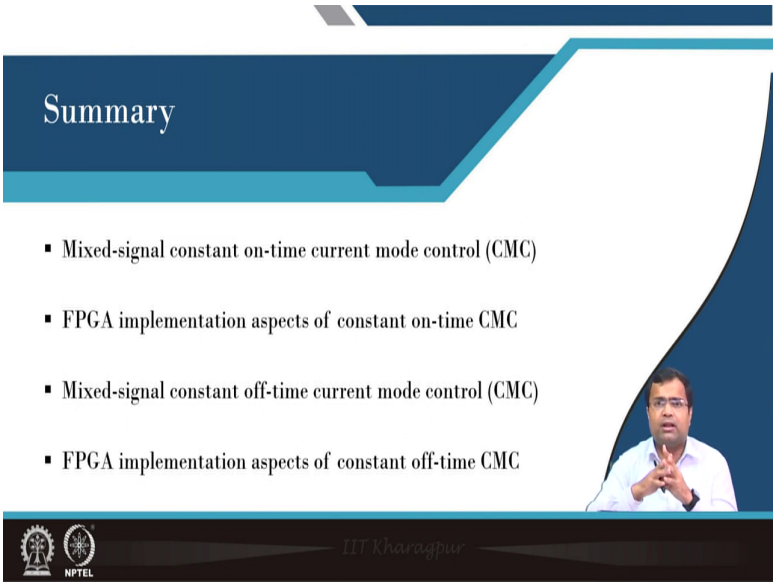

So, just now we have completed the live demonstration of mixed-signal peak current mode and valley current mode control for using constant on-time and off-time. We have shown mixed signal current mode control architecture, where the aspect of FPGA implementation then constant off-time mixed signal current mode control and their FPGA implementation.

So, in the subsequent lecture, we want to take a comparative study between all 3 control architecture and see what their benefits and drawback that is for today.

Thank you very much.