Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

Dr. Santanu Kapat
Department of Electrical Engineering
Indian Institute of Technology, Kharagpur

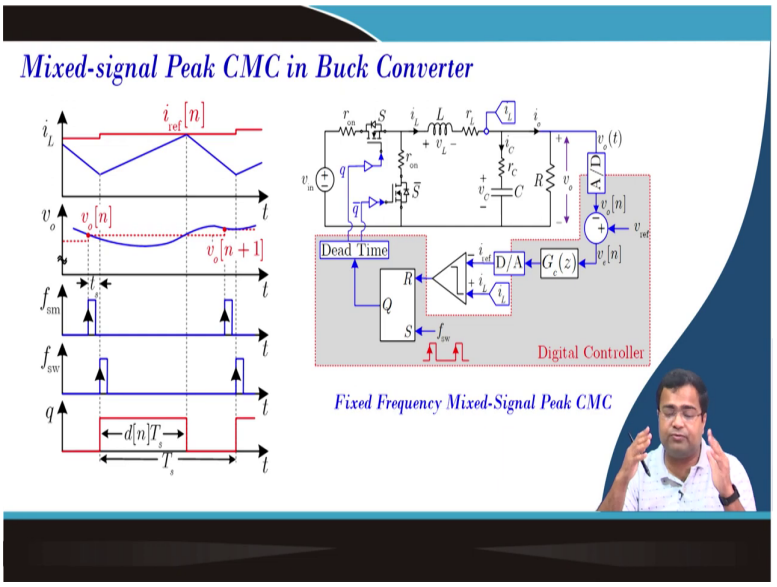
Module - 10
Steps for FPGA Prototyping of Digital Voltage Mode and Current Mode Control
Lecture - 94
Benefits of Constant Off-Time and On-Time Digital CMC Techniques

Welcome. In this lecture, we are going to talk about the Benefit of Constant Time and Time Digital Current Mode Control with some aspects of FPGA implementation.

(Refer Slide Time: 00:34)

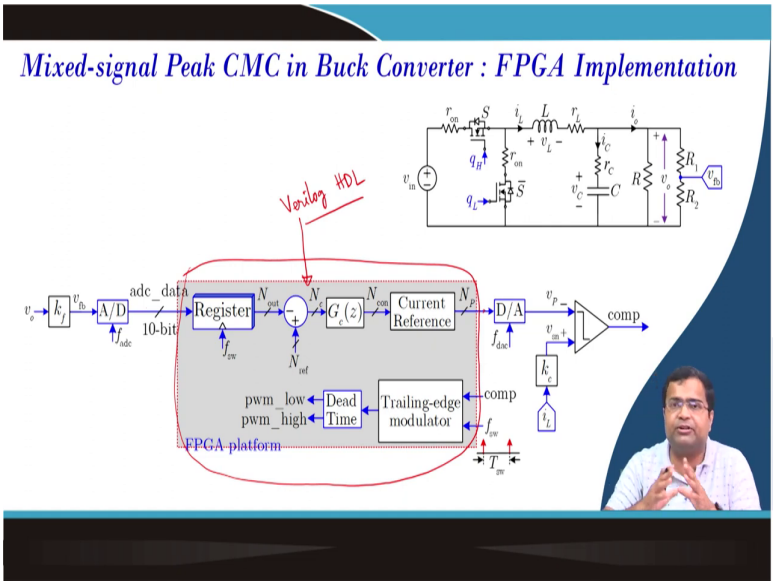
So, in this lecture we will want to discuss the current loop stability aspect in constant on-off time, mixed-signal current mode control then we will discuss some FPGA implementation aspects of on-off time mixed signal current mode control and finally, a comparative study of fixed frequency and ripple based current mode control.

(Refer Slide Time: 00:54)



So, here if we consider mixed signal peak current mode control, you know we have discussed it in multiple lectures including in lecture number 19 and we are not going to spend time here we are talking about peak current mode fixed frequency control.

(Refer Slide Time: 01:07)

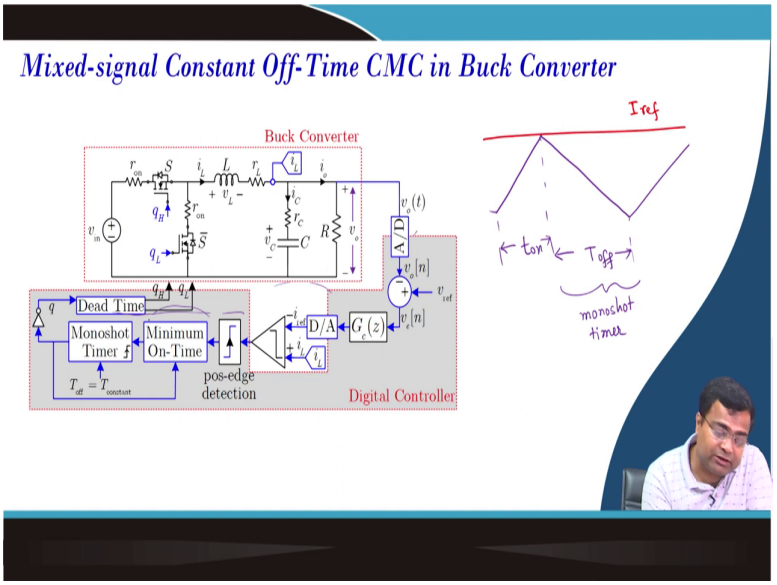


So, if we consider that peak current mode mixed signal control we have discussed the FPGA implementation; that means, this looks like we want to implement a digital controller like a digital IC and this will be sitting inside the FPGA and we are implementing using Verilog

HDL; that means, we are going to use Verilog HDL and this we are going to using the and synthesize and then it will be plugged into the FPGA device.

And it will take the data and data and then it will send the DAC data and the comparator will come out. So, this part we have discussed I think in week 8 the detailed implementation of mixed-signal current mode control.

(Refer Slide Time: 01:57)

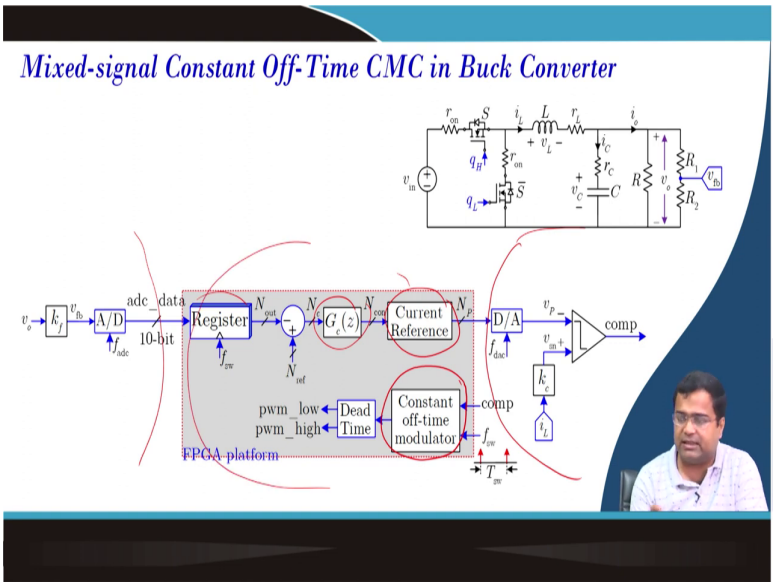


Now, if we go to constant off time. It is a peak current mode control and it is the same architecture; that means if we take the peak current difference it is the same current mode peak current mode control, but in this case, you know hereafter touching. So, compared to the fixed frequency here this time is constant.

So, off time is constant and the on-time comes out from the loop; that means, once you turn off the switch it will go to the monoshot timer. So, it will go to the monoshot timer and then the monoshot timer will once it is finished counting then it will turn on, and again the current will rise when it hit the peak current limit then it will turn off.

So, this process will continue and in this case, all implementation is the same; that means, your ADC DAC controller, the current loop is also in analog, but hereafter the comparator output we have this monoshot timer instead of latch circuit and the for fixed frequency and here we also need to consider the minimum on time.

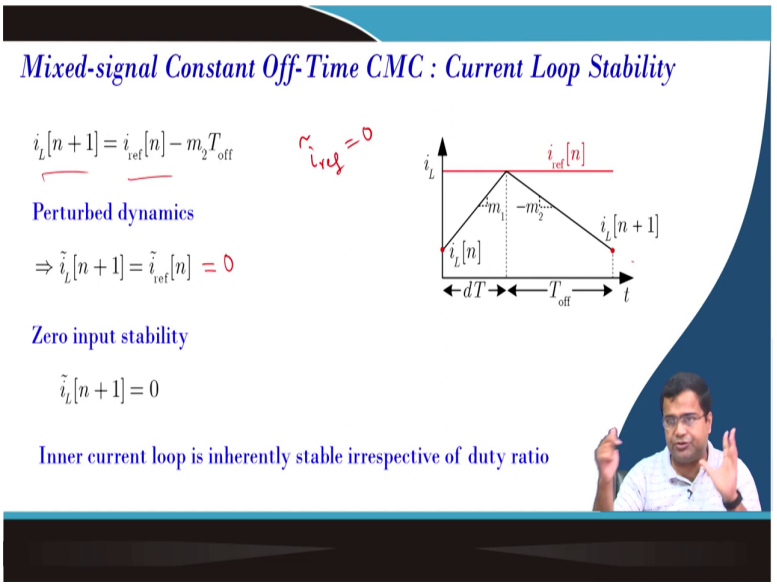
(Refer Slide Time: 03:11)



Now, we want to implement this constant off-time control using a digital platform that is FPGA. Again these blocks are common which we have discussed for mixed-signal peak current mode control fixed frequency. The only difference here and this current reference block register everything controller everything remains the same, but here the difference is the modulator.

So, here we are going to consider a constant off-time modulator and we will be discussing in the subsequent lecture details of Verilog implementation, but this is as if it looks like this whole digital circuit is implemented inside the FPGA.

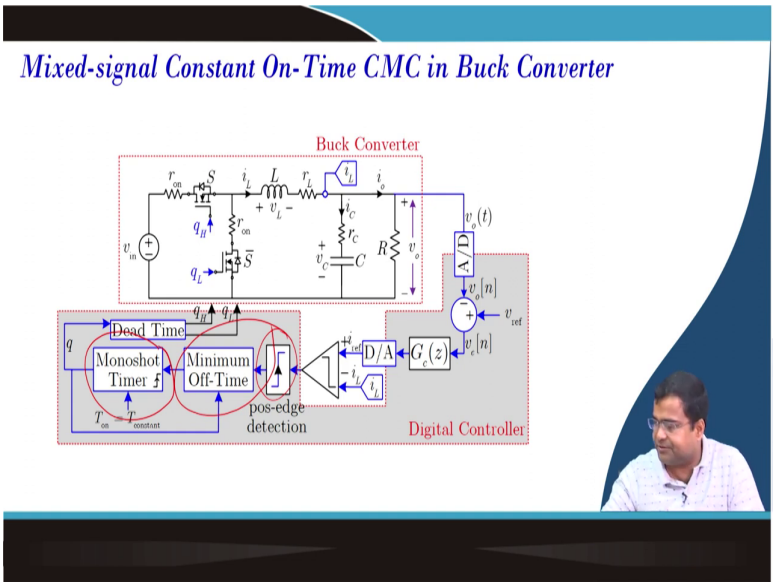
(Refer Slide Time: 03:53)



And we know from the current loop stability of the mixed signal current mode control if we write the final current. It will be in terms of Iref N and m2f, but if we do not perturb; that means, if we take Iref perturbation if we take it 0 then if you just take this current perturbation it will be the same as Iref perturbation and this will be 0. So; that means, the current loop will never become unstable when you apply a fixed current reference, but it may be unstable with a closed loop when the Iref n will come into the picture when you close the loop.

But otherwise, if we apply a fixed current reference it will never become unstable irrespective of the duty ratio. And that is what makes the inherent current loop stability very popular for you know wide duty ratio operation.

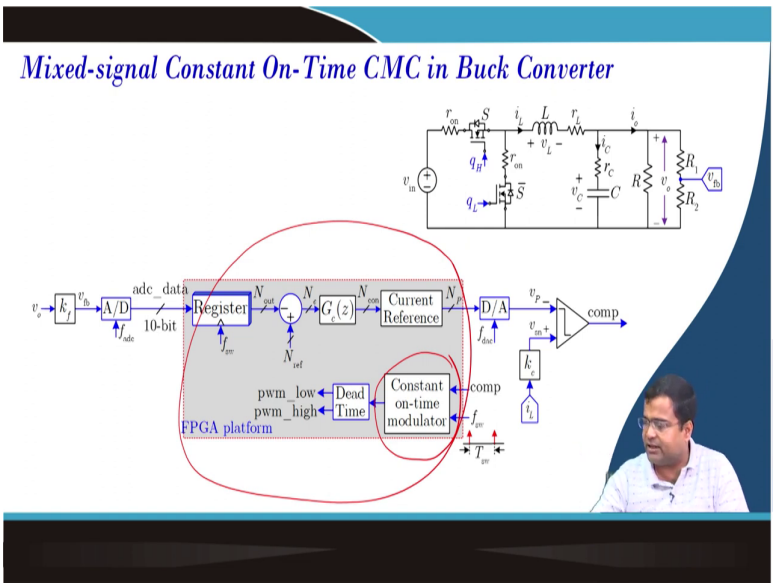
(Refer Slide Time: 04:42)



Now, if I take constant on-time mixed signal current mode control the only difference will be you are using a monoshot timer for constant on time and there is a minimum of time also we have to consider.

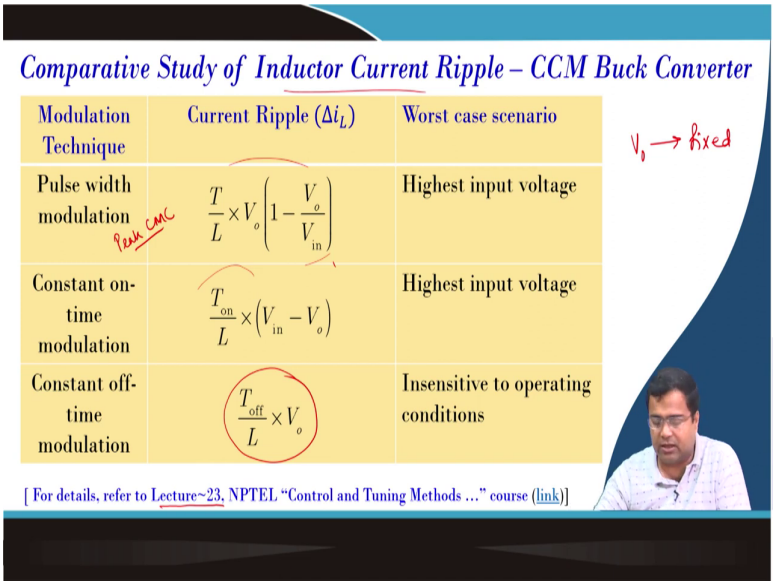
And we have to suitably consider this edge detection circuit and we will be implementing this constant on-time control for both voltage base and current base in the subsequent lecture in Verilog. So, we will hold on to a further discussion of this implementation.

(Refer Slide Time: 05:10)



Now, we can also implement this constant on-time control in using the FPGA. It will look like a digital IC, where the only difference compared to the previous one is your constant on-time modulator and we will discuss this modulator functionality in detail as well as Verilog implementation in the subsequent lecture.

(Refer Slide Time: 05:31)

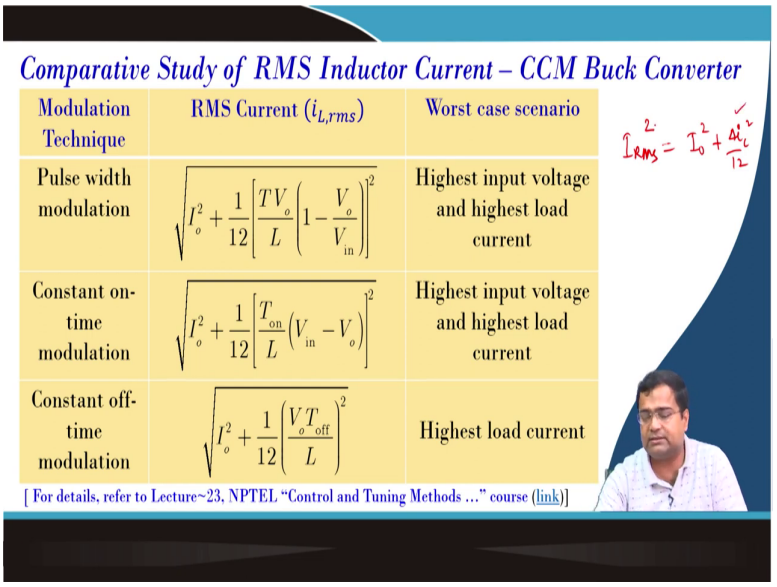


Now, if we compare what is the benefit? So, we saw that pulse width modulation; that means, if you take the peak current mode control then there is a stability aspect for a duty ratio less than 0.5 sorry greater than 0.5 you need to add a ramp, and this ramp composition also has a problem for precise current regulation ok. And it can it is also well known that it will also have an impact on the transient performance.

If we add too much ramp, but if we take constant on-time or constant off-time current mode control then there is no stability aspect, here the penalty is if you consider the current ripple under constant on-time control for a buck converter. It can be shown that the current ripple is maximum when the input voltage is maximum. Pulse width modulation also; means, any fixed frequency modulation is maximum for minimum input voltage we are talking about a voltage regulator where V0 is fixed; that means, it is with a closed loop.

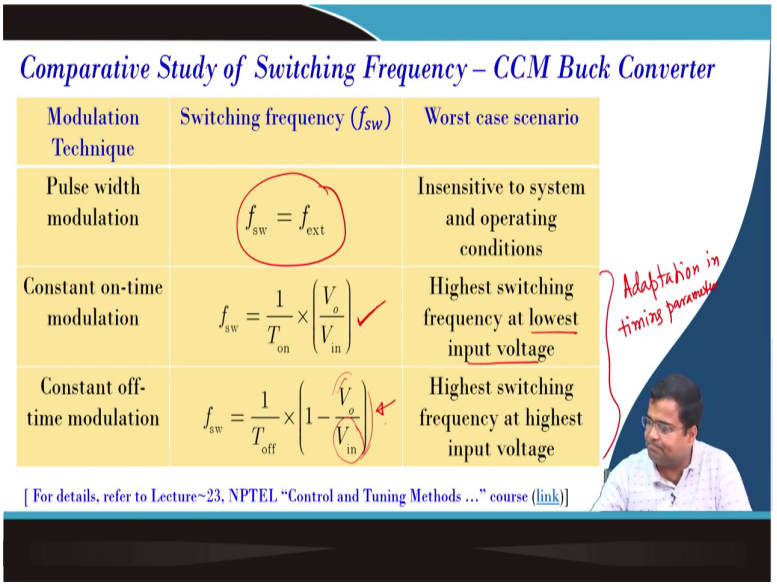
But if you take the constant of time you see it is independent of the current ripple and is insensitive to input voltage variation. And we have discussed in detail lecture number 23 in our old earlier course of NPTEL course.

(Refer Slide Time: 06:51)



If we take the RMS current it will be the same as the ripple current, because we know the RMS current for the buck converter will be if we take the square it is the loads current square plus delta i L square by 12. So, since the load current will be the same under the closed loop. So, if i L increases then RMS current will increase.

(Refer Slide Time: 07:14)



Switching frequency for fixed frequency the switching frequency is fixed, but constant on time if the switching frequency will be the highest at the lowest input voltage which will show here. For constant off time switching frequency will be highest at you know switching

frequency again will be highest at the highest input voltage condition, because this will be low and you know at the highest input voltage condition this will be smallest and this will be highest yes.

Here also here the switching frequency sorry here switching frequency is highest at the lowest input voltage condition; that means, as you decrease the input voltage switching frequency will increase, and in this condition, the switching frequency will increase if you increase the input voltage. So, in both cases, you can go for adaptation in the timing parameter that way you can make the quasi-fixed frequency or fixed frequency operation.

So, that is one of the drawbacks, but you can avoid it can do it adaptively, because you are using a digital platform and this timing adaptation is not a problem you can use all digital PLL and we will discuss some aspects in the last week of this adaptation in on time, but you can make more or less fixed frequency with and you can get the benefit of other feature in terms of stability.

(Refer Slide Time: 08:50)

So, in summary, we have discussed the current loop stability aspect in constant on-off time control it is inherently stable we have discussed FPGA implementation of constant on-off time control. And we are going to you know we have also compared their ripple parameter under fixed frequency and ripple-based control and in the subsequent lecture we will show an experimental case study of fixed frequency versus this ripple-based control their stability and this impact and that will be demonstrated the subsequent lecture that is it for today.

Thank you very much.