Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

Dr. Santanu Kapat
Department of Electrical Engineering
Indian Institute of Technology, Kharagpur

Module - 10
Steps for FPGA Prototyping of Digital Voltage Mode and Current Mode Control
Lecture - 93
Instability in Digital CMC and Ramp Compensation with Experimental Results

Welcome to this lecture we are going to talk about current loop stability in Digital Current Mode Control then what the cause of current loop Instability and how to stabilize the current loop using Ramp Compensation with Experimental Results.

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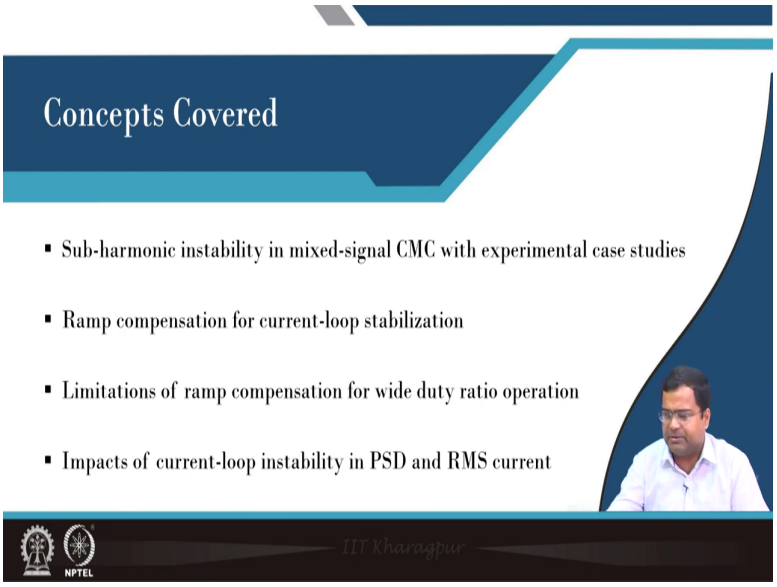

So, we will first you know show the subharmonic instability in mixed signal current mode control where we want to keep a fixed current reference and we will show some experimental case studies. There we will also show ramp compensation for current loop stabilization and what are the limitation of ramp compensation wide duty operation, and what is the impact of current loop instability on power spectral density, as well as the RMS parameter.

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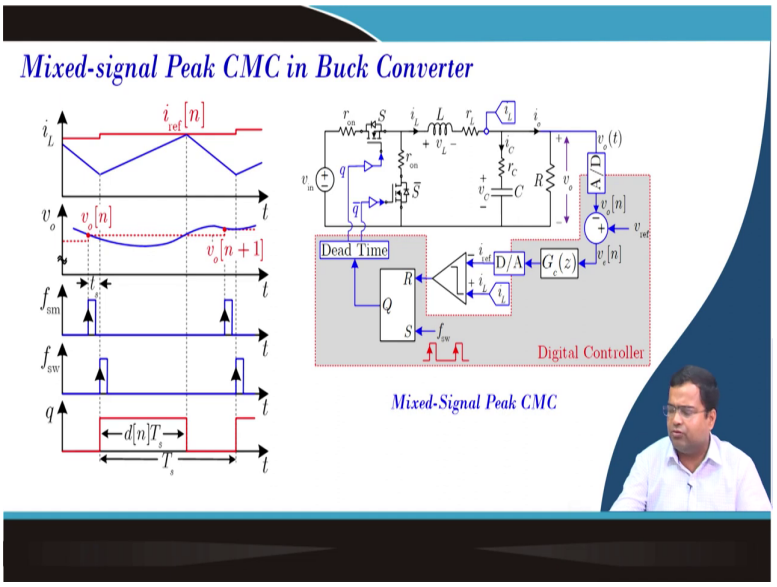

So, in mixed-signal current mode control, we are all familiar with this current mode control architecture and we have explained it multiple times. So, I am not going to explain again.

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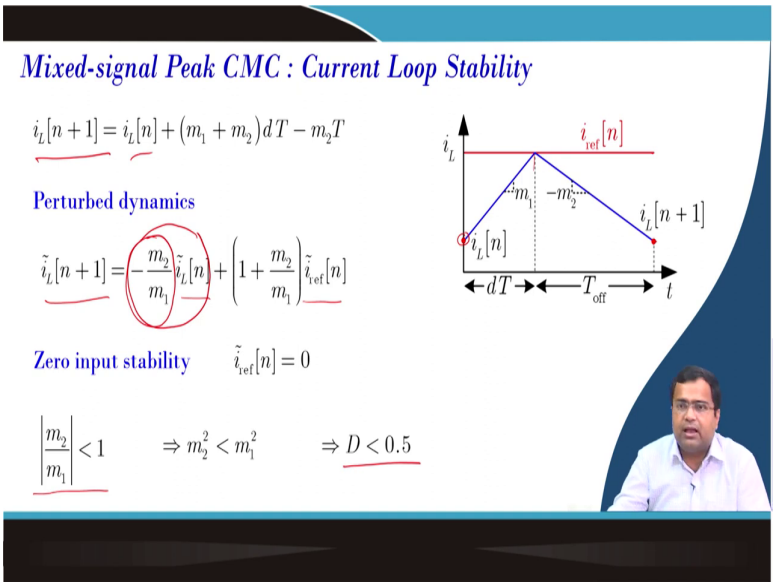

And if you recall you know I think we discussed in week 5 where we considered the current loop stability using a discrete-time model. So, I just want to summarize if you write the full equation of i L n plus 1 which is this current in terms of i L n and duty ratio.

Then if you get the perturbed dynamics; that means, you can get only the perturbed dynamics the i L n perturbation will be a function of i L perturbation and also a function of i ref perturbation ok. But if we do not perturb the reference current; that means, we are talking about the fixed reference current where only the inner closed inner loop is closed and we are using a fixed current reference then i ref perturbation is 0.

Then only this term will remain and stabilize this thing we know that this particular term magnitude of this particular term must be smaller than unity. So, the eigenvalue should be inside the unit circle and this is exactly what that eigenvalue is. And if you further summarize we know that for D less than 0.5 the current loop is stable will be stable. But if you go beyond D greater than 0.5 then the current loop will be unstable and we are going to consider you know experimental hardware case study.

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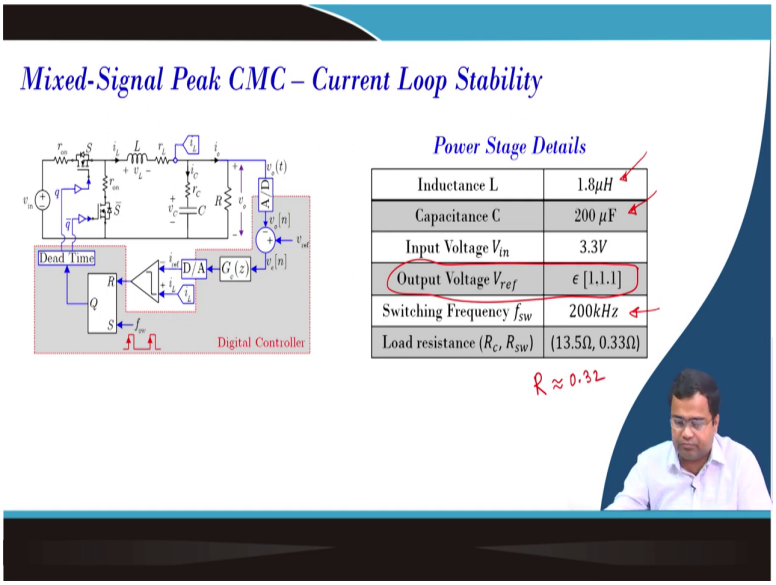

Where again we are considering our traditional 1.8 volt inductor 1.8 microhenry inductor, and 200 microfarad capacitor and here we are not closing the outer loop. So, this output voltage can vary we are allowed to vary because regulation may not be perfectly achievable.

Because we are only giving a fixed current reference, but we are operating at 200 kilohertz and load resistance we have considered that there is two resistance, but for this particular case we have turned on the switch resistance. So, for the R effective we are considering 0.32; that means, this is considering both the resistance in parallel and the controller we are not using any controller.

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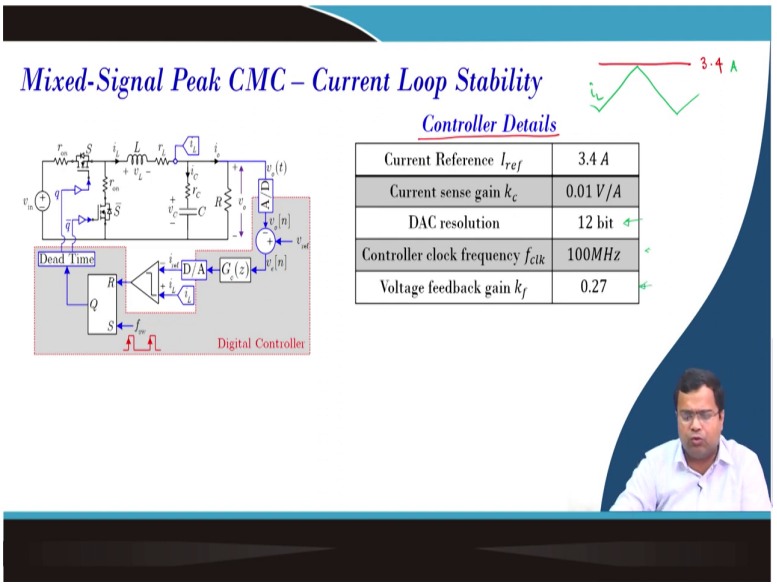

So, I will say instead of the controller it is the hardware details where we are using a reference peak current. That means, we are applying a peak current that is 3.4 ampere and we are comparing the inductor current with this peak current; that means, this is the inductor current we are comparing. So, 3.4 ampere is the current reference, but that is a physical current reference, but actual implementation because there will be a current loop gain and etcetera.

So, then the number will vary, but when I will show the experimental result it will show 3.4 ampere and we all know that the current sensor also has a gain. Because it is a current resistance followed by an amplifier we also consider DAC resolution 12-bit. Because we are sending the data through DAC and the controller clock is 200 megahertz feedback voltage gain is 0.27, but we are not closing the outer loop. So, you do not have to care.

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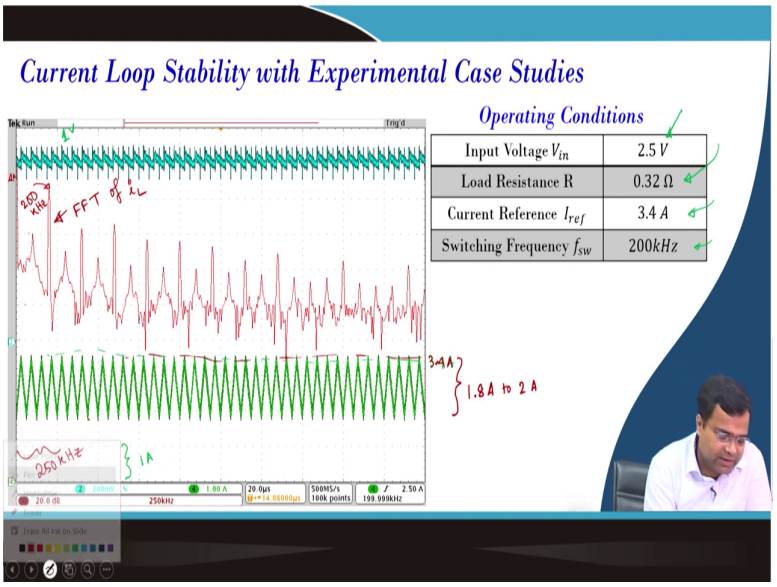

Now, I am showing the first experimental case study where we are setting the input voltage to 2.5 volt, and the load resistance is 0.32 that I have told. The peak current reference is 3.4 ampere and the switching frequency is 200 kilohertz. And if you see the experimental result and you see this division is 1 ampere for the current and the voltage if you see 1, 2, 3, 4, 5 it is almost 1 volt.

Because we are setting the current reference such that the output voltage is reaching 1 volt, but we are we have not closed the loop. And you can see the peak current reference is coming to be roughly around 3.4 ampere; that means if I use a different color. So, this is 3.5, 4 ampere, and another interesting point is that here it is more or less stable that is why I have shown the FFT, which is the FFT of the inductor current.

And you see this FFT is that this particular division is 250 kilohertz; that means, here we are getting a peak which this peak is at 200 kilohertz and that is our switching frequency. So, we are getting a sharp peak at 200 kilohertz and then harmonics with respect to that fundamental component because it is stable. So, you can see the power spectral density that is kind.

Another interesting point we should remember is the current ripple. So, the current ripple if you consider it is coming just below it is around 1.8 to 3.6. So, roughly I think it is around 1.8 ampere is the current ripple; ripple that is our current ripple roughly. It may be slightly higher I think it will be almost like 1.82 to roughly around 2 ampere it is not exactly correct, but maybe around 1.8 or so ok. Let us consider it as 1.8A because we have not regulated the volt.

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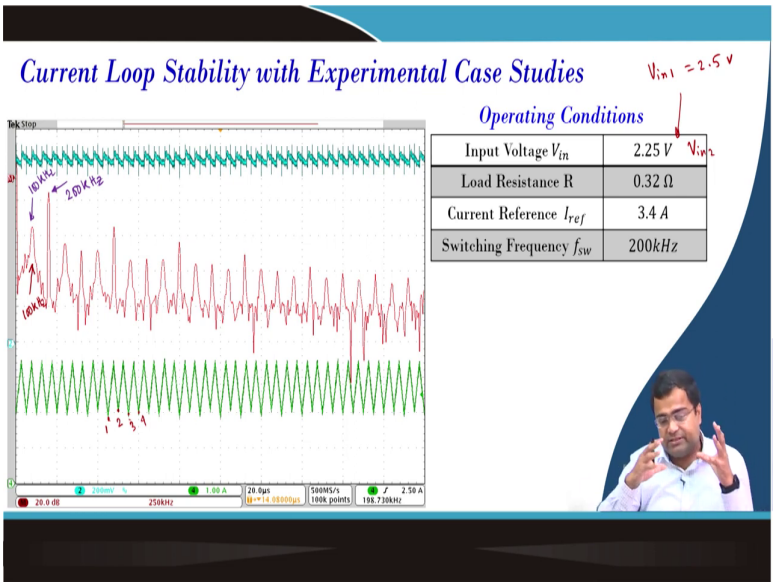

Now, what we have done? We have decreased the input voltage. So, earlier case one was 2.5 volt. Now we have reduced it to 2 points, this is V in 2. What will happen? You see slowly the subharmonic has started because you see that in between this peak, it is reduced.

Because if you take this as 0.1, this is another point, this is another point. So, 0.1, and 0.3, are sort of repeating, but 0.2, and 0.4 are sort of repeating. So, slowly several oscillations just started and this is also you know evident from this peak which is at 100 kilohertz because we are talking about subharmonic.

So, subharmonic means this peak is at 100 kilohertz, and the switching frequency peak is 200 kilohertz. So; that means, we can see the power spectral density sub-harmonic that is why sometimes called sub-harmonic instability because it is half of the switching frequency.

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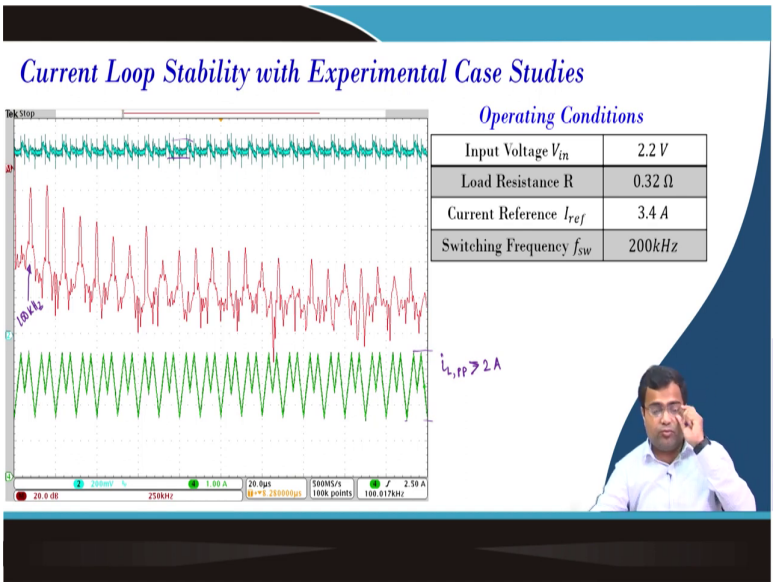

Now, what will happen here the ripple impact is not fully visible. Now we are further decreasing to 2.2. Just increase by 50 milli volt, decrease by 50 milli volt and you will see a drastic change in the current parameter now this peak has gone up this is at 100 kilohertz. So; that means, you have a dominant effect of the subharmonic component and that is also obvious in the ripple parameter because it will increase.

And you can see this current peak-to-peak current ripple; that means if I say i L peak to peak how much will be that? So, this division will be almost 1, 2. So, it is crossing it is I would say more than 2 ampere. So; that means, the current peak-to-peak is higher than the current ripple that we have seen.

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The next part is if we further reduce to 2 volt. Now the effect become more prominent so; which means, you see now the subharmonic component is dominating over the fundamental component. That means, you have clear evidence and the ripple current has significantly peak to peak has significantly decreased.

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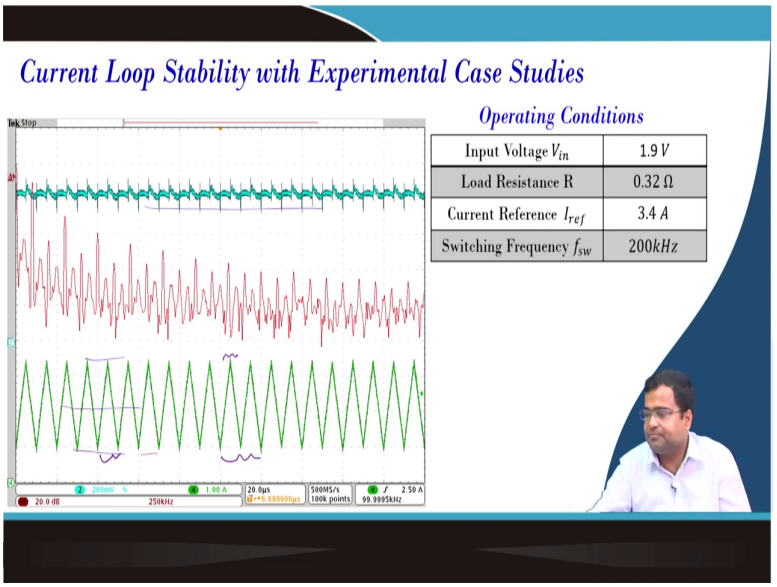

So, then if we further decrease you will see the switching frequency become half is like become half. Because this to this it is 20 microsecond, you can see this is 20 microsecond. So, this will be 10 microsecond, but we have 5 microsecond, 200 kilohertz switching

frequency and this is because of non-linear phenomena and you can see that output voltage also goes down. Because your peak current is fixed. So, this guy is going down.

So, the average will be going down as a result of your average voltage. So, you need to anticipate this can be you know regulated by an integral control, but this instability can cause a large ripple current as well as voltage.

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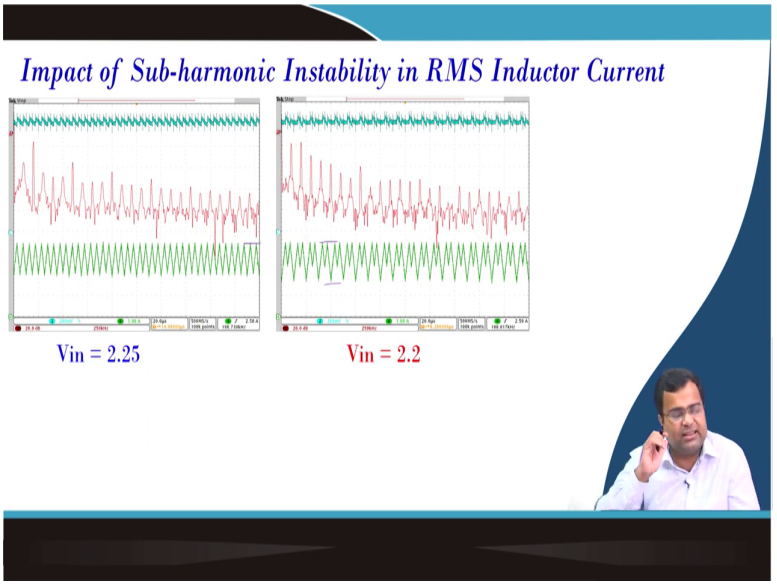

So, this impact of sub harmonic if you say 2.5 and 2.6 it is visible in terms of power spectral density. The RMS current we saw there will be an obvious increase in the RMS current because of the instability and the ripple parameter is also increasing from peak to peak.

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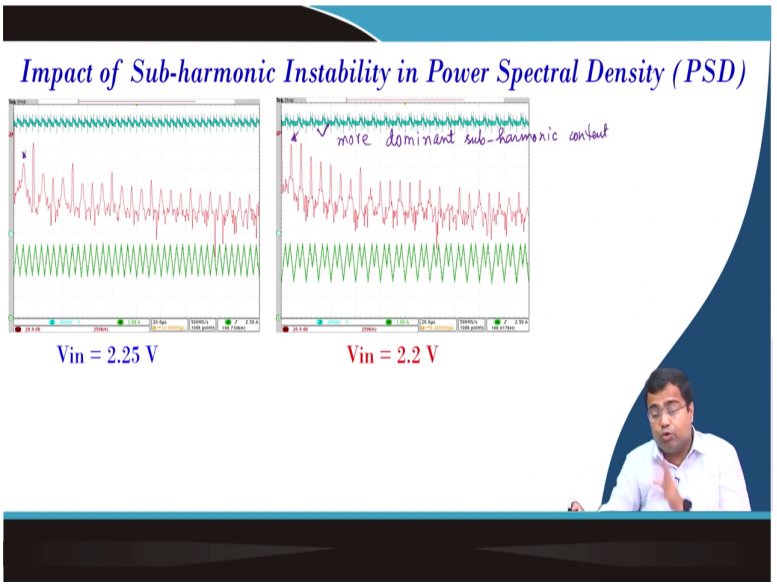

And if you take the power spectral density you can see the subharmonic component become more dominant compared to this case. So, this is more dominant sub-harmonic content and which is not desirable.

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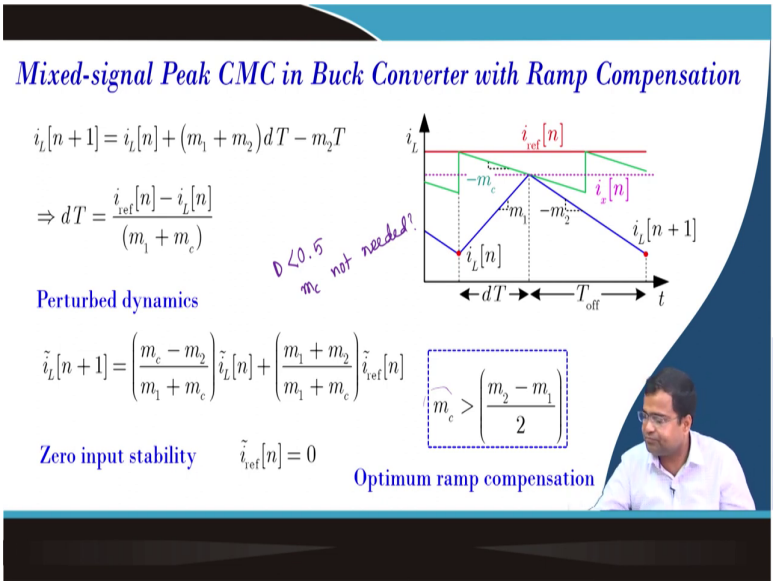

Now, we know about ramp compensation if you add the ramp compensation then the duty ratio expression will get changed and if you get the perturb dynamics for fixed current reference. It can be shown that the current loop will be stable if the compensating ramp is greater than this.

But we have to make sure if the duty ratio is less than 0.5 then by this calculation MC becomes negative, but we are not going to use a ramp when so; that means, we will not use the ramp. So, MC is not needed in that case, but when you close the loop in fact, we may need this MC even at a slightly lower duty ratio because of the closed loop effect.

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Then if we add the ramp this was before adding the ramp at 3; for 2.2 input voltage after adding the ramp now, it becomes stable. So, what we are doing? Because with because we have a fixed current reference now through the DAC we are generating also a ramp with this kind of thing.

So, from digitally inside and then inductor current is getting compared with this. Since we are using a very low ramp; that means, the peak has not changed drastically it should have reduced from 3.4, but the reduction is very small because the ramp is very small.

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And because of the use of a small ramp even at 2 volts where it was totally unstable here also it is unstable, but it has improved, but it is not purely stable. So, what do we have to do? We have to increase the ramp slope; that means, for stabilizing the current loop when the duty ratio varies widely for large duty ratio operation your ramp slope has to be increased and this can be computed from this slope.

But if we use a large ramp throughout then what will happen? It is well-known fact that you can because of the same design if you add more and more ramp. So, the benefit of current mode control is lost because of closing the current loop. We want to control we want to replace or you want to mimic the inductor to be a control current source.

But when the ramp compensation is added then the two poles are. Because when there is a single pole approximation in current mode control the capacitor pole and the inductor poles are separated the inductor pole goes far away, but when you add more ramp then these two poles again start coming close to each other.

And if we add more ramp then it will slowly become voltage mode control. So, all the benefits of current mode control will be lost so; that means, a very high ramp compensation may not be desirable.

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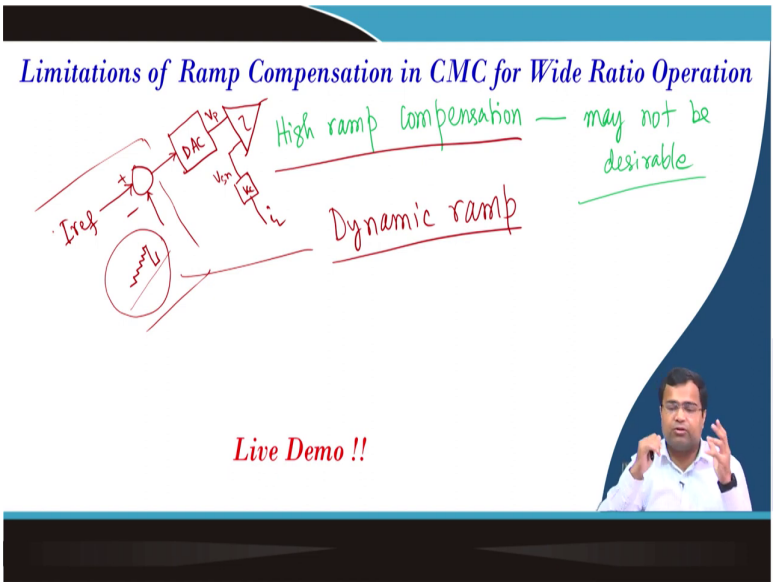

So; that means, the limitation is that high ramp compensation may not be desirable. Because it will affect sorry may not be it may not be desirable. Because what will happen for wide for even for nominal duty ratio stable operation it will not behave like a current mode control because you are adding a ramp. So, you are losing the benefit of the single pole approximation.

So, your compensation design has to be redesigned; that means, your PI controller may not be enough. So, you may have to campaign a PID controller, and also it may affect if you consider the PI controller, it may affect your phase margin and that is why you may have to reduce the cross-over frequency. So, your overall controller has to be slow down you have to slow down the controller.

So; that means, the high ramp compression may not be desirable. But in digital control so this is for throughout the fix. But you can also consider dynamic ramp compensation how because you know this ramp we are using the digital platform; that means, the current reference minus your this ramp right?

This is all under and this is now going to the DAC and this is compared in the so this is your peak voltage and this is your sense current and we have this current loop sensor gain i L. So, what I am saying since it is inside the digital platform. So, you can always play with the ramp slope inside the digital platform.

So, you can do a dynamic ramp compensation or you can disable this ramp during transient and enable this ramp during the steady state for stabilization. So, all this play around I mean you can play around this control strategy we have to be very careful about this dynamic mechanism. Because you need to identify suitable transient and steady-state conditions based on your duty ratio if you keep on watching the duty ratio.

You can simply extend the ramp and keep it throughout during transient and steady states. So, all these possibilities exist in digital control, but now we want to show a live demonstration of digitally current mode control fixed frequency with fixed current reference with and without ramp using the harder prototype.

Now we are going to consider the mixed signal current mode control and we want to see the current loop stability where we have used a fixed current reference. So, first I am running this Verilog code this is now we can you know compile this code there are steps and I think all the steps we have discussed in the previous lecture.

So, I am just going to browse through those steps very quickly and you know this is the code where we are generating the reference current. And we have the provision for ramp compensation there is an external switch by which we can add the compensation.

So, now, once we run this code then once the program file is generated. Then what do we have to do? We have to select this particular file and this bin file then we need to program it. So, it will take some time and once this programming file is dumped into the FPGA into the flash memory and then we have we will be ready for running the actual hardware.

So, this is the step where our Verilog files synthesize. Then it generates the implementation detail for the FPGA prototyping and it also generates the dot bin file. Now, in this bin file, we are using another interface and we have demonstrated that the MIMAS FPGA configuration for this particular FPGA is down.

And now this program is dumping into the FPGA. So, we will take maybe less than a minute to complete this dumping process. Now the computer will be out of the real-time loop and we are going to demonstrate the current mode control. So, we are almost in the final stage of our demonstration. Now so this shows it is done.

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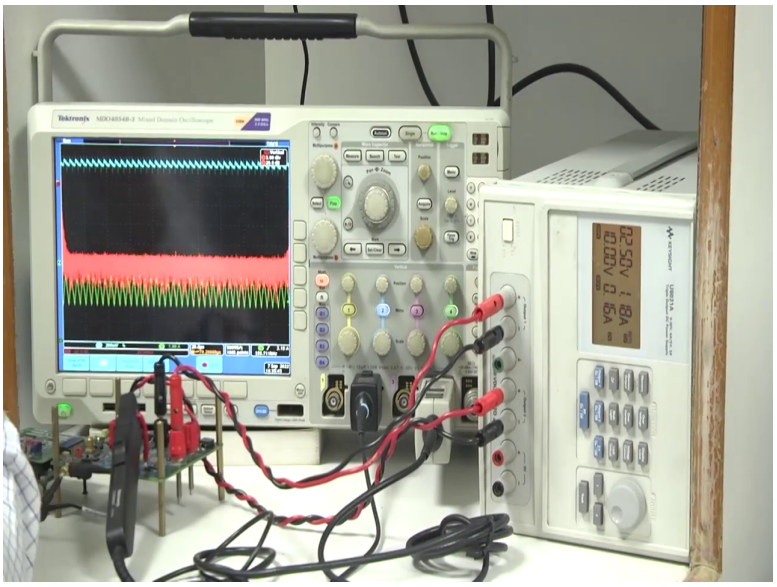

Now, we are coming to the actual demonstration. So, this is the power supply where we have two the first channel. This is the second one is for powering different IC you know ADC, DAC, and all and the first channel is our actual power input.

So, if you turn on this power input this is the scenario we have set 2.5 volt as the input. And as we have discussed in the lecture we have used a fixed current reference which is at 3.4 ampere. Now in this 3.4 ampere, this is the output voltage and we are going to see stability. So, in this condition, we are turning on the known FFT algorithm.

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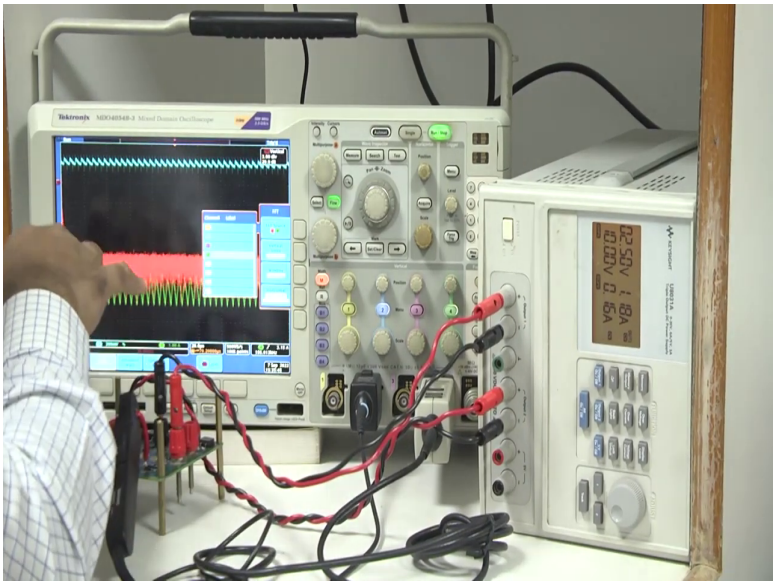

And this FFT we are taking channel 4 and we are showing this FFT you know we want to take this FFT here first. And then we want to consider the 250-kilo hertz range now we are taking this FPGA screen. So, this is the 0 frequency coming, so 0 frequency is here now.

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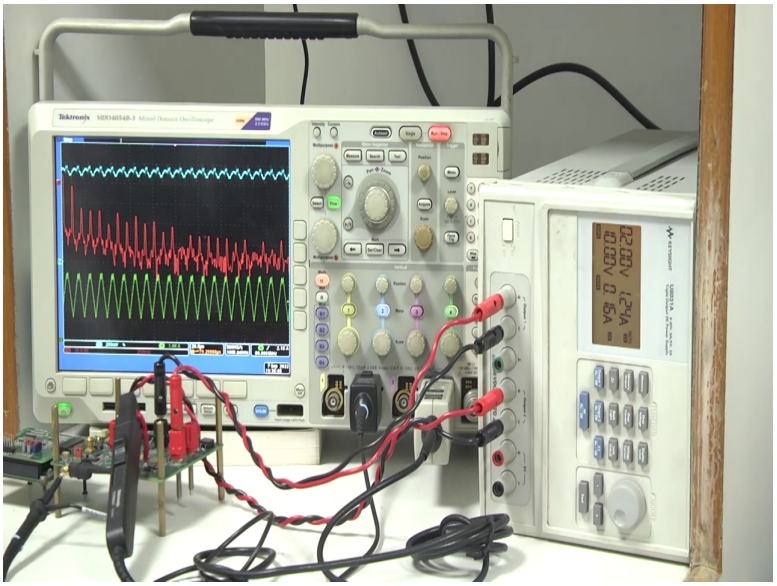

So, now we have placed the 0 frequency here. So, you can see there is a spectral peak at 200 kilohertz. Because this length is 250 kilohertz and this one is 200 kilohertz. So, that is our switching frequency that is the fundamental component and then there are harmonics.

Now, today we have demonstrated what we have demonstrated that if we decrease. So, at 2.5 kilohertz the current loop is perfectly stable. Now we are reducing that to 2.25. So, let us go to 2.25. So, we are slowly decreasing the input voltage and we are coming to 2.25 and this 2.25 it is almost kind of on the verge of instability.

That means you can see if we just stop it you can see that it is almost instability is just about to start. There was subharmonic is just starting to create they are not exactly matching some cycles they match in between there is a slope instability.

So, now we are running and we are coming to 2.2 volt. One we go to 2.2 volt which we have shown. You can see that it is there is subharmonic instability and this spectral peak is coming that is the subharmonic which is at 100 kilohertz that is coming and this we have shown in today's class and then what we are going to do we are going to now reduce this voltage to 2 volt.

If we take it to 2 volt now you will say that at 2 volt we have seen that this instability is coming which is almost coming to a situation where it becomes like 100 kilohertz. But still, there are some switches on and off and this spectral peak is now very sharp at 100-kilohertz subharmonic is very dominant. And you can see that ripple has drastically peak to peak has increased so it will affect the RMS current.

Now if we further go to one point nine that we have shown if we go to 1.9 in volt then it looks like the switching frequency becomes half there is no component here. So, fundamental is coming at you know 100 kilohertz then all the harmonic, but it is not 100 kilohertz it is set to 200 kilohertz. Because it is a non-linear phenomenon that is making like 100 kilohertz.

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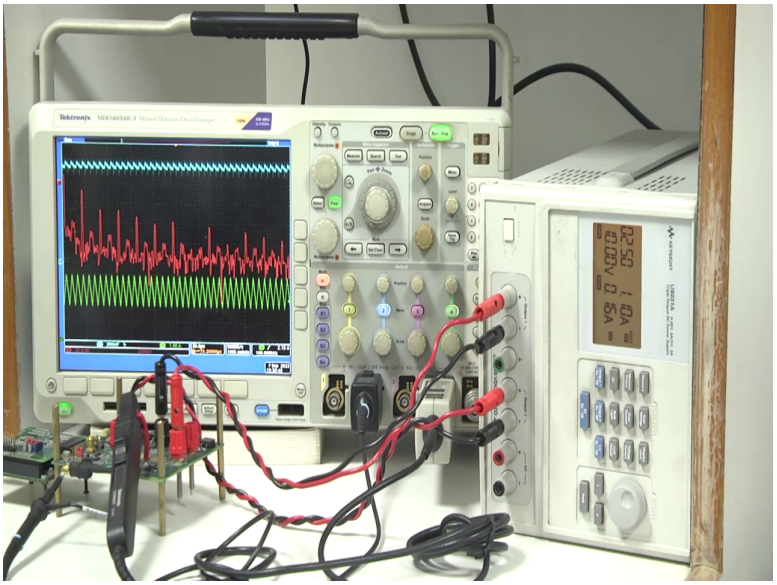

So, now we are going to start the ramp compensation and we have shown at this to 1.9 volt there is a provision of the switch, and this switch we are giving from externally. If we consider this switch now we have added a ramp, but it is a very slow ramp. So, if we add this ramp you see the nature of instability got changed; that means, in between something happening, it is not stable. But there is some improvement in the stability compared to the earlier case when it was looking like 100 kilohertz.

Now, we are going to 2 volt operation. So, 2 volt is also unstable, but it is somewhat better than the earlier case when there was no ramp compensation. Now we are further increasing the input voltage. So, we are going to 2.2 volt we want to show 2.2 volt. So, 2.2 volts now is

stable which was unstable earlier. Now with the ramp it is stable and it will further increase to 2.5 then it was stable in both cases.

So, that way we have seen that the ramp compensation can make it stable and when there is no ramp compensation then it was unstable from 2.25 below 2.25. But you know we added them it was stable, but it was not stable even at a lower voltage. So, you need to increase the ramp and we have discussed that a higher ramp can take the current mode control close to the voltage mode control which is not desirable.

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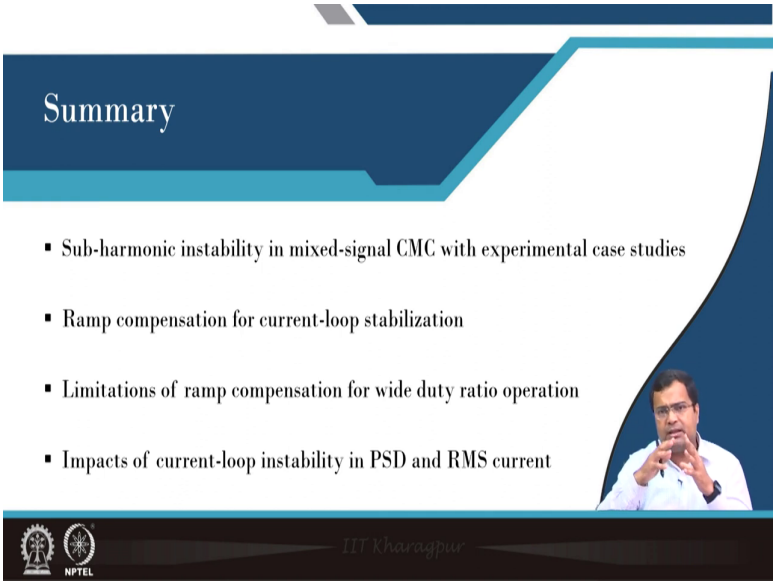

So, we have just completed our video demonstration. So, we have discussed here subharmonic instability mixed signal current mode control. We have shown experimental case studies, and we have also considered ramp compensation for stabilization. We have shown the limitation of ramp compensation and we have also discussed what is the impact of current loop instability in terms of RMS quantity and the power spectral density we will discuss some aspects quantitatively in the last week of the lecture that is it for today.

Thank you very much.