Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 01
Introduction to Digital Control in SMPCs
Lecture - 09
Levels of Digitization in Multi-loop Feedback Control in SMPCs

Welcome back. So, in this lecture, we are talking going to talk about Levels of Digitization in Multi-loop Feedback Control in Switch Mode Power Converter.

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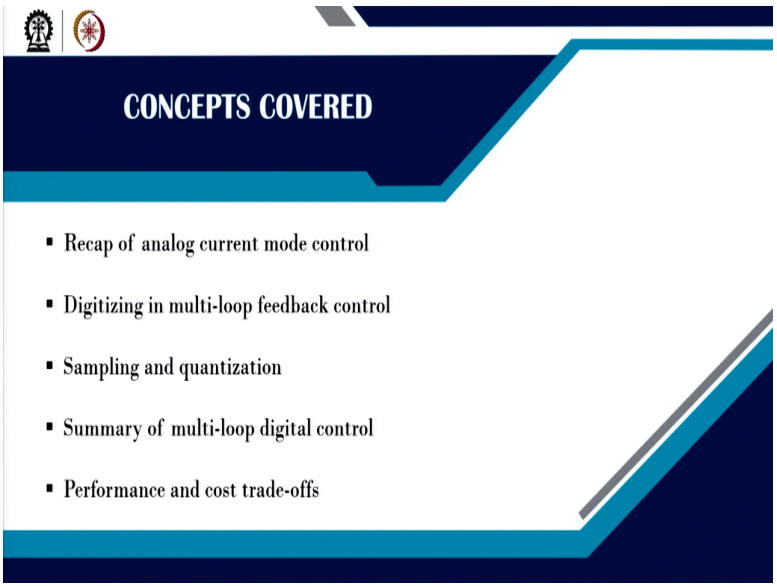

And when you talk about multi-mode control, in general, I know the current mode control is a good example of multi-mode control; sorry multi-loop control. So, you want to recapitulate analog current mode control; then, we will start discussing what is the technique for digitizing multi-loop feedback control which is a current mode control. Then, we will talk about sampling and quantization and a summary of multi-mode digital multi-loop digital control, and then, some aspects of performance and cost trade-offs.

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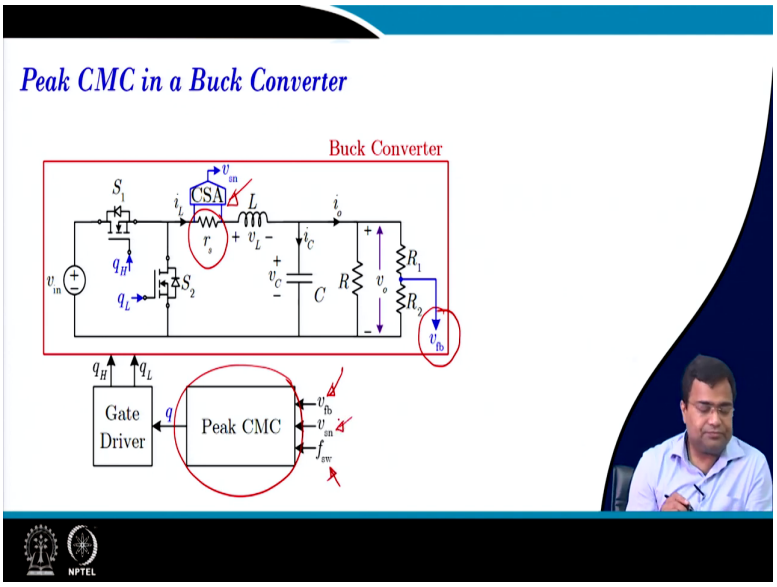

So, if we go for peak current mode control in a buck converter and this is the diagram of the buck converter here, we are using a current sense register here, and then, there will be a current sense amplifier and this sense current is a feedback for the loop. So, this is a peak current mode control architecture and here, it is the feedback voltage that is tapped across the resistive divider then, we are also using a fixed frequency clock, an external clock and this is a sense inductor current.

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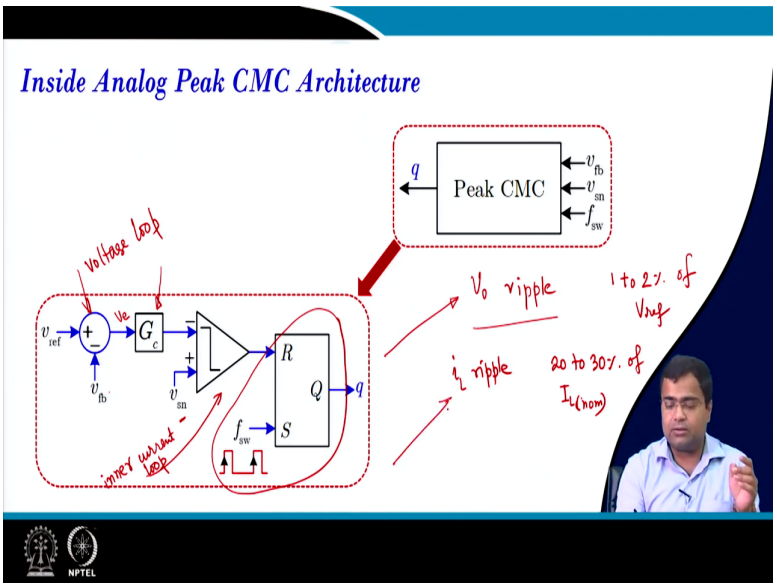

Now, if you go inside the peak current mode controller, what is there? We know that first the reference voltage will be compared with the feedback voltage, then it will generate the error voltage; then, there is a compensator which is a voltage controller. Then, the output of the voltage controller, we generally call a peak current reference or it is a voltage reference because we are using a sense voltage, which is capturing the current inductor current waveform.

And then, it is compared and the output of the comparator goes to the latch circuit; this is a latch circuit ok. Now, in this control, we have two loops; one is the voltage loop. So, this is our voltage loop ok and this is our inner current loop because it is a sense inductor current. So, it is an inner current loop; an inner current loop. And in current mode control, it is well-known that the outer voltage loop ripple; that means, if we talk about the output voltage ripple generally, we generally consider 1 to 2 percent, 2 percent of the V ref, or even less.

But when you consider the inductor current ripple, then we generally consider 20 to 30 percent or even higher of that I L average that nominal value ok; that means, the nominal value is the nominal load current for a bulk converter. So, if we are talking about 20 ampere nominal current. So, 30 percent of 20 amperes means it will be 6 amperes. So, it can be 4 to 6 amperes in the current ripple.

So, we can imagine the ripple in the inductor current is quite significant in terms of their percentage compared to that in a voltage mode control because in voltage sorry voltage ripple because we generally want to achieve a clean output voltage, although it is not achievable; but still, we want to achieve the average value the ripple should be very very low. But the current ripple is large.

So, generally, the current dynamics are much faster and the voltage dynamics are slower. So, now, the question is in this two-loop control, how to start digitizing. Keeping in mind, the voltage ripple is much lower and the current ripple is much higher. So, what is the mechanism for sampling?

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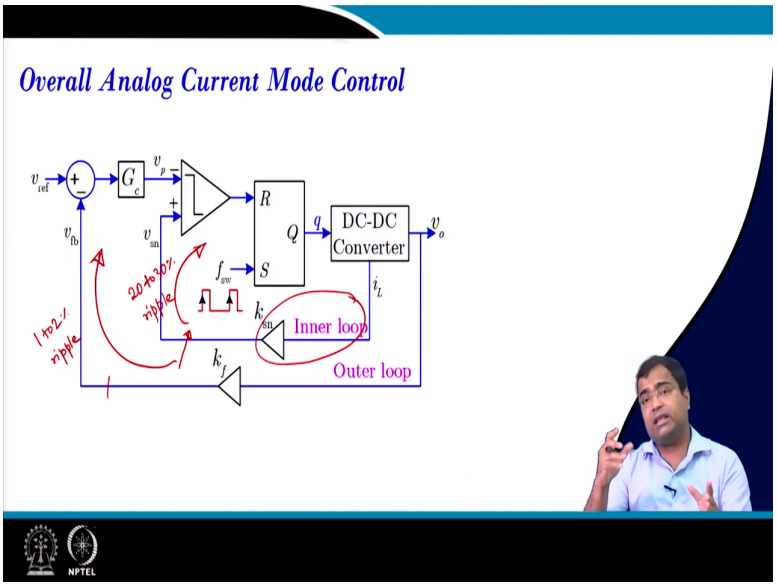

So, if you take the overall current mode architecture, this is the inner current loop that we have discussed and this is the outer voltage, right? So, this is the inner current loop. So, that is why it is a good example of two-loop control; sometimes we call it a cascade control, master-slave control. So, the inductor current loop is much faster and it has around 20 to 30 percent ripple; whereas, it is just a 1 to 2 percent ripple of this concerning V ref.

Now, the question is how to start digitizing this loop; that means, we need to retain the first dynamics of the inductor current. But voltage loop dynamics, although the ripple is lower, is smaller if you go for a small signal-based design, then generally the voltage loop bandwidth is lower; that means, we generally consider around one-tenth of the switching frequency.

So, compared to the current loop and current loop generally, we use almost full bandwidth, or the bandwidth of the current loop is decided by the current sensor. That means if you use a current sensor that has you know like 10 times the switching frequency. So, the current loop bandwidth will be decided. But the voltage loop bandwidth is lower. So, now, we have to pose the question of how to start digitizing where the outer loop bandwidth, if we talk about a small signal model is lower, but the inner loop bandwidth is faster.

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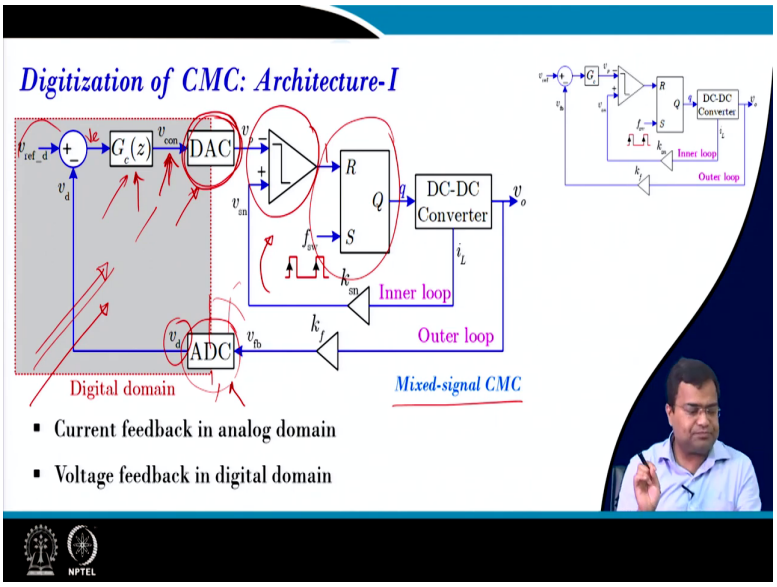

So, one architecture; the high bandwidth current loop which has a large ripple, let it be in the analog domain because this will carry significant ripple information which we cannot compromise, and also, the same current dynamics are much faster than the voltage dynamic because we have discussed the percentage ripple.

But generally, for the output voltage, we have a large capacitor because that is a standard process of any POL regulator, where we take the inductor to be much smaller and if we take to talk about 1 megahertz switching frequency, the inductor can be in the range of around 200 to 500 nanohenry; whereas the capacitor depending upon your input-output voltage undershoot and overshoot requirement, it can be as large as several hundreds of microfarad.

So, you can imagine that the voltage loop and dynamics are much slower. So, it is reasonable to keep the voltage dynamics in the digital path. That is why we are putting A to D converter that is digitizing. But the next question, when you have this digital voltage, then the reference will be digital, ADC is also digital and control is digital. As we have discussed in the previous lecture that digital is in the single feedback loop.

Thereafter digitizing the voltage, everything else was digital, we have to only consider the sawtooth waveform inside which is also digital. But here, it is a mixed domain; which means, you have voltage in digital after the ADC; the compensator is also digital, but the output of the compensator is generally used for the current reference, but the inductor current is the analog domain.

So, naturally, you need to consider a DAC converter. So, that means, when you take this architecture you have 1 ADC, it is called mixed signal current mode control. This is a version of digital current mode control, where we use a mixed domain; which means, an analog loop for the current and a digital loop for the voltage. So, current feedback in the analog domain and voltage loop in the digital domain.

Now, you may ask if one of you knows the challenge here is that you need ADC and DAC. So, the cost of the DAC can be high, and power consumption can be high, but it retains the first dynamics of the current. Here also is another thing we have to keep in mind, this is an analog comparator. So, we cannot have a very fast comparator because if you use a fast comparator, then it may consume more power which is another issue.

Another issue is that since you are sensing the inductor current, then there can be noise in the current; particularly, switching noise. That means, when the switch turns on and turns off, there will be some spike and this is compared with the digital you know the analog version of the digital signal, where it will be constant if you take one sample per cycle.

So, it will be because we have discussed in the previous lecture if we take one sample per cycle, where there can be a delay. Then, the voltage loop will be updated once in a switching clock or switching period and that means, throughout the switching period, it will be constant.

And then, the control will also be computed in synchronization with the clock. So, that means, the control output will also be constant for the whole cycle. Now, once you have the DAC output, it will be also more or less constant for the cycle; but this inductor current actually when it touch; that means, peak current mode control, there can be a spike.

So, then, you need to sink; that means, you need to use the trailing edge modulator that will you know to avoid any fast you know multiple switching. So, that means, there is a modulator and this is pretty standard. But the question is in this architecture, then you need a high-speed analog comparator, the current sensor is analog; so, it can retain the first dynamic.

But the question is then why put a digital controller, why not put all analog? Because the anyway current is analog. So, the question is whether this digital controller can be tuned because you need to update the controller value. Suppose you are talking about a PI controller.

So, if we use the same value of PI controller for the entire operating range, then we have discussed in our earlier course; that means, the design of compensators, we have carried out based on you know pole-zero cancellation or there can be a conservative approach. But if we use a fixed gain comparator, then this will be designed based on the worst case; but the converter will not operate the worst case the majority of the time.

So, then, we will lose performance which is one aspect. The second aspect; means, we should update the controller value and we can use a lookup table to update the parameter by using some information either load or input indirectly; that means, we need to use some information of the load or the transient and that can be captured using ADC bit; that means, how it is updating that is one possibility.

Another possibility, we will discuss is if we go for a large signal transient we have discussed large signal tuning. We can update this controller value in such a way, we can get the fastest transient. There, we want to retain the ripple information of the output voltage ok; that means, we need to emulate or we will discuss some aspect there.

So, we can achieve almost the fastest response like a time optimal control; but due to the delay of the ADC, the performance may be limited which is another possibility. The third possibility, since we are generating the reference current from inside of the digital controller; is that means, this whole in digital, we can always use a programmable current reference because in peak current mode control, we should be able to protect the circuit.

That means, if you want to protect, we want to program the current reference with either a higher or lower value because if you use a program current value from the digital domain, then it will limit the actual inductor current. So, you can keep the actual limit inductor current by using an external command; that means, you want to comment that I want to limit the current to 4 amperes or 10 amperes, or 15 amperes.

So, this is much more flexible than just a common line because this is ultimately a number that you can adjust through a resistor. Another aspect even if we are going for a large signal transient because of the delay, you may lose the control loop bandwidth because we have discussed that digital control has some shortcomings. When you have this A-to-D converter, we cannot have a very high sampling rate because that will unnecessarily increase the cost and the power.

So, we have a limit on the ADC conversion rate, and because of the limit, we will have a delay, but imagine, if we take let us say for example an analog comparator and if you look at how the voltage loop is deviating within some hysteresis band, then you can quickly ramp up this current using some non-linear algorithm.

That means, you can increase the current very rapidly, then we can bypass the linear control loop. So, all these possibilities are there or if you go for let us say if you are talking about PFM control under light load because we have discussed and we will be discussing it in this course and even we want to implement it.

If you are going for peak current mode pulse frequency control, which will increase the light load efficiency so, we can there we need a constant current reference; a constant current reference then, on time will be automatically adjusted so that it will behave like a constant on-time control and this will also ensure that voltage ripple will not go beyond that.

Because we have discussed in lecture number 24 in our earlier course the different light load control methods. So, here, we can set the current reference to optimize efficiency under light load control. So, many possibilities exist which will not be possible, or in fact, it will be very difficult in analog control. So, that is why this loop enables you to do whatever you want other than just simply tuning the gain.

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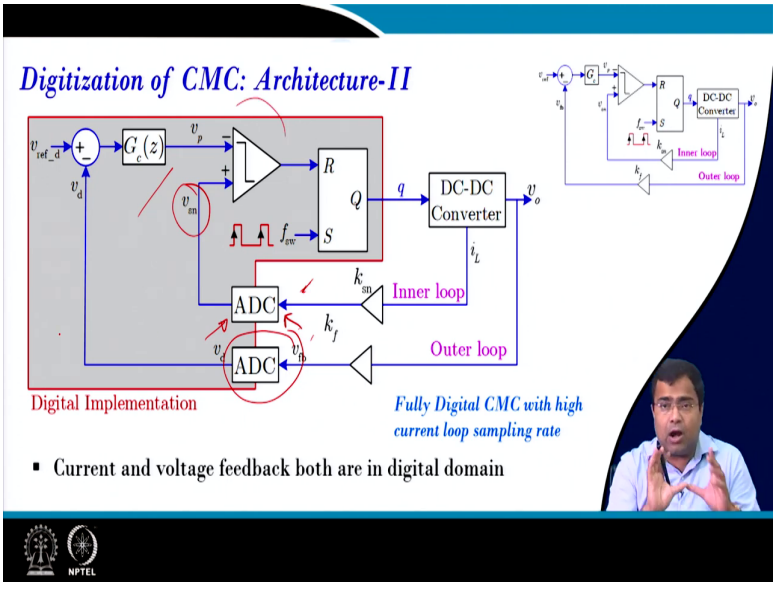

Another architecture; we can keep even the current loop digital. So, earlier, we will retain the voltage loop and discuss various possibilities. Now, we keep the current loop also in digital, but we have discussed the current has a large ripple which is 20 to 30 percent. So, we cannot simply take one sample per cycle because then, you cannot get an on-off operation for the whole cycle. If you take only one value of the current and one value of the voltage, then the current reference will be fixed for the same duration.

Sample inductor current which is here sample that will also be fixed so, either the current reference can be above the sample value of the current, then the whole cycle will be on or the current sample can be above the current reference, then the whole cycle will be off. So, you cannot get an on-off operation either fully on or fully off. So, eventually, it will lead to a lot of non-linear phenomena.

So, to avoid that you need to add a higher sampling rate for the current so that you can retain some useful ripple information and that also is difficult if you just take four samples or five samples. That will not only increase the ADC sampling rate but may also lead to a lot of non-linear phenomena ok.

So, that is why we may not have this technique that has some limits because you cannot have a very high sampling rate of the current loop because that will unnecessarily increase the cost. So, this is called fully digital current mode control with a high current sampling rate. Here, the current and voltage of both loops are digital.

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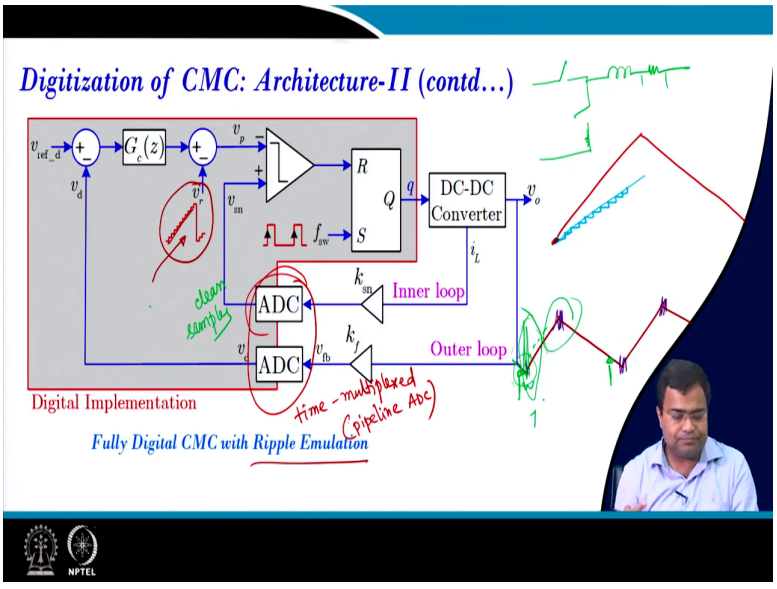

So, everything is digital, then how to address this problem? One way to address this problem, we take one sample of the ADC; that means these two ADC will be a time multiplex. You use a time multiplex; that means, it can be a pipeline ADC; where we can mux the analog channel and we can take the sample voltage and current at two different time instants.

Once you do that; that means, you are taking the current to suppose for example, this is my inductor current and we will be discussing this, and suppose, you capture this inductor current waveform. So, then, you can interpolate using a saw tooth waveform. That means, this can saw tooth waveform internally; that means, this block will be a ripple emulator.

So, there will be an additional block which has to be a ripple emulator. This ripple emulator job is done by this guy; it is not needed because it is taken care of by this saw tooth. After all, either you add the ripple with the current sample or subtract the ripple from the current reference. So, they will be analogous.

So, that means, here as if we are taking the ripple current through this virtual ramp; that means, this ramp is trying to provide the ripple information of the current which is lost because you are taking only one sample. Now, there are many research papers; which means, many people try to get the actual slope. So, that means, the slope of this ramp people try to achieve is identical to the inductor slope, and how to do that? Naturally, to know the information about the inductor, you need to know the input voltage and which is not a robust solution.

There are other techniques also; when you go to that architecture, we will discuss them. So, it can also be shown even if you take the exact current ripple, it may not be good for the first scale or the stability point of view. So, what will be the right choice of slope that we will discuss when you go to stability and another aspect of digital current mode control?

So, the only thing we keep in mind is that it is possible to implement a fully digital current mode control with ripple emulation in which the ADC of the current as well as the voltage can be sampled once per cycle. As a result, both the ADC can become a single ADC with two analog mux which means two analog channels.

So, you can tie multiplex and this can cut down the cost because only one ADC, and there is no DAC requirement. And in fact, this method also helps suppose if you take the sample, suppose I am talking about the inductor current like this. Now, when you go for sense current,

sometimes you know the high frequency, there can be some kind of spike here. For a very high-frequency current sensor, there can be a spike; but if you take the current sample.

For example, you take this clean current sample here, when before the switch turns off. So, there are the clean samples, right? If you take a such clean sample it is going that these are my clean samples; these are my clean samples. Then, you can add RAM. So, that means, as if you are adding RAM here.

So, in that way, you can make the current controller or current loop insensitive to switching noise and that is not avoidable in analog control. As a result, most of the analog control, even for this case also sometimes uses a minimum dead time because if there is a large spike in the current, particularly during transient or some spike.

So, we need to avoid this for buck converters, it is easy. But suppose, if you are talking about a converter, where both sides of the inductor have a switch node or suppose you know if we take a buck converter, you know if we place a current resistance across the inductor; then, you will not have such issue, may be very less.

But suppose you are talking about a current sense resistance or maybe RDS on the switch. When you talk about the RDS on the switch, this resistance is kept in the switching path. As a result, when there will is a turn on and off, there will be (Refer Time: 20:15) action.

So, naturally, such can create some spike in the current and this spike can cause false triggering; that means, the switch can be turned off at the very beginning and that may lead to a lot of non-linear phenomena. So, in analog control, people use something kind of blanking; that means, they do not take any action for a certain time duration.

Then, only they compare, and that limit the effective duty ratio operation; that means, you cannot achieve a very low duty ratio operation due to this blanking mechanism. So, that means, the duty ratio below 10 percent, or 5 percent, will be 0. So, it will start from 5 percent to that full swing. But when you go to digital control, such a problem can be avoided because you take the clean sample and you emulate the current slope internally.

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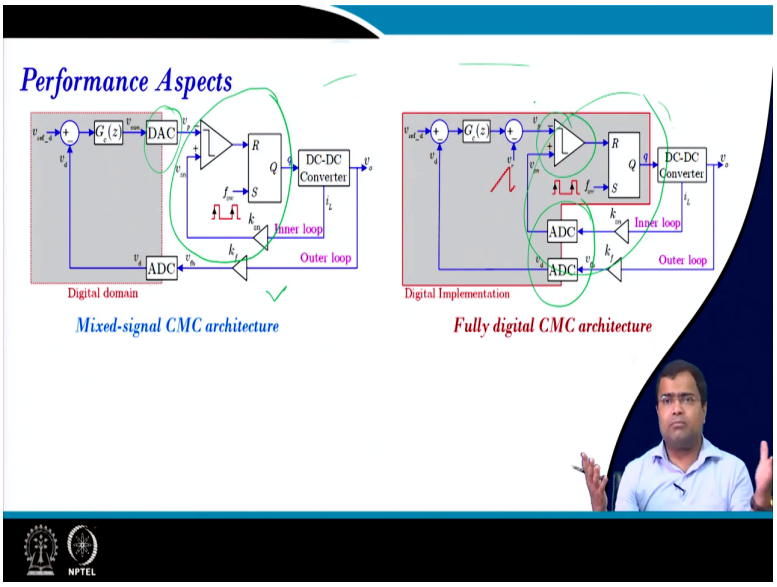

So, if we compare the performance, naturally this may be faster because the current loop is analog and you can do a lot of trajectory-based control. This may be slightly slower, but if you can properly emulate this current emulator and if you take the if you synthesize the trajectory, so this is kind of a research problem which are not discussed too much, but I can say that you may not get exact performance in general, but there can be a way to anticipate and you can get a very fast transient current signal.

So, performance point of view, as it is in general without talking too much about the trajectory shaping, this technique is slightly faster because of the analog current loop. But it also requires a D to A converter as well as the analog current analog comparator and if you go to fully digital ripple emulation, then you can use one ADC; you can avoid DAC as well as there is no analog comparator, it is a digital comparator which will be much faster with low power because it is just a CMOS transistor.

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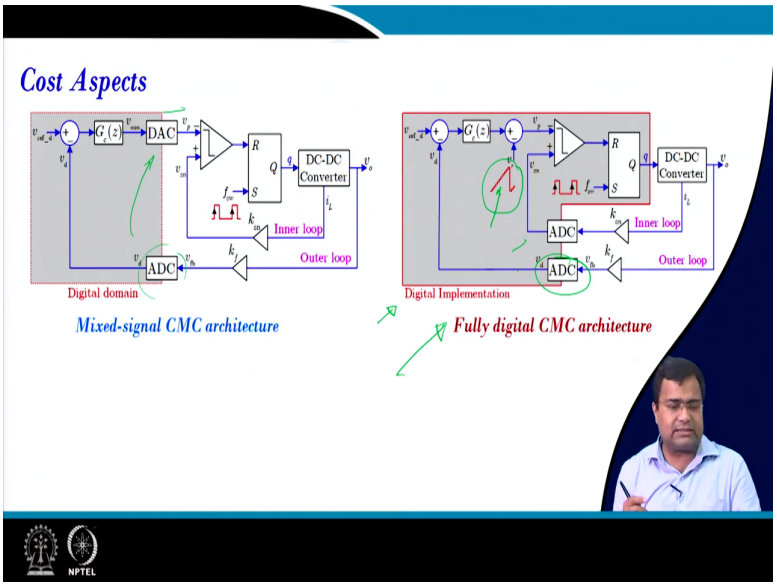

If you talk about cost, so you can cut down the cost with this technique. But this technique will also impose a challenge because the resolution of this emulated RAM will create a duty ratio limit which is not there in analog control because analog control, is just an analog signal; there is no resolution problem The resolution will only come due to the resolution of this ADC as well as DAC. So, it will only give a resolution of the peak current reference and that will impose some duty ratio resolution.

But in this case, the resolution limit will come due to the ADC as well as the resolution of this ripple emulator which will also; so, it is something similar to the voltage mode control resolution problem. But you still have current sample information. So, which will be faster than voltage mode, which means, from a cost point of view, this may be effective; but this may lead to even stability problems.

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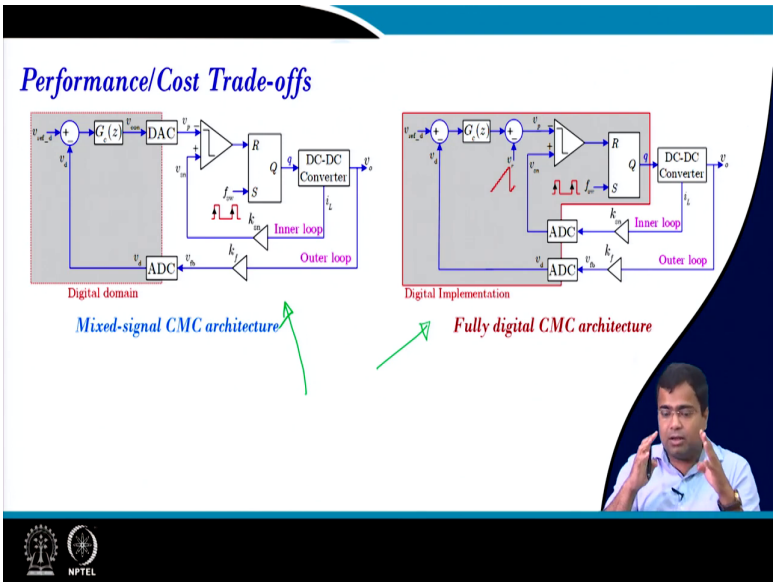

So, we need to discuss their performance and cost setup; but at this point, I will say both are equally good, but this technique is often used in commercial products ok.

So, this is about we discussed the basic concept of digitization. But in the subsequent week, we will elaborate detail about the internal architecture how to develop MATLAB models and how to simulate them effectively, we will go for hardware implementation. So, in the hardware, we are not going to consider fully digital because our hardware will have one ADC, and one DAC; but we will show the mixed signal current mode in the hardware architecture.

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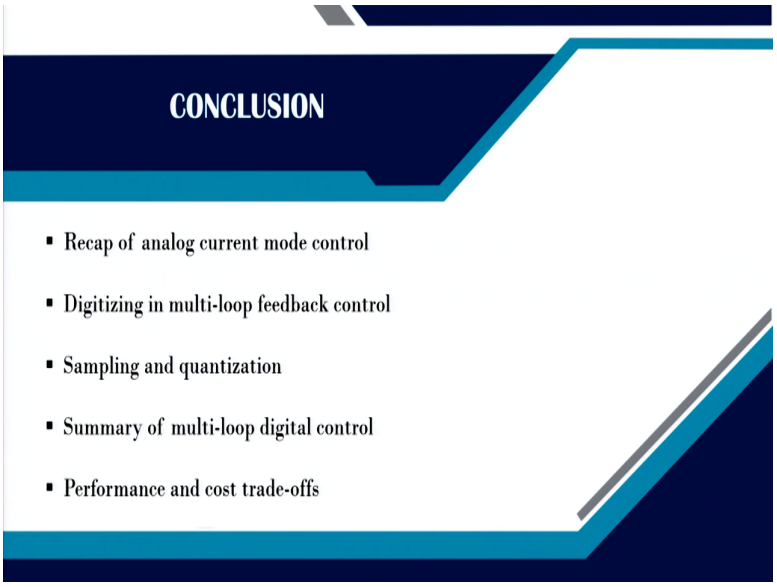

In summary, we have discussed various we have recapitulated the analog current mode control technique and this is like two-loop control. Then, we discussed how to digitize this two-loop control; where should we know sample whether we should sample the digitize the voltage or current or their combination? Then, we discussed some issues of sampling and quantization.

We have summarized that multi-loop digital control and we have discussed some aspects of performance and cost. But we will discuss this architecture in detail in the subsequent week. So, for today, I think we have just summarized the basic steps of digitization. So, that is it for today.

Thank you very much.