Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 09
Digital Control Implementation using Microcontrollers
Lecture - 89
Texas Instruments TIDM-02008 Reference Design Overview

Hello and welcome to the NPTEL online certification courses under the course Digital Control in SMPCs and FPGA-Based Prototyping. Today, we are going to study Digital Control Implementation Using Microcontrollers and specifically the Texas Instruments TIDM-02008 reference designs overview.

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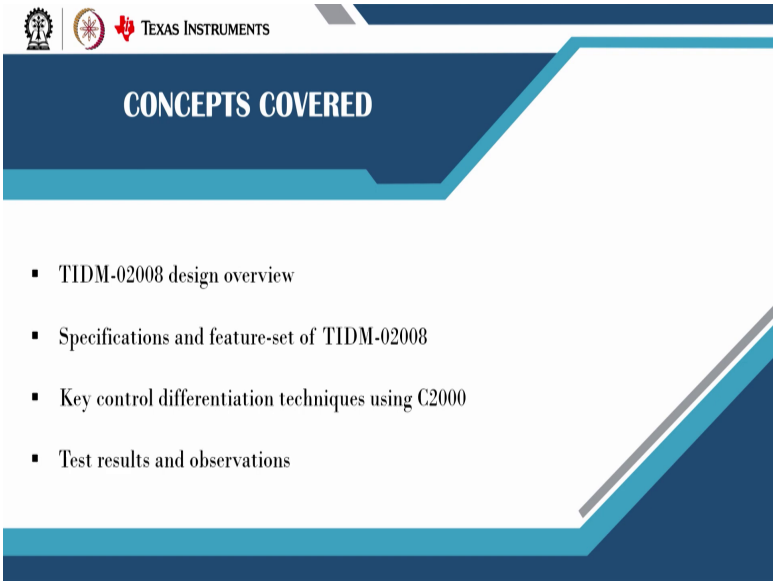

The concept covered in today's lecture will be the TIDM-02008 design overview. The specifications and feature set of TIDM-02008. The key control differentiations techniques were implemented using C2000. As well as the test results and observations.

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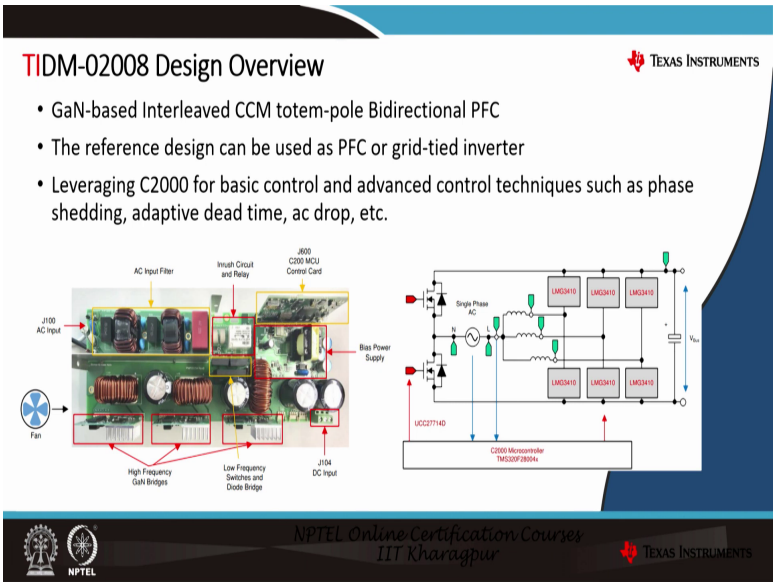

So, what is TIDM-02008? So, TIDM-02008 is a GaN-based interleaved continuous conduction mode operated, totem-pole Bidirectional PFC. Fundamentally the reference design can be used as a power factor corrector or a grid-tied inverter based on the supply side that you provide.

Leveraging C2000 capabilities for basic as well as advanced control techniques such as phase shedding, adaptive dead time, ac drop will be something that will be covered through the course of this lecture. The images that you see here on the bottom left are the actual hardware board design that is presented. On the right that you see is the schematic. To deep dive a little bit into the schematic, what we see on the left side in the actual design is 3 inductors.

They are the filter inductors on the bottom side of the image that you see are the high-frequency GaN bridges. There are 2 inputs provided to the design AC input as well as DC input based on what you want to operate if you are operating in the PFC mode of operation you would want to provide AC input and if you want to operate at an inverter level then you will provide DC input.

There is a control card presented in the design. And there are 6 GaN bridges LMG3410. In detail, we will go through the C2000 microcontroller implementation using the TMS320F28004x device.

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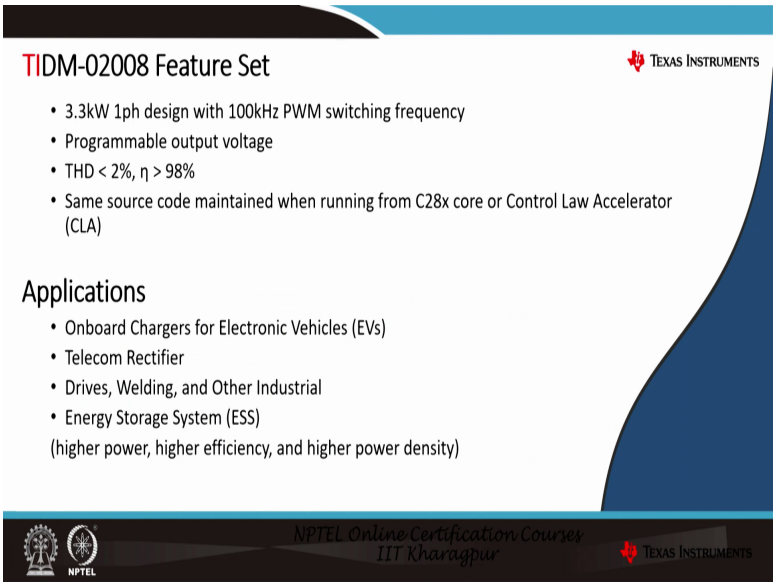

So, fundamentally the TIDM-02008 feature set includes a 3.3-kilowatt single-phase design with an operating frequency of 100 kilohertz PWM. It has a programmable output voltage feature, additionally, its operating THD is less than 2 percent. In an efficiency of greater than 98 percent. One good thing is that the same source code can be maintained when running from the C28x core or the control law accelerator as discussed in the previous lecture. If you are using the control law accelerator you free up the C28x core thereby adding additional bandwidth for the C28x.

The applications include the onboard charges for electronic vehicles, telecom rectifiers, drives, welding, and other industrial equipment. It can also be used in energy storage systems. The attractive part about this particular design is its higher power, higher efficiency, and higher power density.

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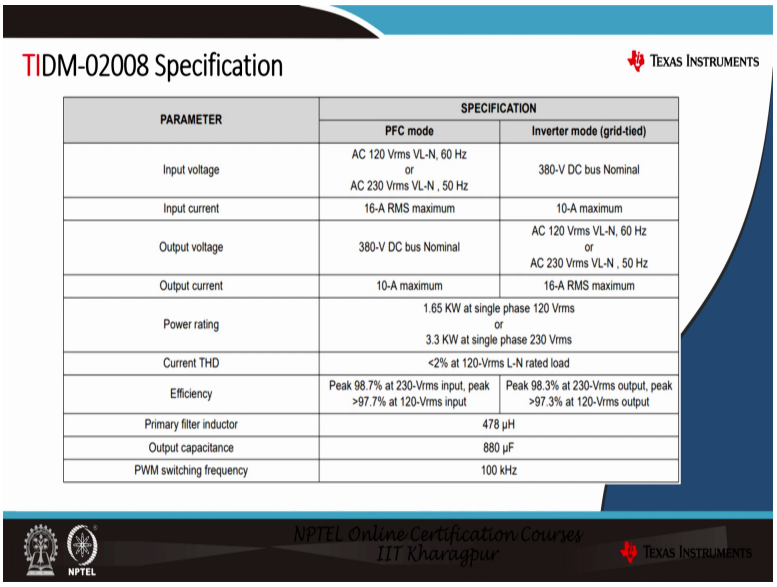

PARAMETER	SPECIFICATION	
	PFC mode	Inverter mode (grid-tied)
Input voltage	AC 120 Vrms VL-N, 60 Hz or AC 230 Vrms VL-N , 50 Hz	380-V DC bus Nominal
Input current	16-A RMS maximum	10-A maximum
Output voltage	380-V DC bus Nominal	AC 120 Vrms VL-N, 60 Hz or AC 230 Vrms VL-N , 50 Hz
Output current	10-A maximum	16-A RMS maximum
Power rating	1.65 KW at single phase 120 Vrms or 3.3 KW at single phase 230 Vrms	
Current THD	<2% at 120-Vrms L-N rated load	
Efficiency	Peak 98.7% at 230-Vrms input, peak >97.7% at 120-Vrms input	Peak 98.3% at 230-Vrms output, peak >97.3% at 120-Vrms output
Primary filter inductor	478 µH	
Output capacitance	880 µF	
PWM switching frequency	100 kHz	

So, the TIDM-02008 specification includes an input voltage of 120 or 230 volts with a frequency of 60 hertz or 50 hertz. If operated in the PFC mode.

If you are operating under the inverter mode, it has a 380 volt DC bus nominal voltage as the input. Input current will be 16 ampere RMS or 10 ampere RMS based on what mode you operate. Same way if you are operating in PFC mode the input voltage of inverter mode will become the output voltage of PFC mode. That is 380 volt DC bus nominal voltage will be the output voltage of the PFC mode.

Same way the AC 120 volt RMS 60 hertz or AC 130 volt RMS 50 hertz will become the output voltage for the inverter mode of operation. Output current the same way 10 ampere maximum or 16 ampere RMS maximum for PFC mode and inverter mode respectively. The power rating will go from 1.65 kilowatt if operated at a single phase 120 volt RMS or 3.3 kilowatt at a single phase 230 volt RMS.

The current THD will be somewhere around 2 percent when operated at rated load. The efficiency is around 98.7 percent at 20 volt RMS and it will be somewhere around 98 percent again at 120 volt RMS. The peak efficiency, when operated in inverter mode, is 98.3 percent. Whereas, and if you are operating at 120 volt, it is somewhere around 97.3 percent.

The primary filter inductor as per the calculation comes to around 478 microhenry. Whereas, the output capacitance comes somewhere around 880 microfarad. The PWM switching frequency kept for this particular design is 100 kilohertz.

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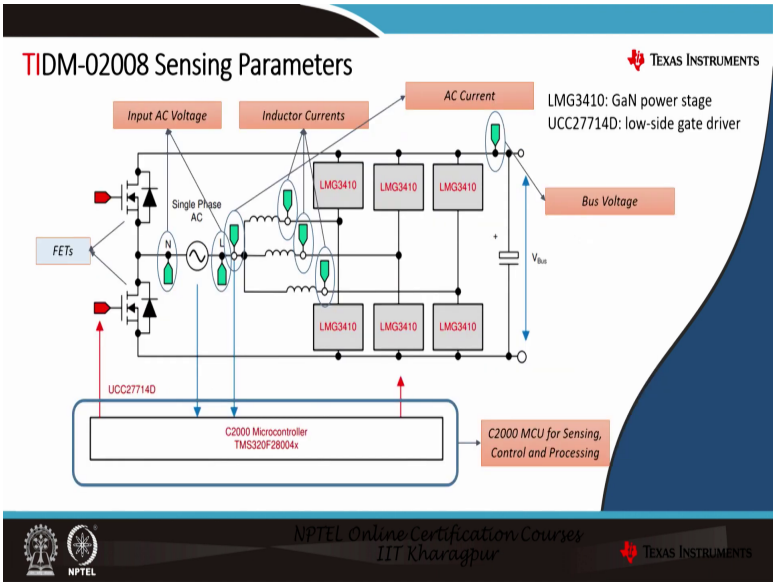

So, moving on to the control side of it, the TIDM sensing parameters that we need for the control are input AC voltage. That is the line to neutral voltage is highlighted. Then there are 3 inductor currents. So, IL1, IL2, and IL3 as highlighted in the picture. Then there is the AC input current that we are sensing and finally, the bus voltage as shown here on the right.

To control all these things fuse the TMS320F28004x device for sensing control as well as processing. There are three additional parts to this one the LMG3410 which is the GaN power stage. The UCC27714D that you see on the bottom left is the low side gate driver and there are 2 FETs sync FET as well as the active FET. These parameters will be used for additional control.

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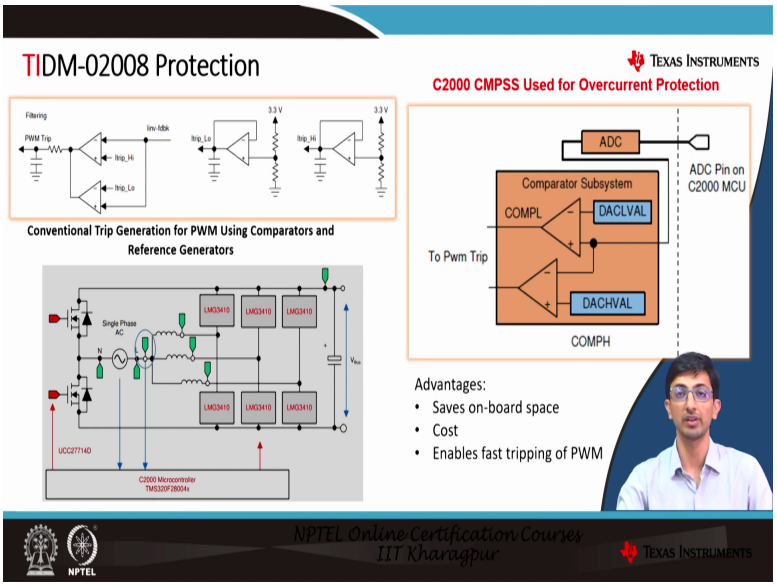

So, moving on the first and foremost important part is protection. So, we will be sensing a lot of currents IL1, IL2, and IL3 AC currents in this circuit for protection purposes. So, first of all, I would like to compare the conventional analog control with the digital C2000 control.

So, the image that you see here on the top left is a representation of the analog control. The right image the 2 right images that you see generate their reference for the PWM trip signals. Strip low, as well as Strip high, will be fed to either the negative input of the comparator or the positive input of the comparator. We have the I inverter feedback coming in which will be compared with the references generated and based on the actual status of the current that is the I inverter feedback current we will generate the PWM trip.

If the current goes beyond a certain limit or it goes below a certain limit. Now, this requires quite an amount of complexity in terms of design. If you are going for if you are opting for a digital controller digital comparator what happens? You get an analog input you throw it to the ADC. ADC will give you a digital output that you can use that you can feed into the internal comparator available with the C2000 for over current protections.

The blue colored blue shaded DACLVAL and DACHVAL that you see are the DAC register that can be user-programmable. So, you need not have any separate circuit that we used to have for the analog part of it. We can simply feed in the value in the registers and based on which we can have the comparators. The comparator output can be fed to the PWM module which ultimately can generate the PWM trip.

The advantages of going to the C2000CMPSS are the onboard space reduction, and the cost advantage since you do not use any external circuitry everything is there on board. And specifically, lastly, it enables the fast tripping of the PWM. Since its hardware is connected internally.

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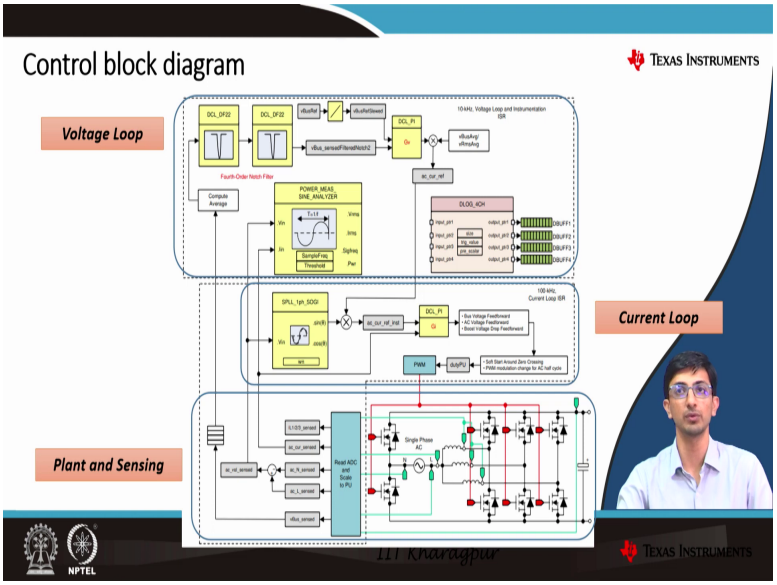

The control block diagram of the TIDM2008 is represented as shown here. The bottommost part that you see is the plant and sensing, the topmost part is the voltage loop and the middle part is the inner current loop.

The plant in plant and sensing what is there is the sensing part of the circuit. So, it will feed all the sensed signals to the voltage loop as well as the current loop. The voltage loop has a band reject filter or a notch filter rather which will generate ultimately an AC reference and feed to the inner current loop. The inner current loop ultimately processes the data and generates the duty cycle required for the PWM and feeds it back to the plants and sensing. This is the overview of the control block diagram of TIDM2008.

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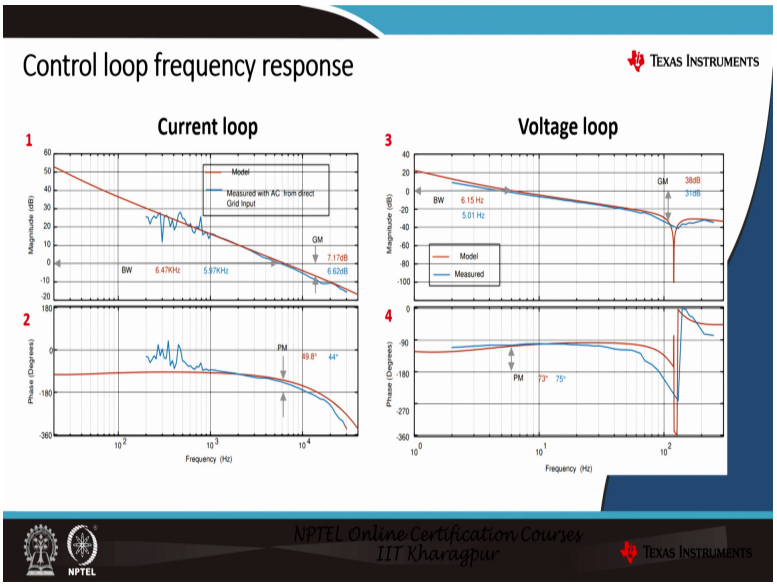

The control loop frequency response observed looks something like this. The red line that you see in images 1, 2, 3, and 4 is the modeled control loop that we design. And the blue line that you see is captured using the software frequency response analyzer which is the SFRA tool available with the C2000 digital power SDK. As you can see here the blue line that is the measured line is almost matching the model that was as per our desired result requirement.

And in the current loop as well as the voltage loop the gain margin, as well as the phase margin, represents that the loop is pretty much predominantly stable as required.

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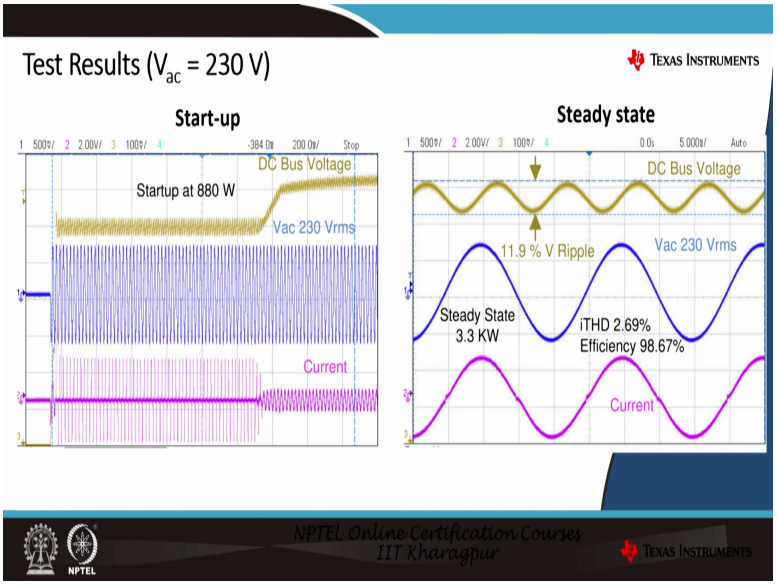

So, the test results that we see here the startup was somewhere around 880 volt and then we moved on to the steady state power of 3.3 kilowatt. The DC Bus Voltage ripple observed during the steady state was nearly by nearly 12 percent. Whereas, the current THD comes to around 2.69 at the full rated load and an efficiency of 98.7 percent.

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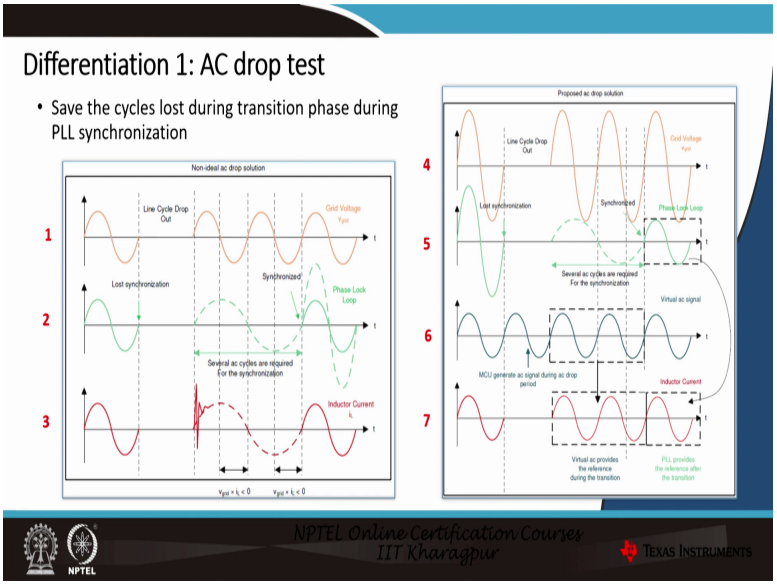

So, there are a couple of differentiations that we implemented using the C2000 device. The first differentiation is the AC drop test. So, as an example in the 1st, 2nd, and 3rd images that you see here. If let us suppose this the line cycle drops out what happens is that? When it again comes back the PLL requires a certain amount of cycles for synchronization back with the grid voltage.

So, what has happened is that we lose a certain number of AC cycles which goes for synchronization purposes. What a proposed solution dictates is that let us suppose the line cycle drops out for whatsoever reason. We will generate a virtual AC signal that is there within the MCU to consider that as a reference for the PLL. So, as an example let us suppose that the line cycle dropped out at some particular instant as shown here in the image.

Automatically the reference will be taken over by the virtual signal that is generated within the MCU and when the line voltage comes back automatically we do not need now the PLL, but we have already the virtual AC signal generated within the MCU which will do our job for the PLL. Which can generate the required result. So, that ultimately saves the number of cycles lost for the PLL synchronization.

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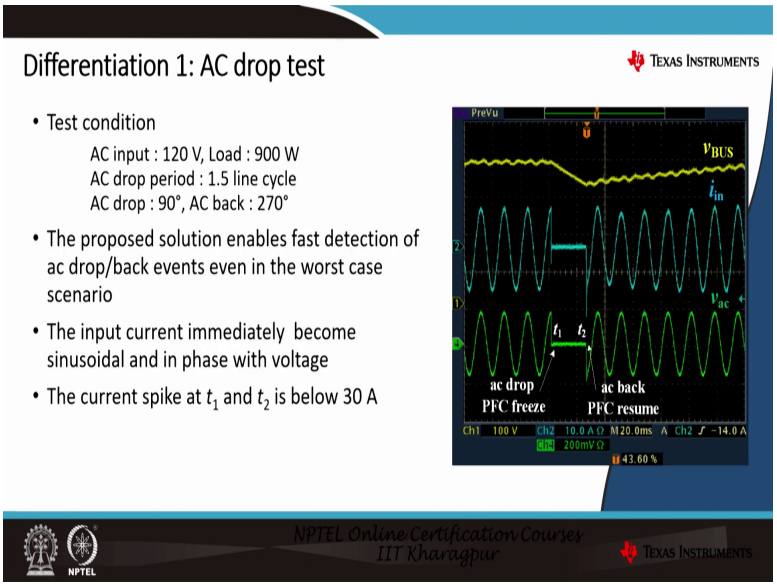

Now, this result has been tested and the test results are shown here. So, the test condition was that the AC input provided was 120 volt. The load was kept at around 900 watts. The AC drop period that we kept was a 1.5 line cycle and that AC drop started at 90 degrees. That is the peak of a sine wave and it was brought back at 270 degrees that are the worst-case again scenario at 270 degrees. The proposed solution as shown here enables fast detection of ac drop-back events, even in the worst-case scenarios. And the input current immediately becomes sinusoid and phases with the voltage.

Moreover, what you can see here is that the current spike at t1 and t2 is basically when the dropout event occurs when the PFC freezes, and when the PFC resumes back you can see that the current also is below a certain limit. The voltage bus that is that you see in the yellow colored image the voltage bus will start reducing because there is no input from a voltage weak grid available. So, that will slowly come down to 0, if this condition drop condition remains for too long.

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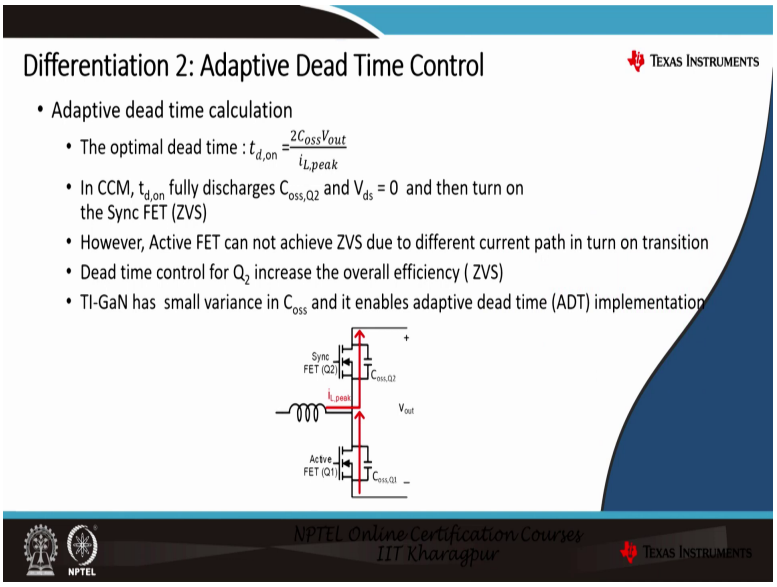

Coming to the next differentiation is the Adaptive Dead Time Control. So, in normal FET conditions what happens is that, if you have a fixed dead time then there are chances that you know you have a spike in current. So, what spike in the peak? So, what we are trying to do here is that you have Coss Q2 and Qc Cos, Q1 for Sync and Active FET FETs respectively.

What we are trying to do is that we have the Coss value already defined. We know the voltage across the Cos that is going to happen and we know the current through the Sync FET. So, what we will try to do is we will calculate the charging time a discharging time required for the capacitor across the Sync FET. Based on the discharging time we will keep the optimal dead time that is required for the Sync FET. Using this what we can achieve is the Z ZVS for the Sync FET operation.

The same thing cannot apply to the Active FET, because Active FET the current passing through the Active FET will vary depending on the mode of operation. Sometimes it may be the peak, sometimes it may be input current as well. So, the Active FET current is not predetermined, and hence the same concept of calculating the optimal dead time is not possible in the Active FET.

So, if we if still even if we achieve the dead time control for Q2 that is the Sync FET we will still be able to increase the overall efficiency using the ZVS additionally one question may arise what about Cos? Is it always constant? There will be some variance, but ti GaN has a

very small variance as compared to others in Cos and it enables adaptive dead time control implementation.

So, this is the formula that will be used to calculate the optimal dead time.

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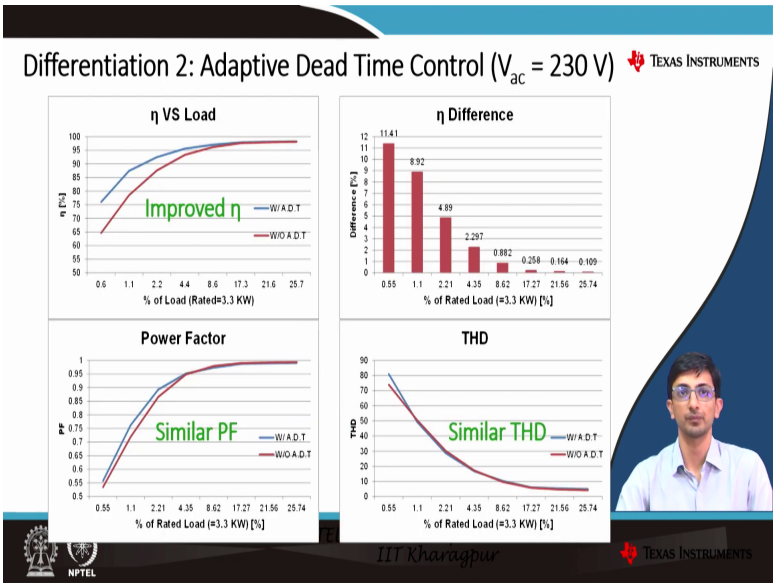

As you can see here in the image. There are 4 parameters that we considered one is efficiency versus load, the second is efficiency difference the fourth third one is power factor and the fourth one is THD and we have compared. One is without the adaptive dead time control, the other one is with dead time control represented using the blue line, and without adaptive dead time control that is using the conventional dead time. We have represented it using the red line.

You can see the difference in the efficiency versus load curve that at a lower rated lower percentage of rated load we have significant improvement in the efficiency. Whereas, as you move towards the higher end of the load the difference in improvement reduces. That same thing you can see here in the image that is on the efficiency reference image.

So, let us suppose that if I look at a 0.55 percentage of rated load then the efficiency difference observed is nearly 11.5 percent, but that 11.5 percent efficiency difference does not remain the same when the load rated load increases when you operate at a higher load. For power factor as well as THD we have observed similar performance.

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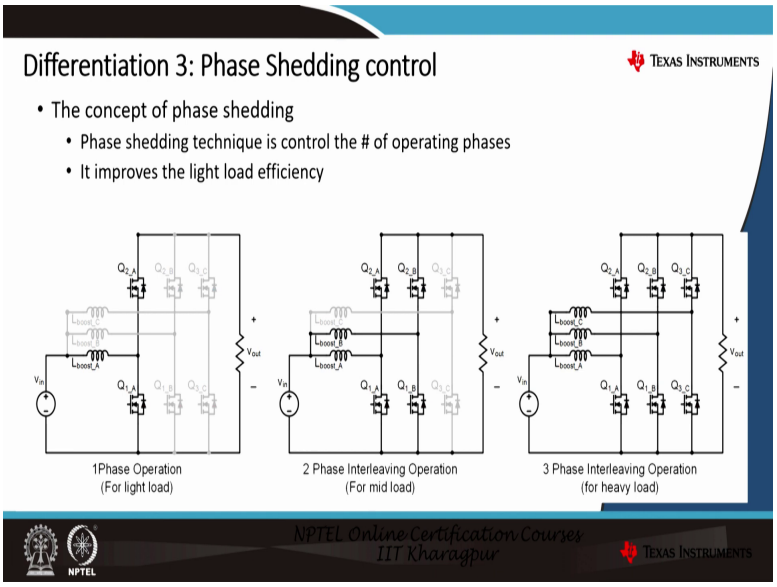

The last differentiation is the Phase Shedding Control. So, the concept of phase shedding is basically that if you have a light load you would not want to operate all 6 switches in parallel because ultimately that will introduce a certain amount of switching loss that will introduce a certain amount of complexity. What you would want to do is that if there is a light load operation then you can only use 1 single phase and eliminate the other 2 phases. When you are having a little higher load that is mid load you can use 2 phase interleaving operation.

And for the heavy load, you can use 3 phase interleaving operation, thereby reducing the number of switches based on the load conditions. Specifically, it does not have any major impact on the heavy load side, but for the mid load you can see a smaller improvement and for the light load perfectly it will give a greater amount of improvement. So, this concept is also implemented using C2000 and the observed graphs are shown here.

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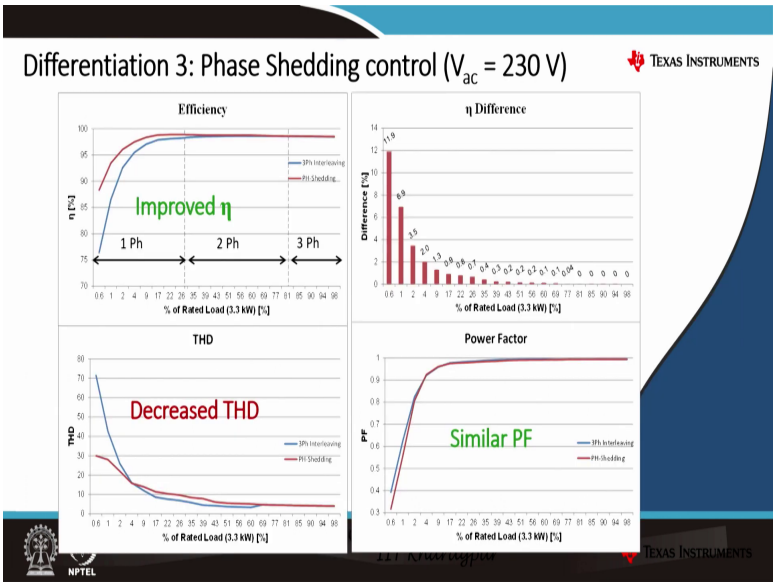

So, in the same way, we are showing the graph of efficiency, efficiency difference, the THD as well as the power factor. The first thing that I will take up is efficiency and as told before we can significantly imprimprovementsthe single-phase operation. So, the blue line that you see here is a 3-phase interleaving operation and the red line that you see here is a phase shedding operation.

So, the in phase shedding operation we can see a significant difference in the efficiency percentage. Specifically talking about the single-phase operation. Then moving on to the two-phase operation that is the mid-load condition we do not see a significant improvement and as and when we move forward to 3 phase operation which is full load condition it almost becomes similar to the 3 phase it has to become similar to the 3 phase interleaving operation.

The same thing can be observed in the image on the right and a graphical manner as well. Where around 12 percent improvement is seen in the efficiency at lower rated load. That is nearly 0.6 percent of the rated load operation. As you move towards 20, 25 percent of the efficiency difference goes on reducing. The THD also has been observed that it significantly reduces and power factor has been observed to be almost similar.

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So, coming to the conclusion part there are certain references which you can take up. So, one is the C2000 digital power SDK within that we have provided all the calculations required for using your inductor, and capacitor as well as some other parameters. And in addition, you can go to the TIDM2008 product page, which gives all the details about the design guide as well as some other schematics that are relevant.

One more device that we used was the GaN LMG3410. So, I have marked the relevant context page over here. And lastly, the C2000Ware Software Development Kits that the fundamental development kit used in all our software's that you can download from TI dot com.

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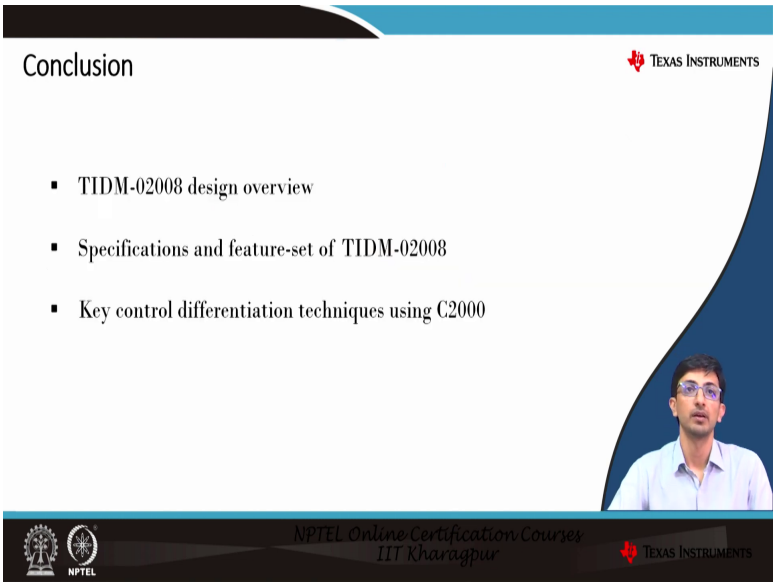

In conclusion today we studied TIDM2008 which is the bidirectional totem pole PFC design overview it's specification and feature set lastly we understood the key control differentiation techniques that are the basic as well as an advanced technique using the C2000 software.

Thank you.