**Digital Control in Switched Mode Power Converters and FPGA-based Prototyping**

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**Module - 08**
**Digital Controller Implementation using Fixed-Point Arithmetic and Verilog HDL**
**Lecture - 80**
**Implementing Digital Pulse Skip Modulation and Experimental Results**

Welcome to this lecture we are going to talk about the Implementation of Digital Pulse Skipping Modulation using Verilog HDL coding programming and also we are going to show some experimental case studies.

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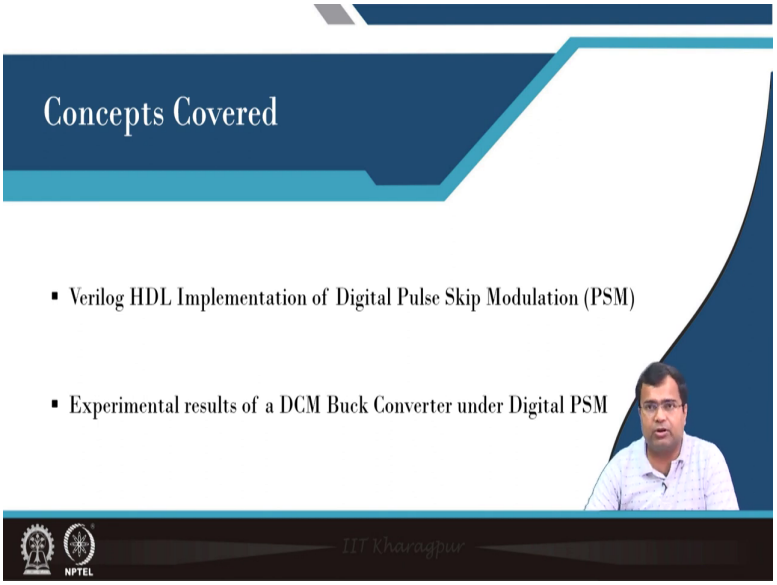


So, in this lecture, we will talk about Verilog HDL implementation of digital pulse skipping modulation and the experimental result of a DCA buck converter under digital pulse skipping modulation.

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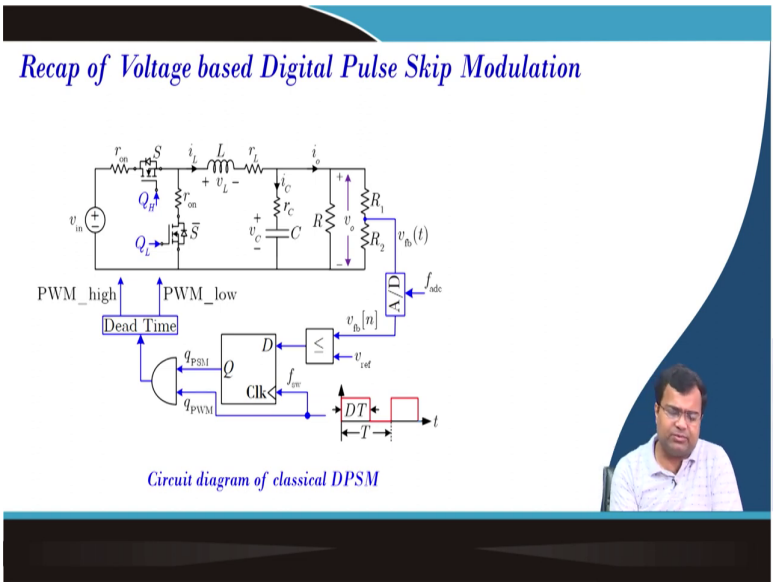


So, if we recollect our digital pulse skipping modulation we are talking about a very basic digital pulse skipping and we have discussed this in the previous lecture on this operation.

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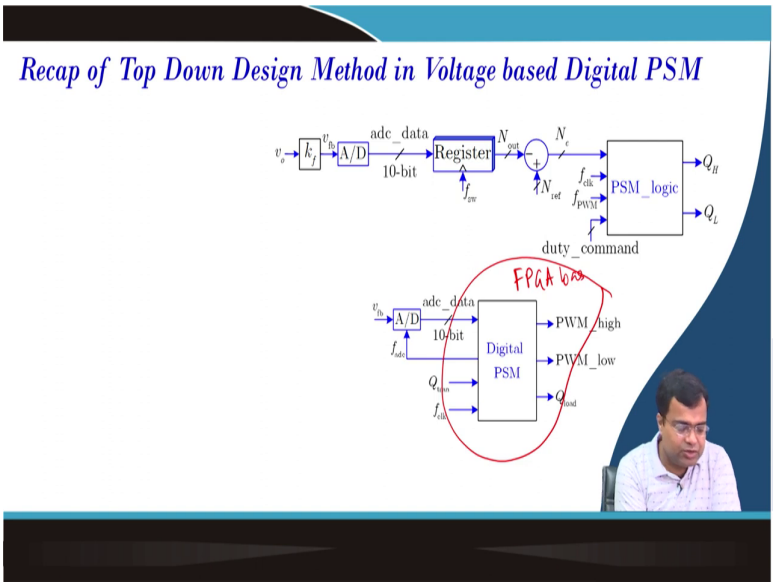


And we want to design this block inside the FPGA; that means, this will be our we have to design FPGA base implementation.

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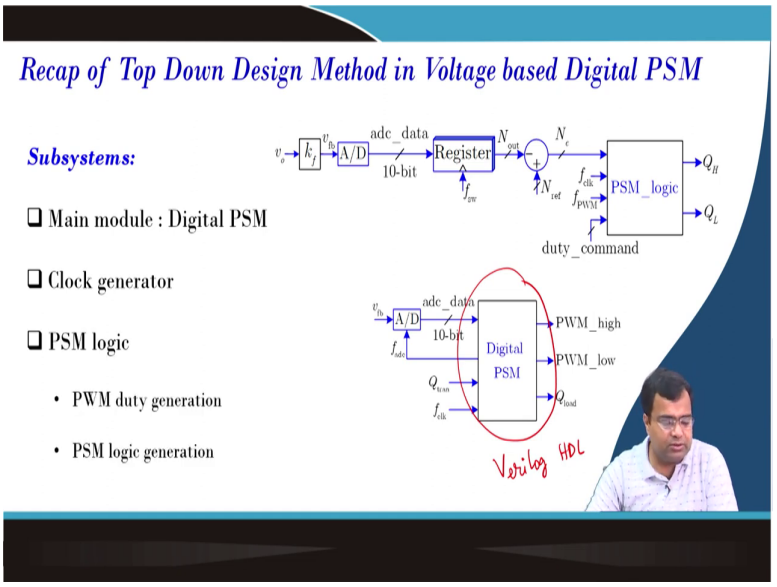


So, I would say we want to design this block, this block we want to design using Verilog HDL, we want to write Verilog HDL and we want to prototype using FPGA. So, we have started the discussion of various modules, so we will consider one main module and two other modules.

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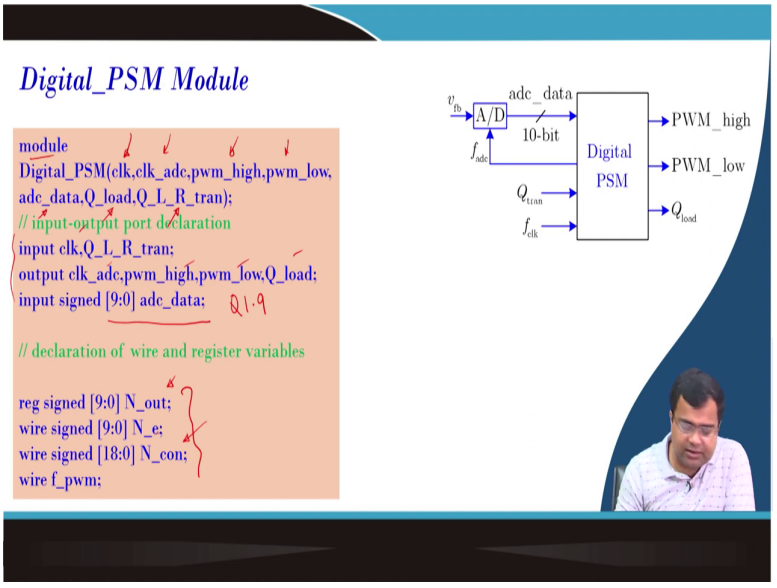


So, let us go back to the Verilog.

So, this is our module the module name is digital PSM then bracket all the input-output ports and this will interface with our real world; that means, you say file with the actual device pin.

So, you need a high-frequency clock then the ADC clock PWM high signal PWM low signal ADC data that will be used and we are also giving some transient to load Q load and then the type of transient. So, here we are talking about we are not considering a transient case study yet, because when you go to multimode only this makes sense. Because if you go to high load and operate in pulse skipping this is not desirable because there is no pulse skipping ok.

Because I will show you even if you decrease the input voltage if you fix the duty ratio at a certain voltage there will be npulse-skippingng operation and as a result, there will be no output voltage regulation also. So, here we have to declare the port input-outputt port. So, that clock ql r is the input ADC clock PWM high PW low Q load is the output.

And this is a sign data coming from the ADC and this is in the Q 1 dot 9 format in 2 s complement. Then this part we have already discussed that we are talking about output then control signal ok and then error.

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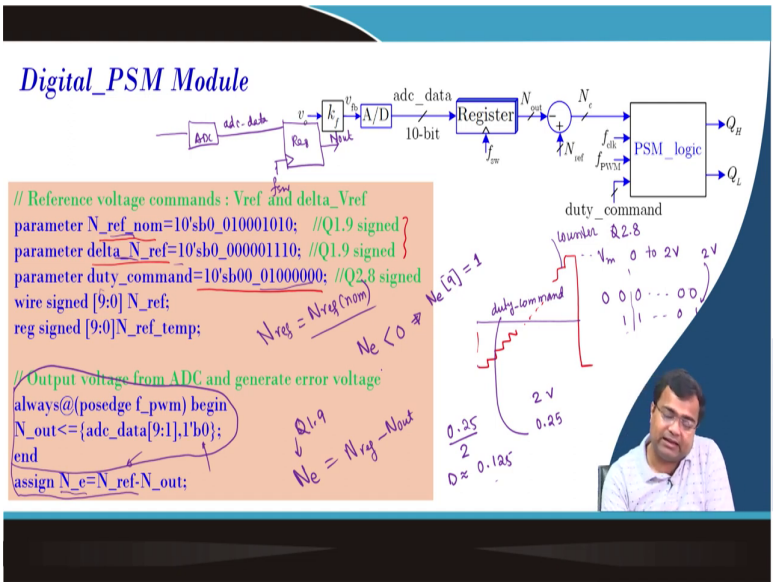


So, here we are defining parameters we can make a reference transient that provision is kept, but in this lecture, I am not going to show the result.

So, this thing we have discussed in our both digital voltage mode and current mode control; means, we will consider one reference nominal value and another er delta reference. Sat we

can add them up to make a reference transient the duty command we are taking here it is 2 dot 8. So, these are Q 1 dot 9 and it is Q 2 dot 8.

That means if you consider the duty ratio; that means, we are talking about this will be compared because we will be comparing this thing with a sawtooth ok. Now, how do I generate the duty ratio? The So, duty ratio is here which will call duty command and we are talking about this counter which is for RAM this we are talking about Q R 2 dot 9.

Because you need a 9-bit resolution and the counter; that means, for this RAM voltage we can say V m or what it should be positive and we are talking about the RAM voltage varying between 0 to 2 volt, that is why the counter can take the value from. the for this counter the first bit will be 0 then the next bit will be 0 0 0 0. So, it will vary from this 2 maybe 1 close to 0 1. So, whatever corresponds to 2 volts will consider.

And in this Q format 2 dot 9 we are considering 2 dot 8 because we can drop. So, the counter is also 2 dot 8, not 2 dot 9 I am sorry, because it requires a resolution of 9 bit. So, it will take 8 bits in the decimal and 1 bit in the integer. So, this is a counter. In this context, the counter can be almost all 1 to get 2 volt. Then what will be the corresponding value?

So, if you consider that if you take all 1 so; that means, all 1 is 2 volt then this duty command will give rise to 0.25; that means, we are talking about 0.25 by 2 and the duty ratio will be you know; that means, it will be how much 0.125 that is the duty ratio that we have considered ok.

So that means, it is a lower duty ratio only and reference so here we are actually capturing the signal sorry this point this particular part is used as if we are getting a stream of data from ADC and that is our ADC data and we are using a register and register has a clock of f sw. So, at this value, we are getting the, which is called N out ok. So, the register is capturing data at the edge of this clock and this is the, what and then we have taken the error voltage.

So, here error voltage like in actual voltage we write V ref minus V out. Here V out means it also data means it we are also considering you know the step-down and other feedback gain everything. So, the reference has to be scaled accordingly if you directly take output voltage you have to take the reference voltage, if you scale down by a feedback factor this has to also scale down.

Here we are intentionally discarding the LSB. So, we get a lower resolution of the ADC, so that we will not encounter any you know limit cycle oscillation issue. And as usual,w e have discussed that this reference is taking from either nominal or this nominal plus delta V ref, but we are considering here N ref to be equal to N ref nominal. So, we are not making any at this point of time any reference transient.

So, now we are talking about N e which is N ref; that means, N ref minus N out, so just to avoid any confusion we can remove this particular term. Now, you know if N e is negative, what does it mean? That means, the output is higher than the reference and this N e is a significant number it is in Q 1 dot 9.

So, N e is negative it implies that sign bit because the 9 bit will be equal to 1 because it is a 2 s complement any negative quantity will have a leading bit 1 and if N e is greater than 0, then the sign bit number will be 0 and this is very important because this will decide our pulse skipping operation.

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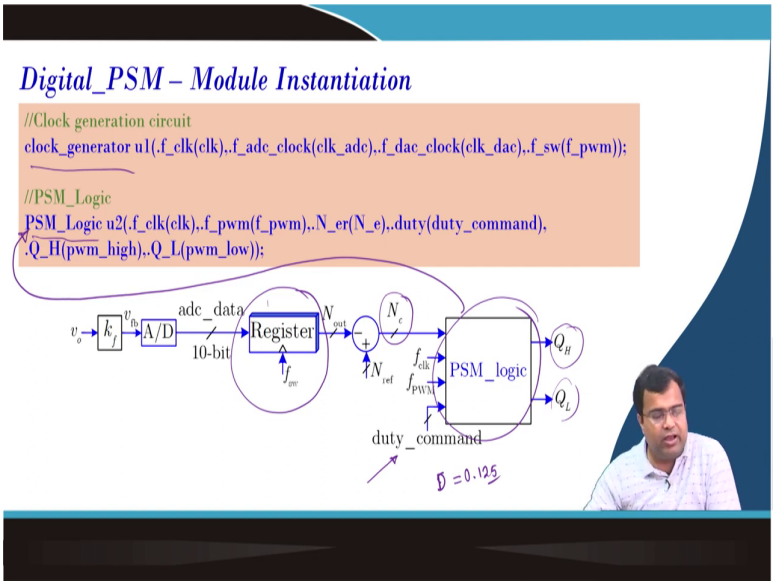


So, for this clock generator, we are instantiating one clock generator and one PSM logic. So, this is overall, so this register we have discussed we are taking data from V dc.

We are discarding 1 bit here and then we are generating the error voltage and this is going inside the PSM logic block, so which is here PSM logic block and PSM logic block are

generating Q H and Q L and we should remember that we are given a duty ratio comment to achieve a duty ratio of 0.125 that we have discussed.

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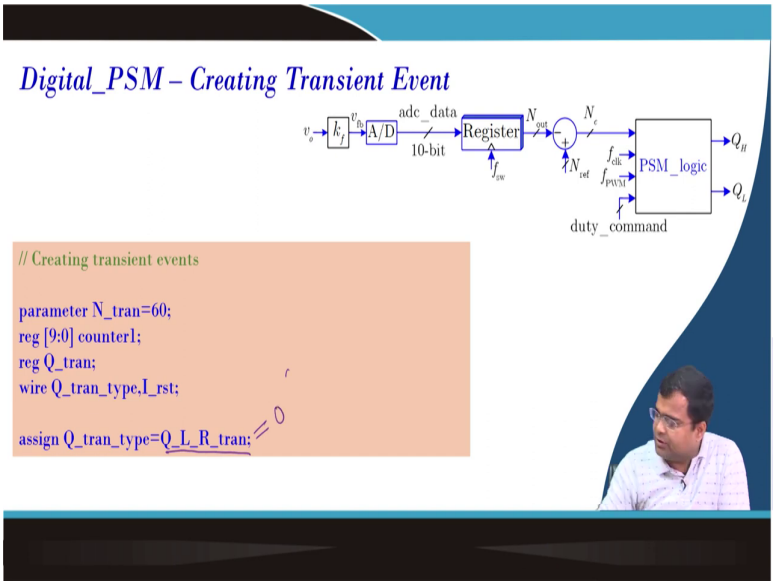


So, we are not going to discuss now creating transient. So, this part we can drop this because we are we may or may not want any transient.

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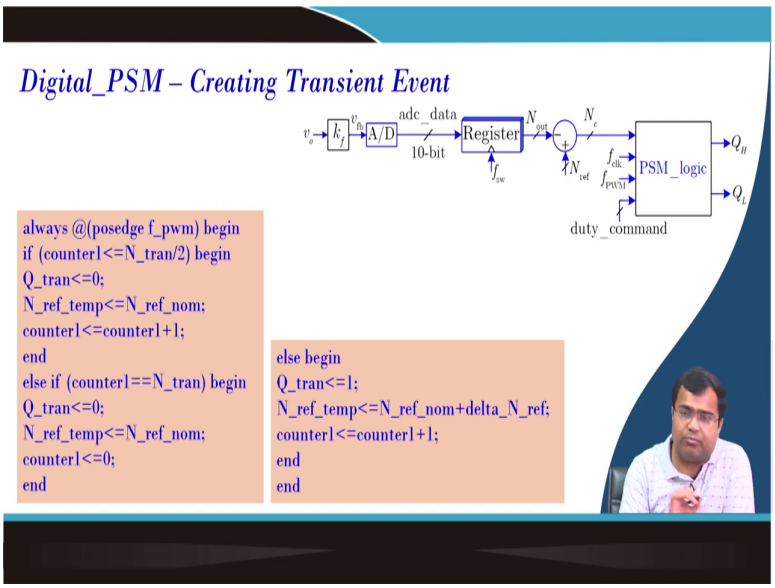

So, you can see that N ref we are directly we can consider reference command as well, but for this particular case study we are directly we are not making any reference transient; that means, we are not doing any transient.

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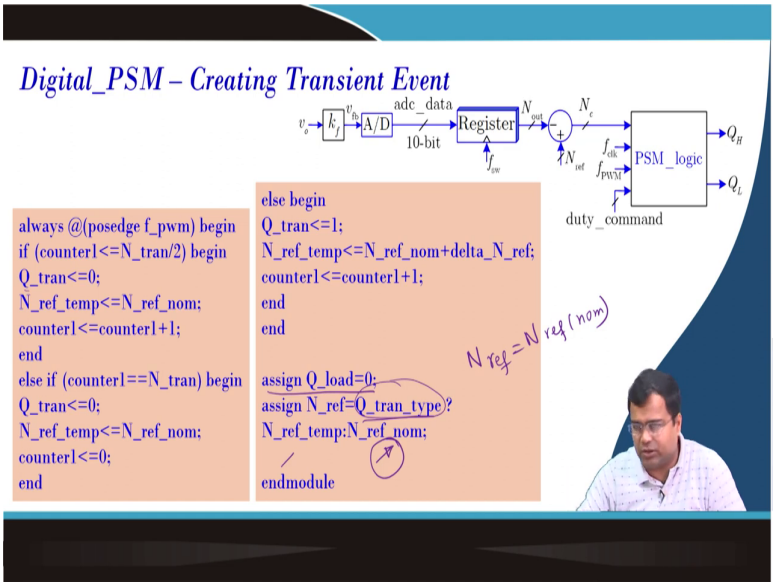


You can see the Q transient is 0; that means, there is no reference transient. So, Q transient is 0 sorry. So, here we are setting the load transient to be 0 and the option that we are giving Q tran type; that means if you go to the Q tran type; we are giving the assign external load. And here externally there is a switch when I go to the demonstration, so that switch will place in a position; that means, it will not make any transient.

So, if you take this guy to be 0 then what will happen if this is 0 it will take nominal sorry it is 0 means it will take the right side of this value. So that means, we are considering N ref to be N ref nominal we are not making a transient, but if you set this to be 1 and we will take the reference transient.

So, when you show the live demo we will show this case.

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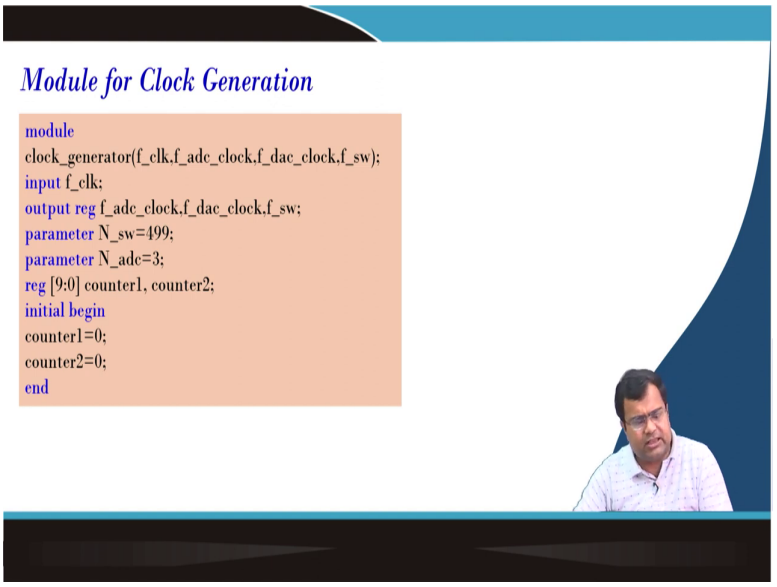


So, now the module for clock generation we have discussed for both current mode and voltage mode control. So, this part I am not going to discuss we have discussed sufficiently in sufficient detail these are the block.

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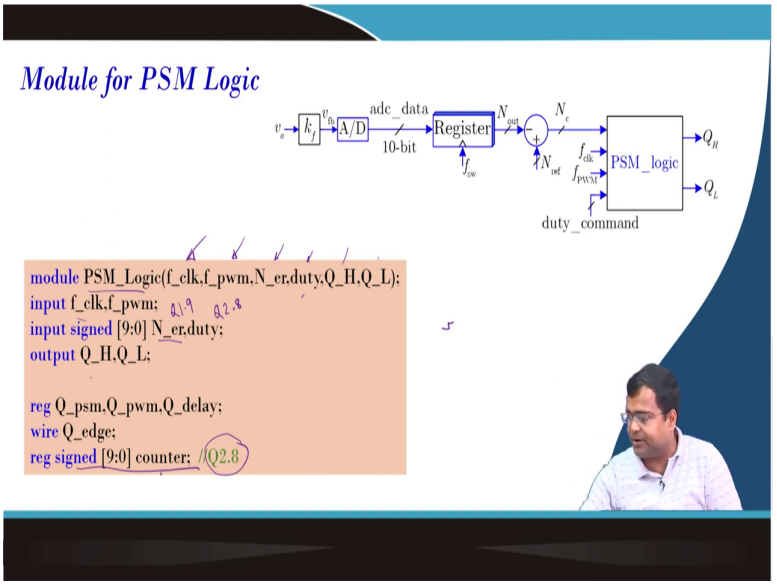


But we want to consider the module for PSM logic which is simple. So, for the PSM logic, we need to provide the f clock high-frequency clock because it requires a counter DPWM counter.

Then f PWM switches frequency clock and then error duty ratio error voltage and then duty ratio comment then it will generate Q H and Q L. So, the input is f clock and f PWM the input is also signed error voltage and the duty command. Though it is a 10-bit number, the Q format, in this case, is Q 1 dot 9, but in this case, it is Q 2 dot 8, but their number of bits is the same.

And the output is a Q H and Q L and then we are defining the register and we are getting a counter this counter will be a sawtooth generator which will be 2 dot 8. So that means, this counter and this duty ratio Q formats are the same because they have to be compared.

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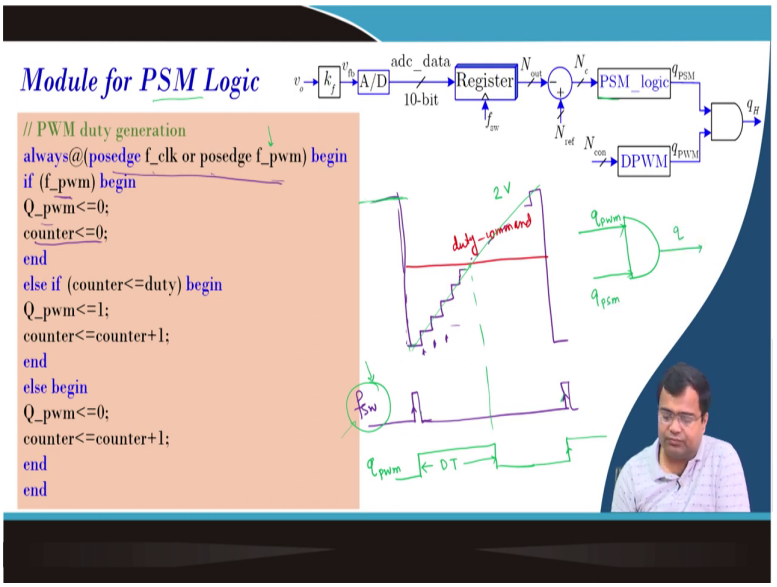


So, you see always at the rate f clock we are taking the posedge of the pwm, if the pwm signal is high then Q pwm is 0 and counter 0 else. So that means, it is the beginning, so what is this logic? That means, you see this is like this. So, we want to sync this counter with the switching frequency clock. So, this is my fsw and these are the edges of the f clock to increment the counter.

So, you see whenever the first edge comes it will go inside this block this clock edge is also because it is the highest frequency clock. Once it says it is high you see it is high then it will reset this counter, so that is why the counter is reset and that is the time the Q pw is also 0.

Now, whenever this goes low then your cow Q pw is high because we want to generate a pwm signal and pwm will compare up to the duty ratio value. That means if we check this is

my duty ratio comment this is my if you remember the duty comment. So, here this will generate you know this if you go let's say if you hit. So, you will get Q pwm to be high, so this is my Q pwm ok, and this corresponds to our duty ratio d t that we want to define.

So, it will do so; that means, each switching period this will happen duty ratio will be generated. So, the objective of this block is like a DPWM counter we are using an external f w PWM clock otherwise you may not need this block itself but can generate PWM whenever the counter is reset.

So, here we are as if you are using a clock synchronized counter the counter reset is happening with the switching edge of this fsw clock because we have used a separate clock generator circuit. If that was not I mean if we do not generate fsw from here then we can do it by the same logic if the counter hit the upper limit of the PWM then we will reset, so these things are possible.

Here we are using an external switching frequency clock because sometimes the switching frequency clock can be provided from outside. So, this feature is given this PSM logic will work even with your external switching frequency clock suppose I want to operate the PWM frequency differently. So, I can sync with the clock and whenever this edge comes I will simply reset the counter.

Again it will reset here, but till the time the next clock comes, the counter will continue to increase. So, this is what is happening ok and we want 0 to 2 volt during this time. So, accordingly, we have to set the resolution in Q format. Now, whenever the duty ratio come common to come, so the Q pwm is defined, so this is your Q pwm. And we know that we need q pwm and q psm and this will generate the actual q ok.

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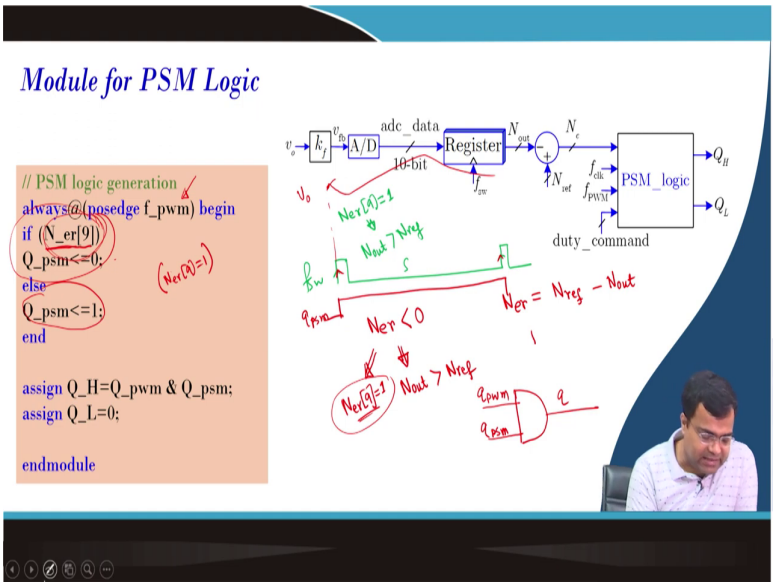


So, what is next now at every edge of this clock? So, if you go back to the basic operation of this circuit you know.

So, every edge of this clock; that means, you know instead of going, so let me bring this thing yeah. So, here this is our fsw clock and we have discussed that at every fsw clock if we draw the output voltage waveform, let us say the output voltage waveform is like this. So, if it was going down then it will go up like this. So, it will check the status of the output voltage with respect to the reference voltage we are talking the sample voltage.

So; that means, you remember what is N er that is my error signal and we have discussed if the error is negative what is N e it is nothing, but. So, it is inside the local variable in this case it is N er ok because these are inside the block. So, N er eventually is nothing, but your reference minus N out. So, N er negative; means, your m this implies N out is greater than N ref; that means, your output voltage is above the reference voltage. So, you have to skip the pulse.

So, this will result in N er 9th bit being 1 because it is a 2 s complement and that is why if this is one this statement will be executed and it will set q psm to be 0; that means, it will keep the pulse. Else this will be non this will be 0 because this will be one whenever say inside any logic is activated when it is 1 equal to 1.

So, here as if your N er 9 bit is equal to 1. So, it will be skipped otherwise q psm a 1 and q psm we have discussed that this is q pwm and this is q psm. So, this is q if the q psm is 1 it will simply plus the pwm for the entire cycle because it is this statement will only be executed at the edge of the cycle.

So, if it is 1; that means, this Q psm will be activated for the whole cycle of Q PSM and during this cycle, it will pass the PWM signal. And if the next cycle it sees the output voltage goes below the reference voltage then N er 9th bit will be 0 and this statement will be executed, so then it will charge cycle it will enable. And if sorry actually I just the statement should be like this.

If we found that in this case N er 9 bit equal to 1 which implies your N out is greater than N ref, so then this will be a skip cycle.

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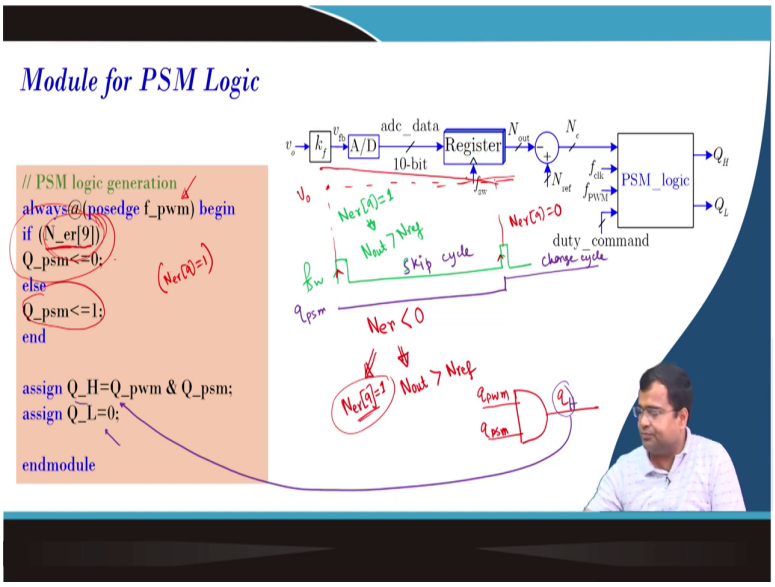


In that case, this will be in this case what will happen you are sorry to continue 0. So, then the output voltage waveform will not look like this, because if it was higher and it is coming in, so this whole cycle voltage will drop. Whenever it crosses this cycle let us say this is V ref if V ref then this cycle will be 0.

So, in this case, let us say N er 9 bit equal to 0 then what will happen? So, this was 0 this will go high for the whole cycle it will go high. So, this is my q psm. So, when the q psm is 0 q

will be 0, so it is called a skip cycle. So, this cycle is called the skip cycle and this cycle will be called the charge cycle ok. So, this method will continue.

Once it is decided you see Q H is nothing but this we are calling Q H directly we are giving because we are using it in diode mode. So, there is no dead time is required and the low side switch is simply set to 0.

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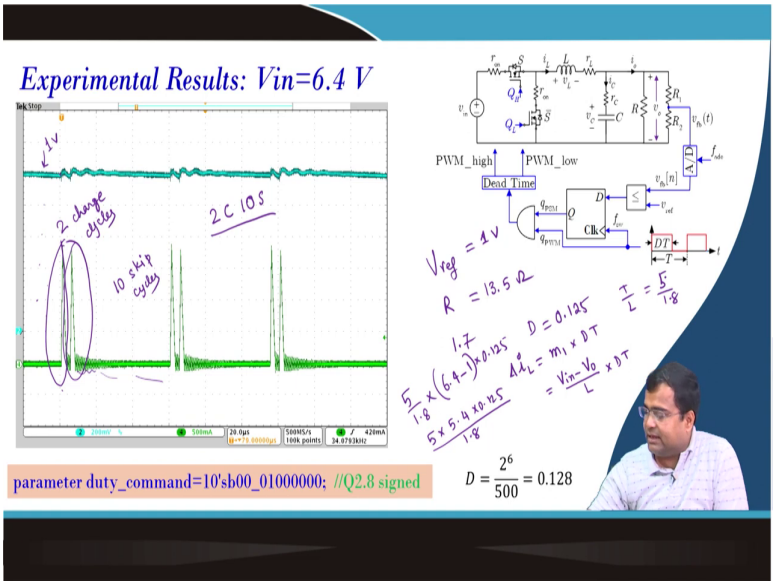


So, this is the experimental result for 6.4 volts we have taken some voltage, where V ref because we want to say that V ref will set to 1 volt; so output voltage should be 1 volt you can see 1 2 3 4 5. So, this is at one volt ok and we have considered load resistance to be 13.5 fixing it.

So, at 6.4 volt this is a current ampere so; that means, this is like what is the peak current limit. So, peak current is 500 milli ampere, so 1 2 3 4 almost it is like you know 1 2 3 1 point 1.7 or something. What was the duty ratio we found? It is 1 point 0.128 or 0.125 whatever.

Now, the time period we know so; that means, what should be my current ripple? It will be m 1 into DT; that means, D into T. What is m 1? It is V in minus V 0 by L into DT. Now, what is T by L? So, T is 5 by 1.8. So, 5 by 1.8 is a T by L then what is V in minus V 0 it is 6.4 minus 1, and that this into 0.125. So that means, it is coming to be 5 into 5.4 into 0.125 divided by 1.8 and you can find out you can calculate it, it will be coming close to this current.

And interestingly here if we take the AC couple ripple the output voltage is lower than this at this edge so that it undergoes a charge cycle; that is why it is turning on. Now, the next cycle also output voltage is lower, so two successive charge cycles.

So, there are two charge cycles, and here is 20 microsecond, and what is our switching frequency is 5 microseconds. So, each will have 4 cycles so the skip cycle is 2 cycles here 4 4, so 10 cycles skip. That means, we are getting 10 here we are getting 2 skip 2 charge cycles and 10 skip cycles, ok, again followed like this.

So that means, we are getting 2 charge and 2 and 10 skip.

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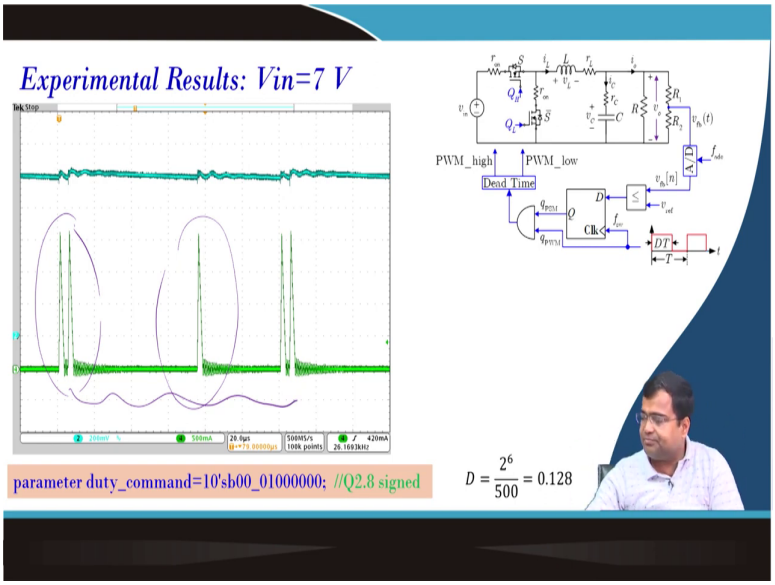


Now, what will happen if we decrease or increase the input voltage to 7 volt?

Now, you see when you increase; that means, your current has gone up, so that injected. So, you can see here; that means, this is a charge balance, so in two subsequent cycles when there is a charge cycle your inductor current is positive. So, it is injected energy from the source to the converter and that is going to the load side.

So, the charge balance is happening over 2 charge cycle and 10 skip cycle. So, effectively 12 cycle switching cycle is your effective time period is a balancing. Now, suddenly you have increased the input voltage since the duty ratio is fixed, so naturally current will go up. So, you are giving the excess charge, but the load remains the same because it is 13.5 ohm and the output voltage is 1 volt.

So, since you are giving excess. So, what will happen is there will be again 2 charge cycles may be more number skip, but they will not balance perfectly, so it may it will undergo 1 charge cycle. So that means, this phenomenon you can see is not happening periodically or they are somewhat unpredictable.

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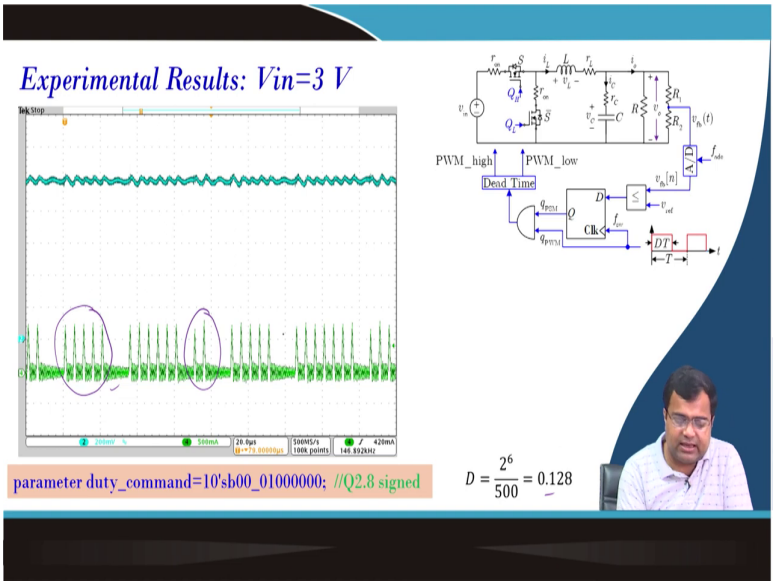


But if you decrease the input voltage you will see you will find more charge cycles because the duty ratio is fixed the current got reduced. So, you are actually injecting less energy, as a result, you will need to inject more number cycles, and then only you can have a skip pulse and then only the charge. So, it is all about the charge balance of the capacitor.

So, the capacitor load current is fixed, but since the duty ratio is the same if the input voltage is lower; that means, the injected charge in the charge cycle will be less, as a result, you need to give more charge cycles to anticipate the discharge period. So, the charge balance, is why the number of skip cycles is less.

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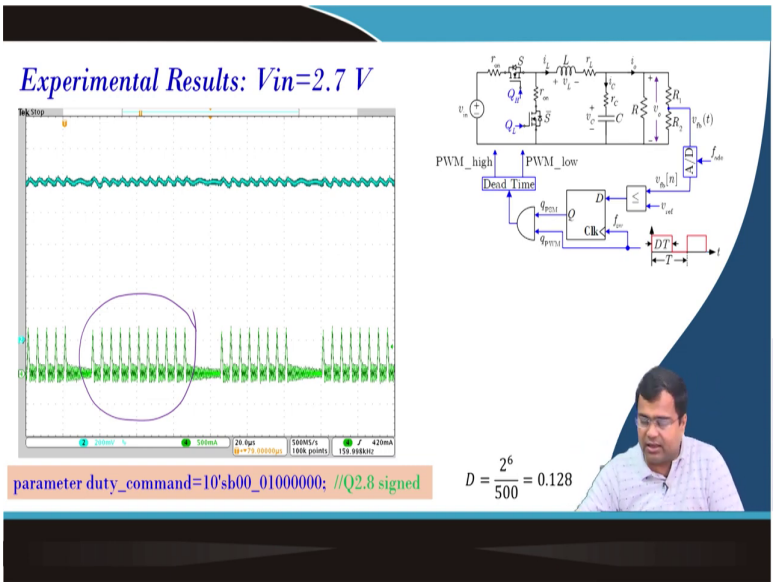


If we make further reductions you see the number of charge cycles is increasing because you know here that after this case 2 charge cycle there are skip cycles like this. But if you further reduce the series of charge cycles will increase and then only the skip cycle will happen this is around 2.7 volt.

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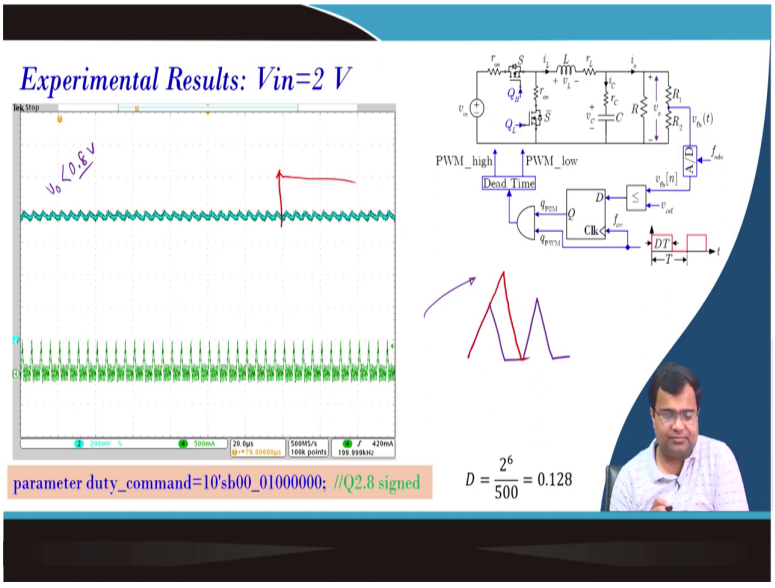


Now, if we make 2 volt then since the duty ratio is fixed the current has gone down and this is the operation where you in a charge cycle how much energy is injected is not sufficient to

maintain the voltage balancing issue. That is why you can see it is coming to be less than 8 volts, where we want sorry less than 0.8 volt.

So, here we are getting an output voltage of less than 0.8 volt where 1 volt is the regulation point; that means, as I discussed that if we decrease the input voltage if the duty ratio is fixed then your injector energy is not sufficient for this case. And you need to either increase the duty ratio because that is the only way so that you know in one case it was coming like this.

If we increase the duty ratio what will happen then only you can go further and if you increase inject more energy then it may be possible to take this voltage up to this regulation point ok.

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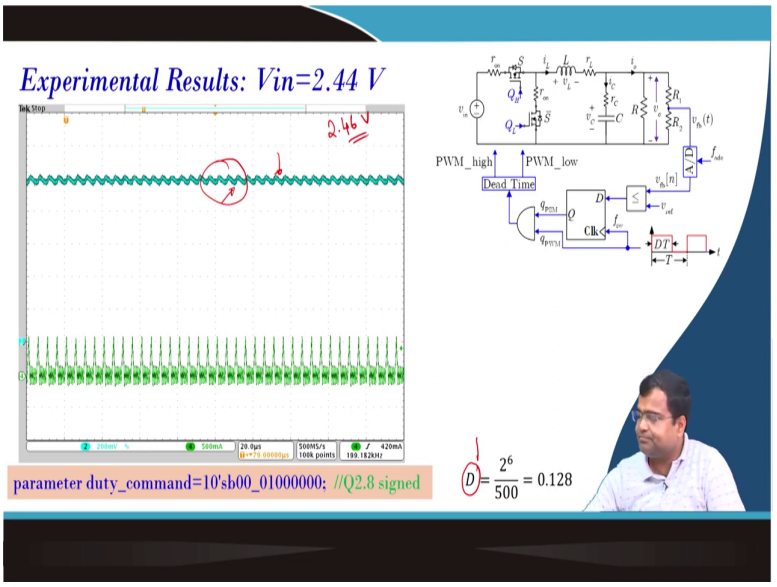


And that is exactly what is happening at 2.44 it is going close to the regulation point, but it is the pulse skipping has not yet started.

So, if you slightly increase, we saw around 4.6 or so the pulse skipping just started; that means, the actual pulse skipping operation should happen in this case is around 2.46 and above below that it will go to the regular PWM operation where since it is the open loaded ratio there will be no regulation in the output voltage and which is not desirable. So, that is why we need to adapt this duty ratio if we saw that there is a frequent you know charge cycle, and from the error calculation if you find that the error is always down.

So, you can put a counter and we can slowly increase the duty ratio using a slower loop because it should not interfere with the regular switching frequency then there will be a non-linear phenomenon will happen.

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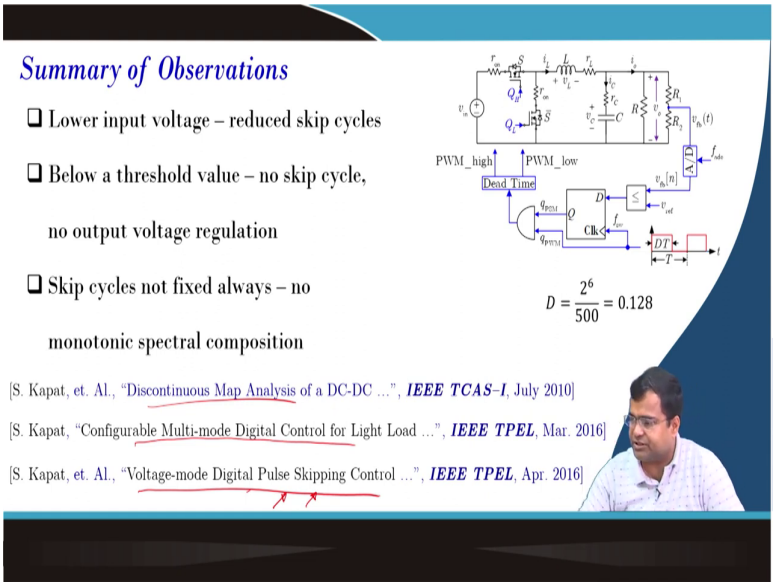


So, a summary of observation and lower input voltage the number of skip cycle was getting reduced below the threshold value of no skip cycle and there is no output voltage regulation and the skip cycle is not fixed always; that means, several charges and skip cycle it was not always happening periodically. And that will lead to nonmonotonic spectral composition this was first reported in this paper that how nonmonotonic spectral composition can come and what are the non-linear aspect dynamical aspects.

Then further techniques were proposed; that means, with this technique you can get always a periodic stable behavior by you can also customizing the number of the fixed cycle here, it is a configurable controller where you can have multiple types of light load control with spectral padding also under light load condition.

But this technique gives you the number of pulses skipping you once it is always possible to define and predefine the skip cycle that way it will allow you to optimize the overall efficiency under light load conditions, but this technique requires closed loop operation even under light load. So, that can be overcome.

So, this gives us some aspects of research for future research.

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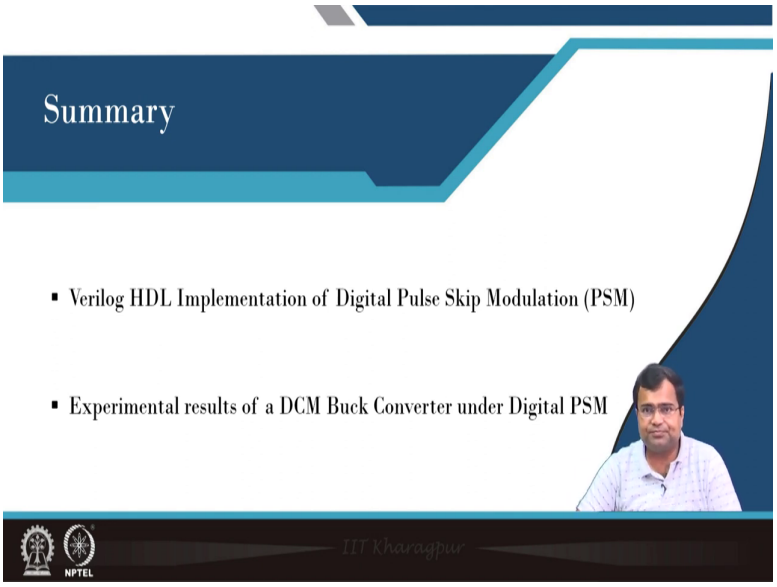


So, in summary, we have discussed Verilog HDL implementation of digital pulse skipping modulation, then we have discussed the experimental results we have shown of a buck converter. And we have discussed some case studies and we have summarized some observations I hope that will be very useful.

But if the power level is low the spectral composition monotonic spectral composition may not have a significant impact on the EMI, but still, it gives us to know the opportunity to think and explore other light load control techniques. And in this course, we will also consider constant on-time light load control in the subsequent lecture, which is also very popular.

And we will also combine PWM with PSM or PWM with consonant type to get multimode, where we want to get wide load current operation where the high load will operate PWM light load will go for either PSM or consonant type. That is it for today.

Thank you very much.