Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 01
Introduction to Digital Control in SMPCs
Lecture - 08
Levels of Digitization in Single-loop Feedback Control in SMPCs

So, welcome to this lecture we are going to talk about various Levels of Digitization in Single-loop Feedback Control in Switch Mode Power Converters.

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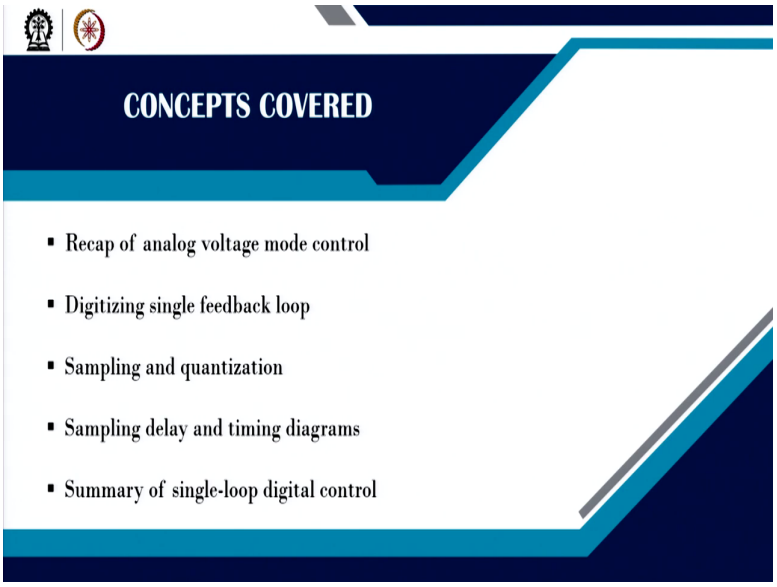

So, in this lecture, we are going to talk about we want to recapitulate our analog voltage mode control, which is a single-loop control. Then we will talk about how to digitize the single feedback loop. Then what are the sampling and quantization with some waveforms and then we also want to discuss sampling delay and timing diagram? And finally, we want to summarize single-loop digital voltage control what is the overall architecture.

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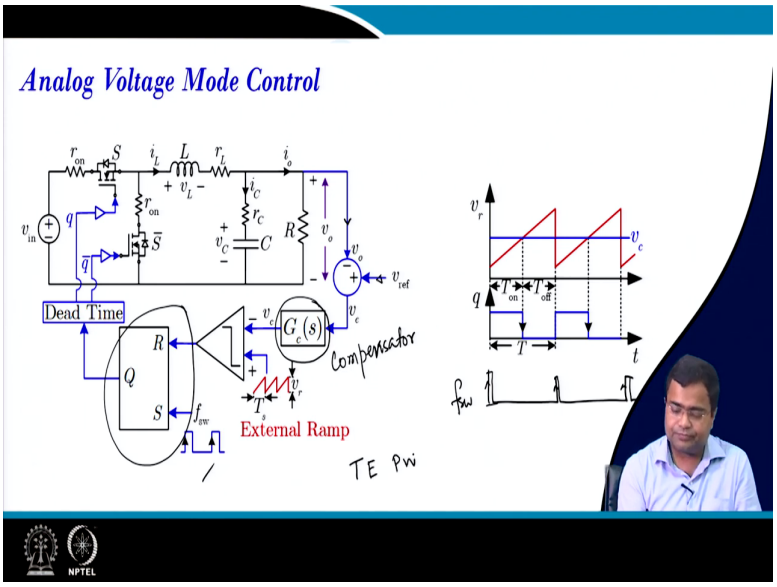

So, if we talk about analog voltage mode control which we have discussed extensively in our previous lecture, you know I think lecture number 6. Here we are talking about a voltage mode control.

In this voltage mode control, we have this outer voltage loop because this is an output voltage, then it is compared to the reference voltage the error voltage goes to the compensator. So, this is our compensator and then this is our compensator. The output of the compensator is compared to the sawtooth waveform and that comparator output goes to a latch circuit that we have discussed ok. And then there is a dead time that as well as the gate drive, so which will generate the respective duty ratio.

Now, in this control, we have discussed that it is under trailing edge modulation where we will have a switching frequency clock this is the clock and if it will turn on at every switching frequency clock ok. So, this will be the switching frequency clock edge, so this is our fsw. And it will turn on at every switch rising (Refer Time: 02:13) using a switching clock; this technique is called Trailing-edge modulation and we have discussed Trailing Edge PWM.

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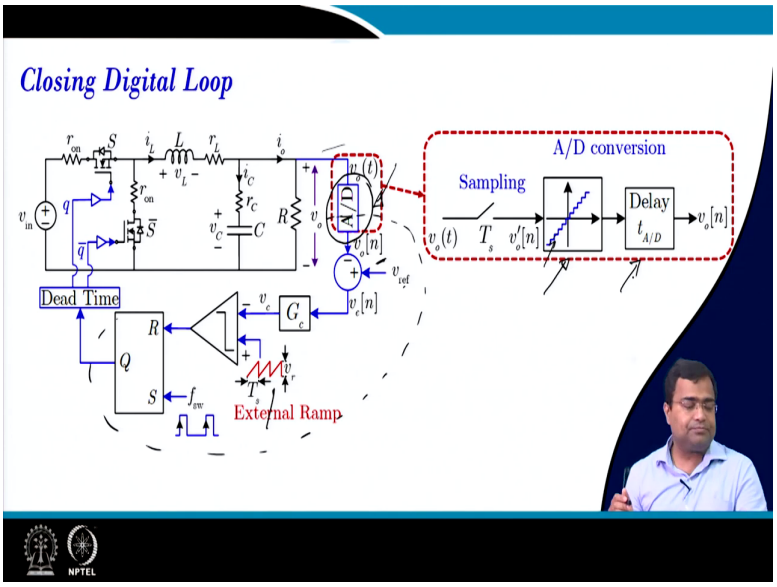

If you want to close the output voltage loop, then first thing again we want to the first thing is required we need to digitize this voltage signal. That means this is the output voltage. Again we may not use a straightaway ADC we may have to use it as a resistive divider or op amp buffer circuit.

But anyway in general if we consider the basic block we need an analog-to-digital converter. This will generate the sample as well as the quantized output voltage. And this output voltage will be compared to the reference, so it may look like from here onward you will have digital blocks because the output of the ADC is digital.

So, the reference has to be digital ok because we need to match the domain we cannot have any digital signal compared to the analog. So, all should be taken into digital, or all signals can be kept into analog, so here we are talking about the digital signal. Now this ADC means for the basic two things in an ADC we have a sample and sampler as well as sampler hold will be there because ADC will also have a register, so it will also hold.

And also it will have a finite resolution because every ADC whether it is 8-bit, 10-bit, 12 bit. So, depending on the bit size the resolution of this staircase will change. So, in high resolution, this staircase will slowly become a straight line. So, the size of this step will be reduced if you increase the bit size. But if you use a higher bit ADC naturally this number of large data has to be processed through a digital system and as you increase the bit size. Let us say on our computer we talk about 64-bit machines and 32-bit machines.

So, suppose you have 8-bit data, and if you have 12-bit data. Naturally, for 12-bit data for the same clock rate your hardware resource will increase and the power consumption will also increase. So, to limit the power consumption because we are all talking about, a high-frequency power converter where the whole thing can be a single IC. Every power matters.

So, we cannot use arbitrarily large bit sizes we have to be very careful ok. And you will also see that this staircase will also have a quantization effect and in the subsequent lecture we will show even in hardware that there is a certain requirement of this quantization as well as the ADC quantization, otherwise, you will end up with a limit cycle oscillation.

So, here this A to D converter has a sampler and it will also hold because of the resistor and it will also have a quantizer. But every ADC will have some conversion time and that is represented by the delay.

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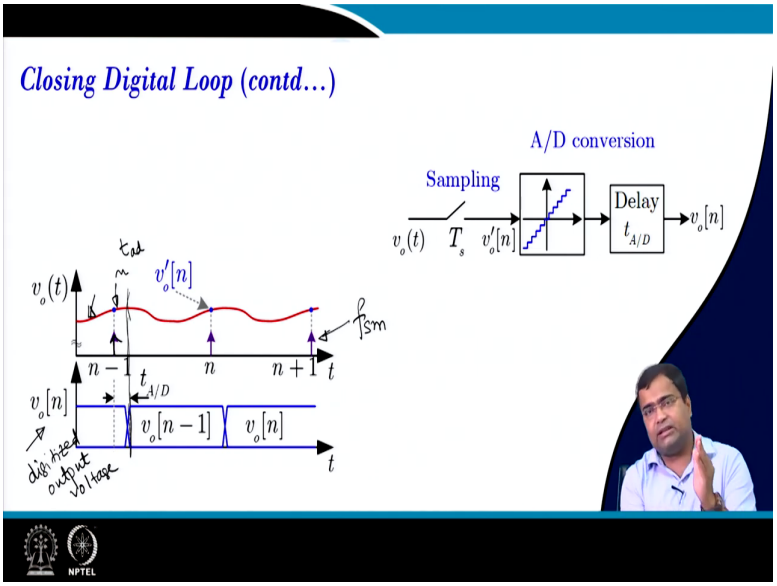

And this conversion time actually if we want to draw this timing diagram. That means, this is the digitized voltage; that means, this is the digitized voltage digitized output voltage. So that means, it will be a number, so if it is an 8-bit ADC then an 8-bit number, and so on.

So, this is the continuous time analog output voltage which is a time domain waveform, and suppose we have sent a signal because the ADC requires a clock. That means, at what clock

edge do you want to sample? Suppose you have sent this as a sampling command, this is let us say our sampling clock.

Suppose you have sent that I need a sample here, but because of the conversion time, this data will be available after a certain time. So, this duration; means, your data is available as if here and this is a comment, so this is your conversion time of the ADC ok.

But the conversion time that we are showing in this waveform looks very small, but this conversion time can be very large. Because if you are talking about low power application and let us say just a point of load converter and you are using an ADC. So, if you want to reduce this timing conversion time; that means, your ADC should support a high sampling rate.

That means, you need to have a very powerful ADC and that will consume a lot of power and also the cost will be very high. But suppose even if you use a high sampling rate ADC if you sample at a lower rate you can reduce the power consumption. So, if you sample at a lower rate naturally the conversion time will increase and this depends on the type of ADC.

Suppose you are talking with the pipeline ADC the pipeline ADC delay will depend on the number of pipeline stages and the clock at which you are sampling. So, all these will be discussed, when we will talk to A to D and D to A converters. But here we should remember this conversion time can be much larger than the switching cycle, if you use a low-power A to-D converter.

But with this such a large delay how to handle the switching converter performance and how to handle different types of stability that will also discuss in this course. But here I want to give a very basic introduction; that means, there is a delay and this delay will cause the availability of the actual data which is much later than when you send the actual sample signal.

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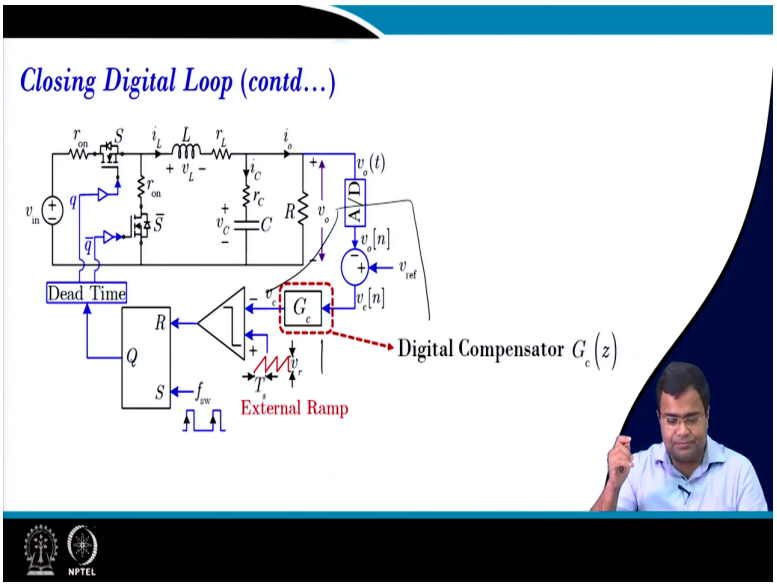

So, now, again the next part when you have a digital signal here, naturally this compensator has to be discrete time. That means, this compensator will be sitting on the digital control platform, which can be a microcontroller, ASIC, FPGA whatever.

So, in this course, we will be prototyping using FPGA, so this compensator will be sitting in the FPGA. And this FPGA means there will be resistors and some arithmetic and; that means, it is ALU operation arithmetic and logical operation and there will be some memory block. So, all this compensator computation will happen by this ALU block ok.

And we want to design some of these blocks, which means a different compensator using Verilog HDL in this course.

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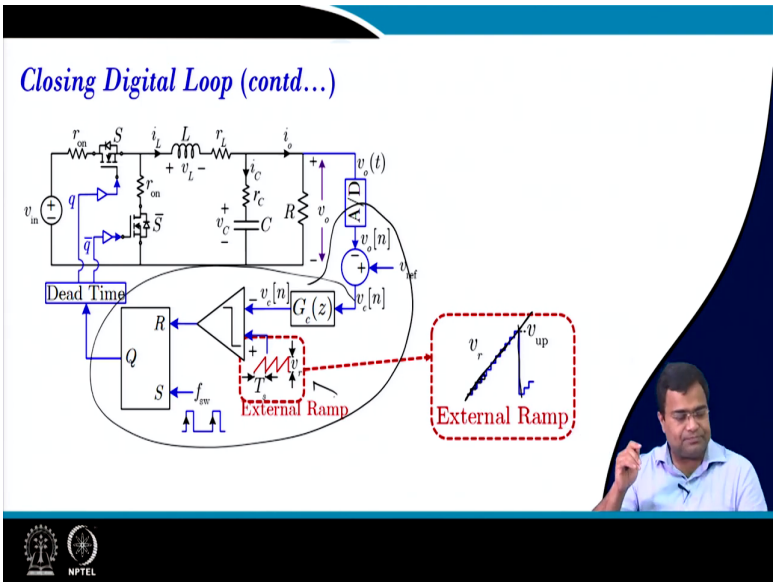

So, next to the ramp, since we are all talking about digital because so far all these signals are digital ok, so these are digital. So, naturally, this ramp should be digital and how do I generate this ram for this ramp? A very easiest way you should use a counter as if the counter is just kind of incrementing right. So, in the counter state keep on incrementing again you reset the counter.

But the question is if you compare an analog ram like a which is a smooth ok and it is just. So, this analog ramp has no resolution problem, but here you have a resolution problem. And if you want to reduce the step size to closely approximate an analog ram then the bit size of this counter.

That means, the counter bit should increase the counter bit at the same time, we should increment using a high-frequency clock. And that will also lead to a lot of power consumption and it may not be possible to achieve high resolution for high frequency, because the clock requirement can be impractically large we will discuss different architectures and how to handle it.

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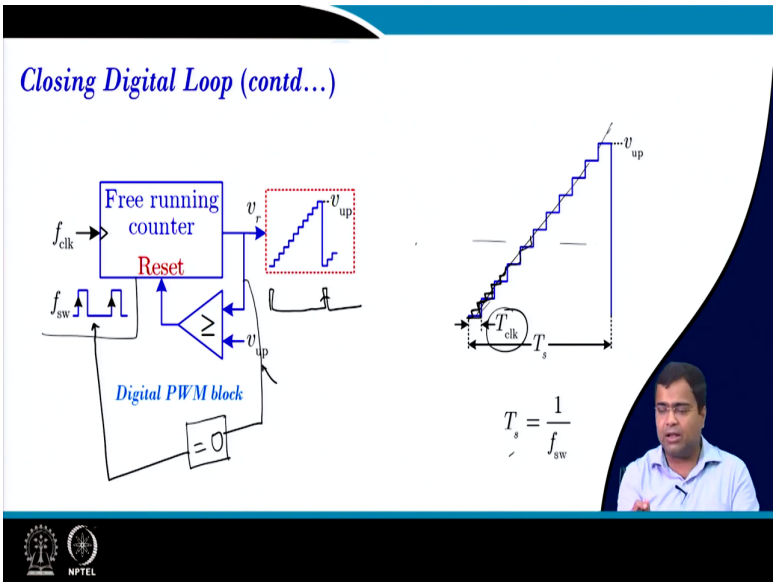

So, in summary, that means, if you use just a counter it can be a modulo counter, it can be a free-running counter. In the case of the free-running counter, you have to compare it with the upper limit and we can suitably adjust the switching frequency just by changing the upper limit if we keep the sampling clock the same.

Here we are resetting the counter by comparing it with the upper value and this reset pulse can be used that means when it is equal, we can use that as a switching clock. Because we need to synchronize with this switching clock right. So, this will be a switching clock. So, this synchronization can be done if we just compare with a 0 block; that means if you put an equality block 0 that will be like your switching frequency clock ok.

So, in this part, we will also discuss when you want to implement using the digital circuit and how to implement this you know this architecture DPWM. And this is you know maybe a zoom version of this counter base saw tooth waveform, where you can see the counter is simply incrementing. And the period of this clock which is a high-frequency digital clock is T clock ok and the switching frequency is 1 by f s.

So, if you want to decrease this; that means, if you want to improve this resolution then naturally the time period T clock duration should be reduced as a result you need a high-frequency clock that is a digital clock. And we will discuss that when you talk about this DPWM architecture there is various architecture to make it practically feasible for high-frequency application.

But the bottom line is this because of this quantization in the ram it may pose a limit on your duty ratio. Because if you compare this with your counter output unlike in a continuous waveform where you can perfectly intersect here there can be a mismatch between the actual comparison and that may lead to some you know duty ratio resolution problems. So, we have to be very careful about the selection of the resolution.

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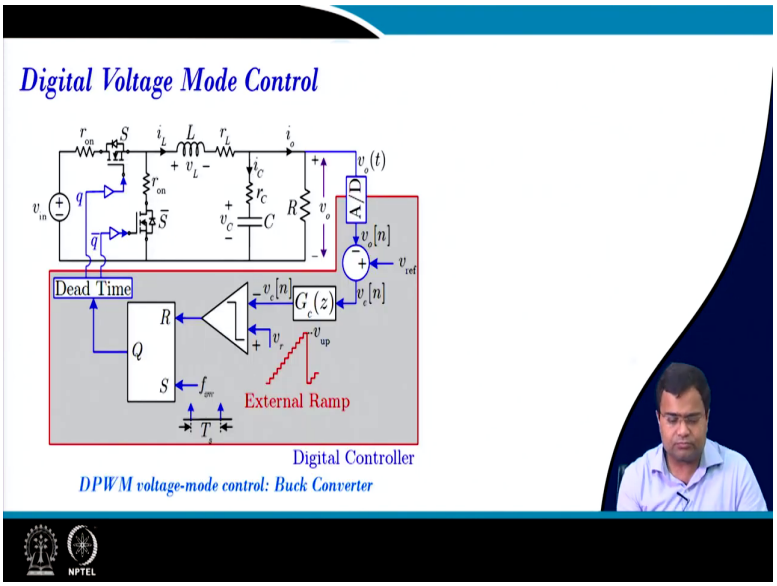

So, this is the overall architecture of the DPWM block, Digital Pulse Width Module is a voltage mode control.

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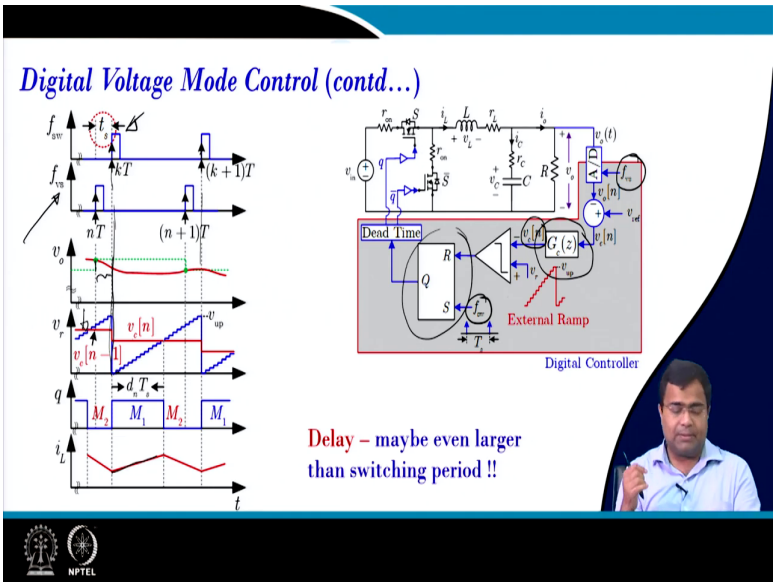

And if we show the waveform overall waveform. You know where it is the fsw clock which is a switching clock. And again we want to recall you know what we have discussed, I think lecture number 7, yes. Modulation technique this voltage mode control analog control is a trailing edge modulation.

And if you consider this almost equivalent to analog ram you see whenever the switching clock comes and this time the switch is turned on and the current is rising right and the saw tooth is rising. And this saw tooth reset again at the next rising of the switching clock.

So that means, this saw tooth waveform is synced with the switching clock and that matches. That means, when the rising has come saw the tooth start incrementing, when another rising has come saw the tooth reset and again start. And the current waveform and the converter turn-on are also synced with the clock because it is under trailing edge modulation.

But if you look at the switching frequency sampling clock which is this sampling clock f vs which is shown here. As I said there has to be a finite time that will accommodate the conversion time of the A to D converter as well as the controller computation. Because it will also take some time to compute because you are using a digital platform.

Because you want the sample to be here and this should data should be available here, this is the delay ok. So, that means once you send the sampling signal here then there will be ADC conversion time and the controller computation time, and your data will be ready here.

So, you can see the data which is a red line, and this data VC which is nothing but the output of the compensator. So, this data is getting updated with the switching frequency clock, but the sample is captured at your know sampling clock. So that means, there is a difference in the time delay and that is to accommodate the conversion type.

And then here we are talking about just one sample per cycle and that will be updated and then accordingly, the rest of this waveform looks similar to voltage mode control. In fact, in digital control, if you take one sample per cycle you do not need a separate latch, because since you are taking only one sample there it is insensitive to any noise because it is not updating.

So, we can eliminate this latch circuit because the latch is already taken care of because the DPWM itself has a delay ok, what latch used to be I mean there. So, DPWM takes the sample

and this is held for the rest of the interval. Here the delay can be even larger than the period and that will discuss when you go for high-frequency implementation.

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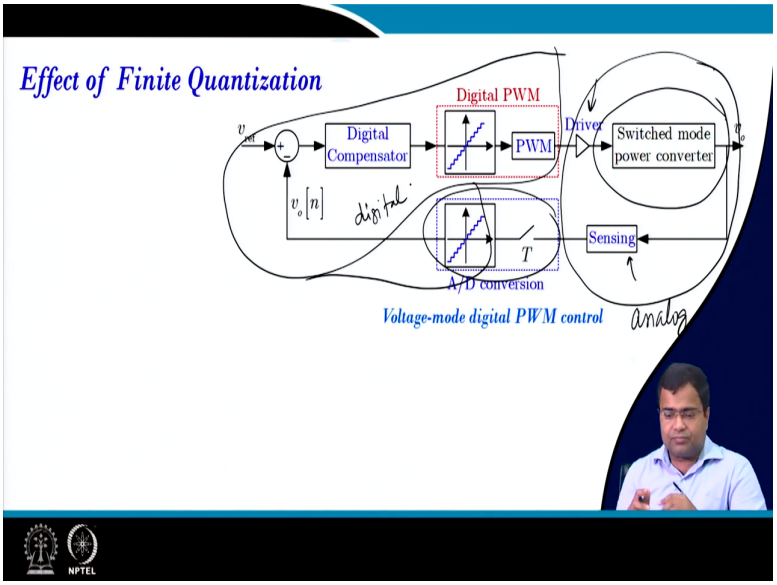

Now this finite effect of finite quantization, means if your quantization level is not. Because if you take the digital controller loop, this is our power converter. Here we will have a driver circuit and this is a sensing signal. So, all these blocks are analog because it is a real converconvertershen this is our A to D converter where it will be a sampling followed by quantization and these blocks are digital the whole blocks. We start from here, so this is the digital block ok. So; that means if we you know.

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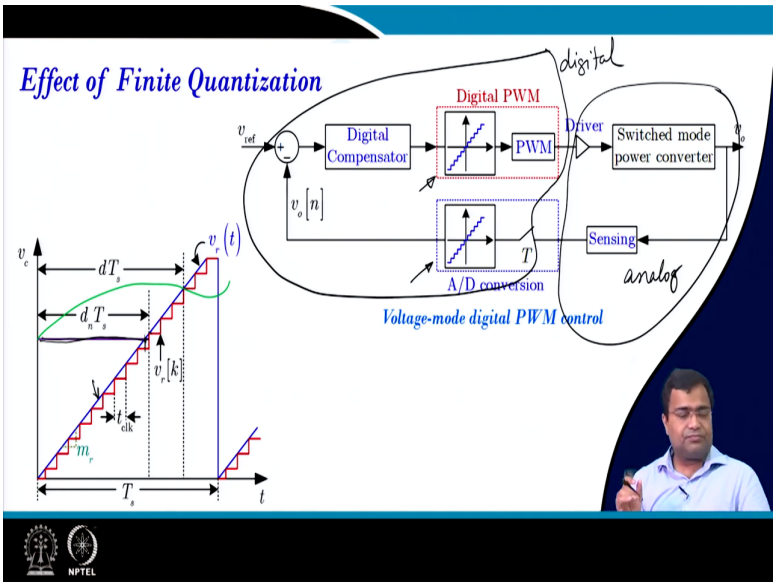

So, this block I would say, from here to here is our digital and these blocks are analog ok. So, here there are two places where you need to consider quantization. One is the ADC resolution where the quantization will come into the picture, another we are using a counter base or maybe other architecture of DPWM where it will be a staircase.

So, the resolution of this staircase is the clock frequency, all this thing that will also insert a quantization. So, these two quantizers are there and we will show you when you go to design, there is a specific requirement of the quantization selection otherwise it will end up with limit cycle oscillations. And this quantizer if you compare it with the continuous-time ram, means analog ram.

This quantizer actually, if you take the output control output or any signal. If it is analog then wherever it intersects that will be your duty ratio, but because of digital you have to wait for the next turn. So, this can insert a mismatch between their continuous time version and the digital version and that will create a duty ratio resolution ok.

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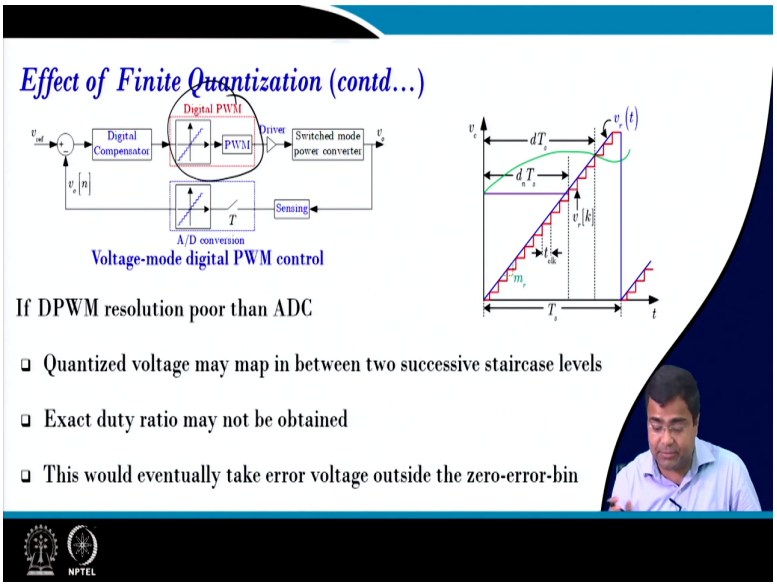

Next, if the deterioration resolution is poor DPWM; that means, the resolution of this block is poor than the DPW of the ADC and we will discuss it in detail. Then this quantized voltage level may not be inside the zero error bin. That means, then it may not be constant between two successive staircases and the exact duty ratio may not be achievable. And this may eventually go outside the zero-error-bin and it may lead to some kind of instability.

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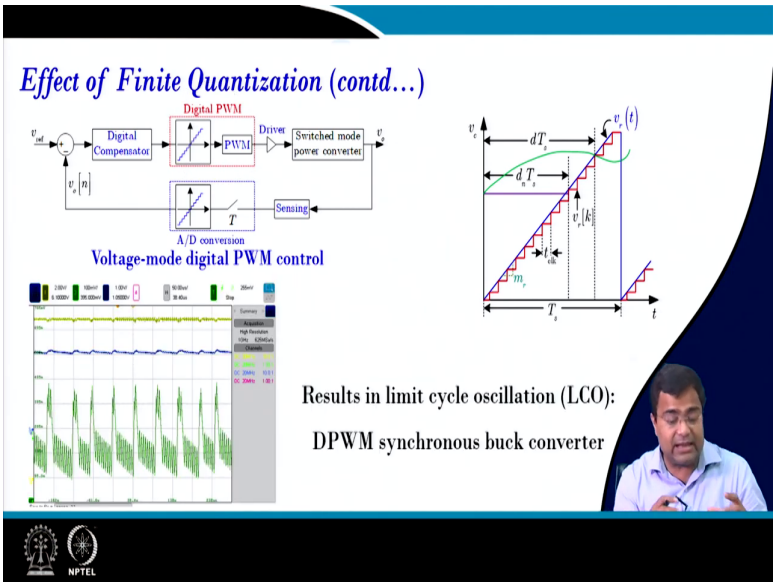

So, some sometime we may call it a limit cycle or it may be a high periodic behavior. So that means, this finite DPWM resolution can lend up or lead to a finite resolution problem or which may eventually go to either a limit cycle or high periodic behavior.

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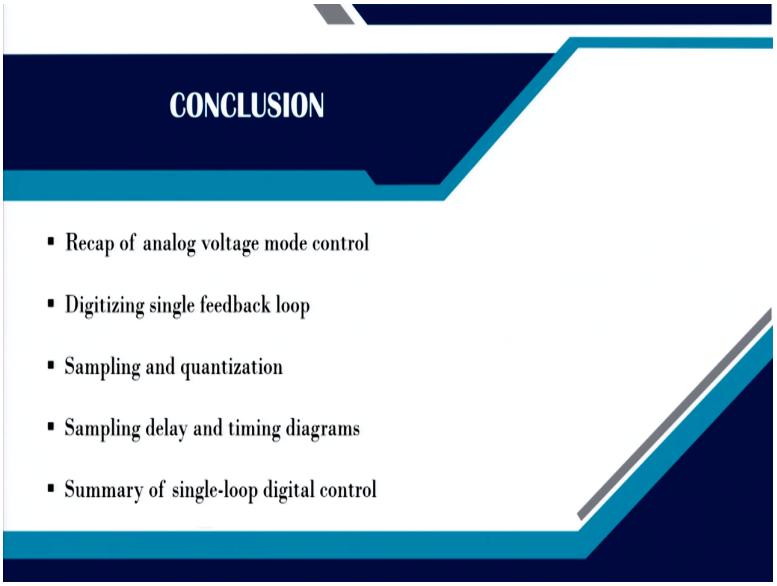

So, in summary, we have discussed that we have recapitulated analog voltage mode control. Then we discussed how to digitize the single feedback loop ok, then what are the like ADC, DAC, and sampling rate quantization; some basic ideas on how to digitize a single feedback loop.

Then we have considered sampling and quantization, but only basic we will discuss them in detail. Then we have also shown that there will be a sampling delay and we have also drawn some timing diagrams that will motivate that when you go to more practical design, the delay we have to consider, and with this delay, we have to extract how much performance can be achieved ok and what are the what will be the first scale stability.

And finally, we have summarized what is the basic step of digital control digital voltage mode single loop control ok. So, we want to stop here.

Thank you very much.