Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 08
Digital Controller Implementation using Fixed-Point Arithmetic and Verilog HDL
Lecture - 79
Voltage-based Digital Pulse Skip Modulation and Top-Down Design Method

Welcome. In this lecture, we are going to talk about Voltage based Digital Pulse Skip Modulation and Top Down Design Method.

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So, here we will talk about digital pulse skip modulation in discontinuous conduction mode. As we have discussed in lecture number 50, this pulse skips modulation technique comes into the picture when the converter operates in light load, particularly in discontinuous conduction mode; where we want to save or want to save losses switching losses and by that way, we are trying to improve the light load efficiency. And here, we will discuss top-down design methodology of digital pulse-skipping modulation

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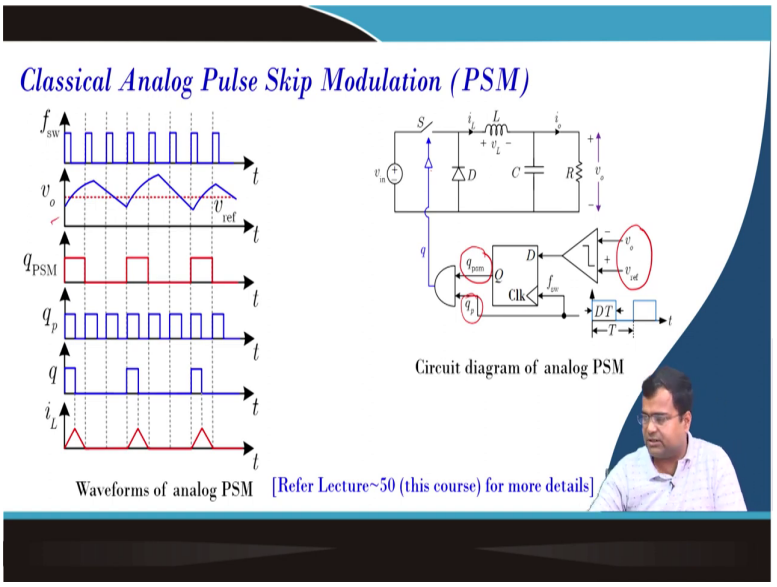

So, if we recall lecture number 50, we discussed classical analog pulse skips control where we have we are simply considering V 0 and V ref. And, this will be compared at the edge of the switching clock. And if V 0 is smaller than V ref, then we will this q PSM will be 1. And it will simply pass this PWM and the effective switching clock will be nothing but the PWM clock. And the waveform is shown here. So, this part we have discussed in lecture 50.

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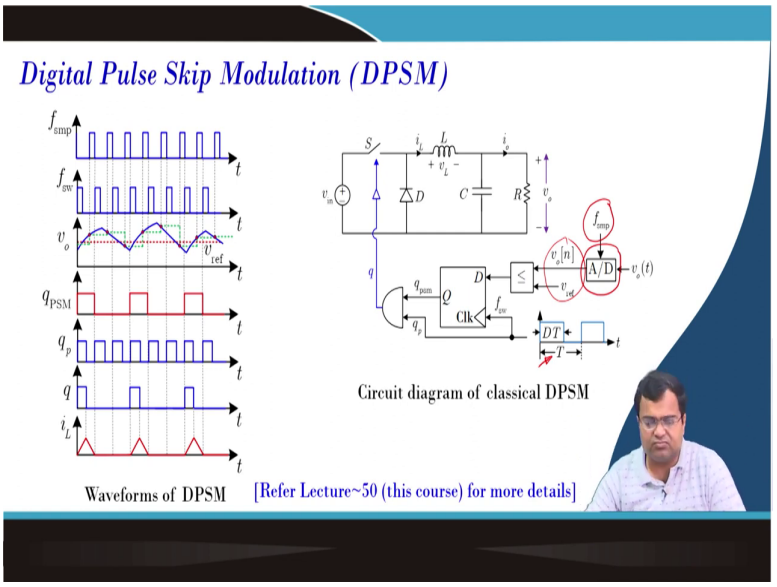

Now, if we consider the digital here we are only replacing digital. So, remember we may consider. Suppose, if you are talking about multi-mode control that we will discuss, we may

keep even this part we may or may not need any ADC as well or we may continue because if you are talking about multi-mode; that means, under high load or continuous conduction mode we will be using either digital current mode control or digital voltage mode control where the ADC is there.

Now, in this case, we can use this ADC because we have to keep track of you know voltage deviation and all. And that ADC information can be used for this pulse-skipping operation. And, here we are talking about very very rudimentary like a basic pulse skipping where we have a fixed duty ratio clock, and the only thing the q will either take the PWM clock or it will be 0 when it is skipped depending upon the status of this output voltage and the reference voltage.

And these are samples at every switching edge of the switching clock and which is nothing but the sampling clock we are taking the same as the switching clock. And this we have discussed in lecture 50.

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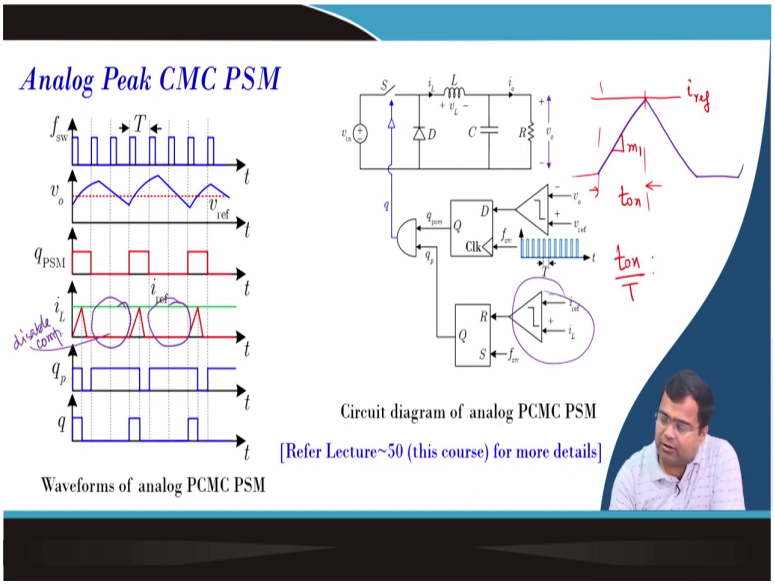

We can have also discussed what we can do because earlier we used a fixed duty ratio and we will discuss this in the subsequent lecture, the fixed duty ratio will have a problem for varying input voltage because if we keep the duty ratio the same. And if suddenly the input voltage increases; so, you may have a large current ripple and that may increase the voltage ripple also ok. Similarly, if the voltage input voltage drops we will discuss it may so happen there may not be any pulse skipping operation even under light load.

So, the selection of duty ratio is important, but in the digital circuit, you may update the duty ratio based on your you know switching frequency consideration right because if you find that your number of skip cycles is reduced and more number of charge cycles are going then we should understand that there is a time to increase the duty ratio. So, duty ratio adaptation may be possible.

An alternative way can do it is by a current base PSM. What was it work? Instead of giving a fixed duty ratio the duty ratio can be generated by comparing with the current, but all I c because you may or may not have this current mode implementation. Here we need to consider the analog current loop ok. So; that means, the duty ratio will be generated by comparing the current reference and the inductor current and that will give you the duty ratio during the PWM operation.

But it may so happen that you know the problem in this technique that if you operate under very light load conditions that this current comparator if you turn on and off you know because we have to disable it also.

During the skip cycle, we have to disable this operation otherwise if you continuously operate this comparator for every cycle even though you do not need a charge cycle then like in this case if you see that as if this operation is disabled, but it depends on unless if you disable this comparator otherwise every time this signal will be there actually I would say this waveform.

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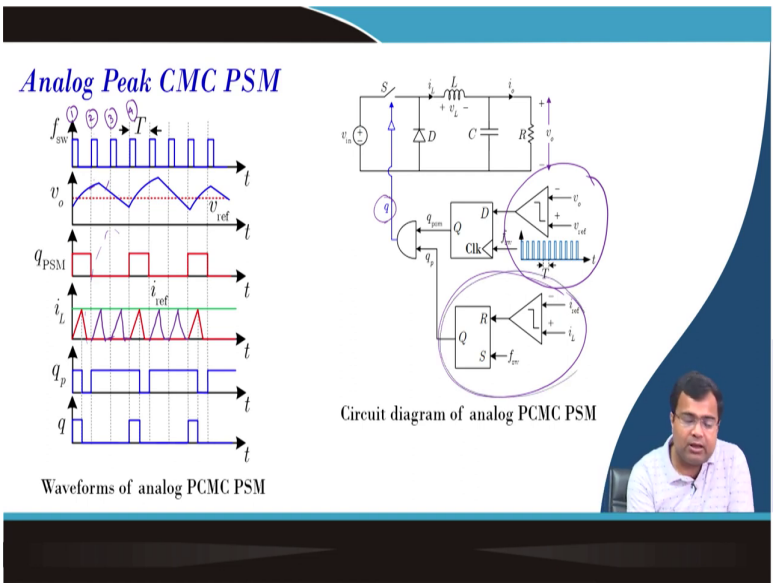

You will always find this waveform will be there. But you may not consider this waveform during the skip cycle, because we found these two cycles the output voltage is higher than the reference voltage. So, the basic logic of the skipping cycle of the selection of whether charge cycle. So, what do we call the charge cycle? When the PWM signal is a pass that is called a charge cycle when your actual duty ratio gate signal will be turned on and off, but when you skip; that means, there is no if the output voltage is above the reference voltage the cycle is skip that is called skip cycle.

So, you will see for these two cycles for let us say this edge is 1, this edge is 2, this edge is 3, and this edge is 4. So, for the second and third edges the output voltage is above the reference voltage which is why we need to skip the cycle during this time the q will not see the PWM signal it will be disabled, but since we are not using a separate disabling clock the current comparator will continue to operate.

So; that means, every cycle the current comparator will operate. So, this may be because your number of charge cycles is more. So, unnecessarily you burn power by this current comparator, and that too under very light load conditions. And that may increase your power loss. So, you have to be careful about the one way you can disable this block during this operation; that means, this operation you can disable; that means, I would say you can disable the comparator. This comparator can be disabled, by that way you can save power.

Again we have to enable the comparator when there is a charge cycle. And this enabling and disabling of the comparator may be faster compared to the switching frequency. So, we have to keep that thing in mind. Now, we go to we have discussed the basic feature of this analog current base, but the good thing about this technique since it is there is a current difference. So, you will not you will always protect the circuit that is one aspect of the protection point of view.

The second part is that you are always giving a current limit so; that means if your input voltage is high so; that means, let us consider this scenario. So, you have a current reference. So, now, if you see this on time t on and this is the slope of the current and this is i ref. So, what is your t on? t on by t is.

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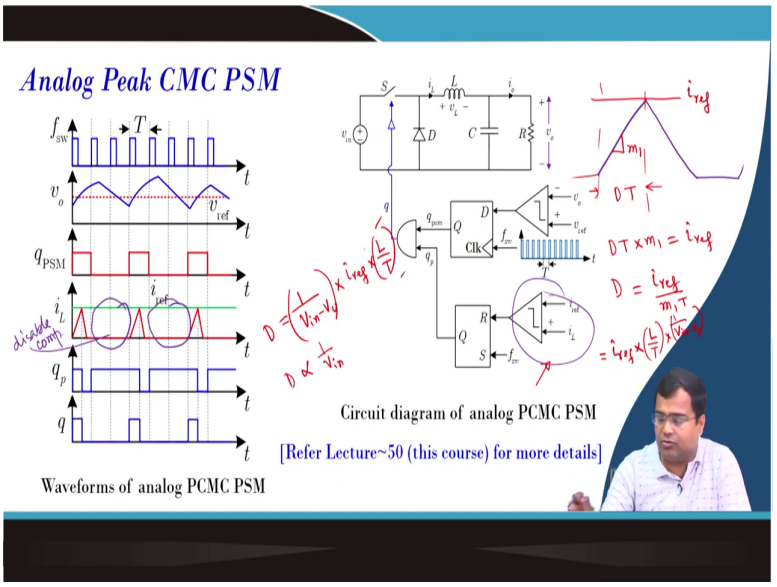

Or instead of t on you can say it is a duty ratio, you can say it is a duty ratio that will be much easier D into T, then your D into T into m 1 is equal to i ref. So, your D will be I ref divided by m 1 t. And what is m 1 for a buck converter it will be i ref into what is m 1 it is; that means, it will be L by T into 1 by V in minus V 0.

That means, whenever there is an increase in the input voltage then naturally since; that means, what is the expression of duty ratio will found? If it is one by V in minus V 0 into i ref into L by T; that means, if L is T, L T are fixed i ref is fixed. So, the duty ratio is inversely proportional to 1 by V; that means if V in increases duty ratio is decreasing if V in decreases, the duty ratio is increasing.

So, in that way we can make sure the pulse skipping is happening, and also we can ensure that the current limit is not crossed, but again we have to consider this practical part into consideration.

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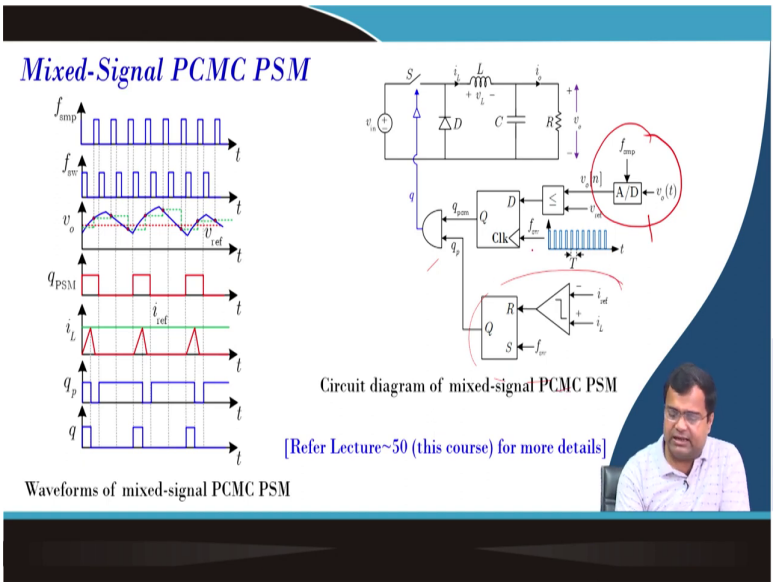

And we have discussed in lecture 50 the mixed signal where we can consider the voltage digital, because if it is a part of mixed-signal current mode control where in continuous conduction it is typically the peak current mode control. And the peak current reference will be coming from where? It will be coming from your outer loop of the p i controller. And there we may not be providing any pulse skipping because you know under high load we do not want pulse skipping.

And then we can disable this otherwise we can use this digital voltage loop and do continue to operate in peak current mode operation, but we have to make sure that we need to ensure enabling and disabling of this comparator otherwise we will be burning a lot of power during light load condition.

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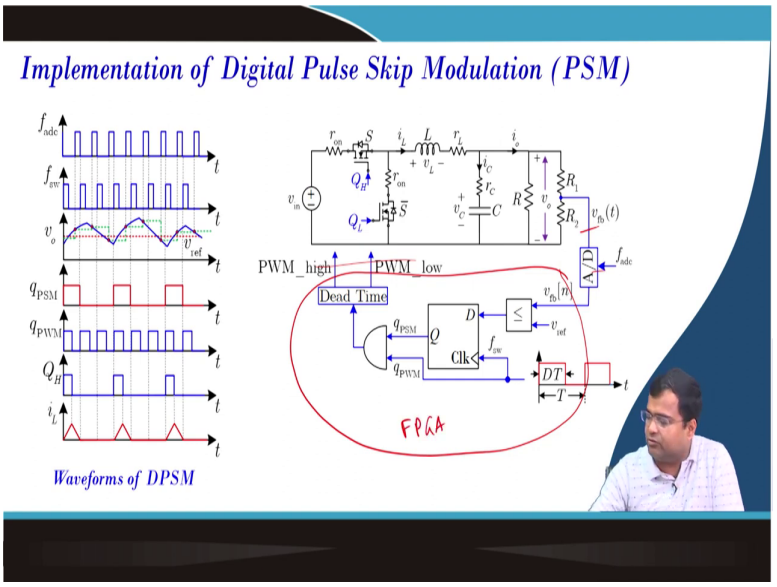

So, the implementation of this block, what do we have to implement? This is our practical circuit this is ADC, and I have to generate a gate signal. So, ADC data to this will be in your digital so; that means, it will be your part of the FPGA that we are going to implement.

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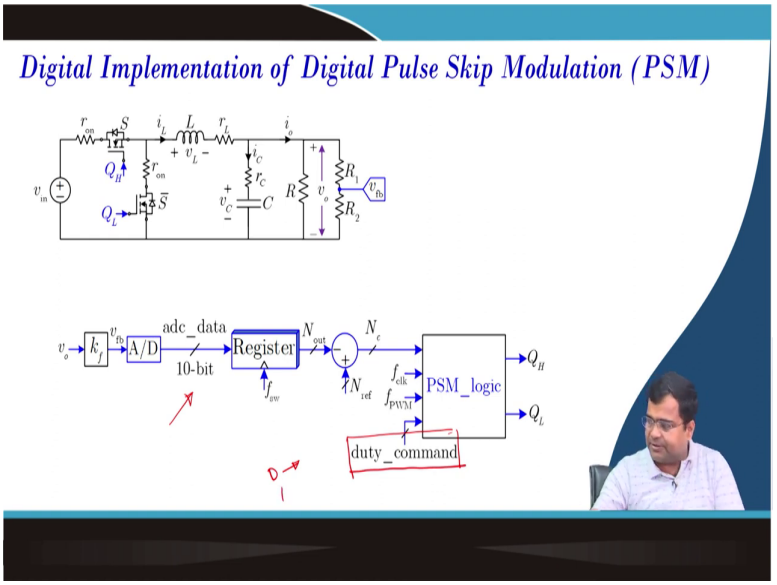

So, we are taking data from ADC, and that data we are calling ADC data. And we have discussed in the previous lecture digital voltage mode and digital current mode control. So, ADC data is coming and we are only talking about digital pulsing no current base it is just a fixed duty ratio base.

So, the duty ratio command we have to provide for the PSM block, but this command can be adaptive; that means, this command will give you the duty ratio which can be varied based on you know how many skip cycles. So, if there are too many skip cycles then you have to consider the current is high it can reduce if the input voltage increases, but if there are less number skip cycles you can always increase this duty ratio to anticipate.

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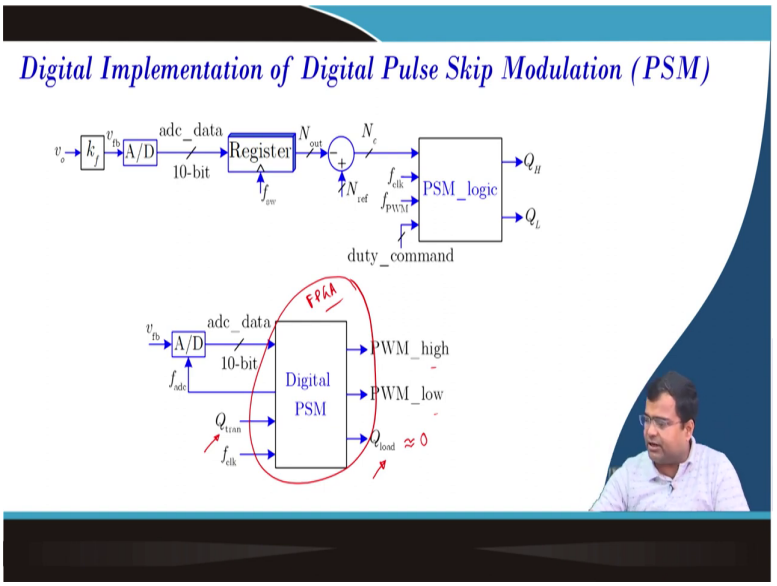

So, we need to effectively design this Verilog module and this will be our FPGA that will be sitting inside the FPGA digital which will generate the PWM high low, and we are not making any load transient. So, this can be set to 0; that means, it will always consider the high load resistance which means under light load conditions, but we can make a reference transient anything transient is possible. When you go to the multi-mode we can use this load and it will switch between PSM and PWM that case also will be considered in the subsequent lecture.

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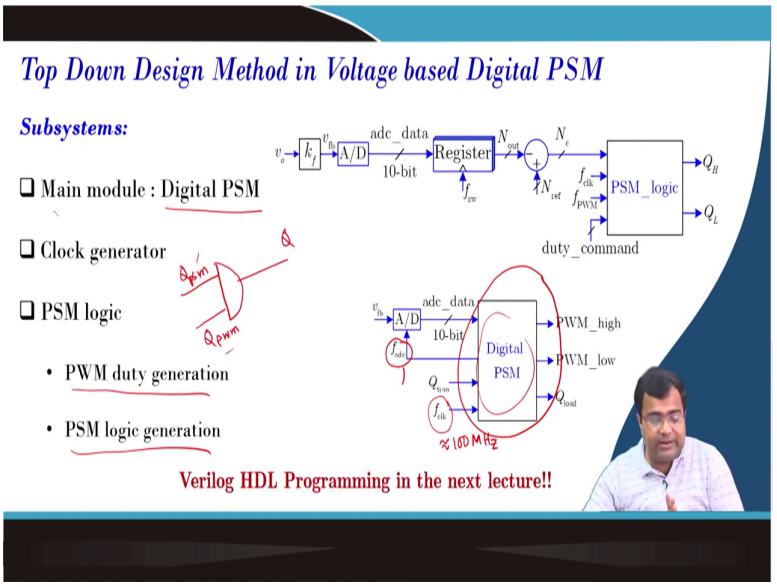

So, we have to make this module; that means this is my overall module and we have to do a top-down. So, the main module will be digital pulse skipping. And this module requires a clock generator to generate the clock for the ADC, and this will take the input clock as the f clock which former case is a 100 megahertz clock. The ADC clock is up to you for light load operation you can reduce the ADC clock, but we have an unconsidered high load of around 25 megahertz clock for the ADC.

Because to reduce the effect of sampling delay otherwise your pipeline ADC has 6 cycle delay. If you use a slower rate for the ADC sampling the effective delay will increase and that will cause stability issues. And we will be discussing the sampling delay aspect in the subsequent lecture. We also need a PSM logic which will be inside this block and finally, this PSM logic will consist of a PWM generator and a PSM logic because we have discussed the actual gate signal will be an and of you can say PSM and Q PWM.

So, when the PSM is low 0, then Q will be simply 0. And it is called the skip cycle when this is high it will take the PWM clock. So, we will be discussing the Verilog program in the next lecture.

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So, in summary, we have discussed digital pulse skipping modulation in discontinuous conduction mode, then we have discussed the top-down design methodology of digital pulse skipping modulation. And in the next lecture we are going to show the Verilog coding which is simple, we already know the other Verilog codes. And then we will also show some experimental case studies. That is it for today.

Thank you very much.