Digital Control in Switched Mode Power Converters and FPGA-based Prototyping Prof. Santanu Kapat Department of Electrical Engineering Indian Institute of Technology, Kharagpur

Module - 08 Digital Controller Implementation using Fixed-Point Arithmetic and Verilog HDL Lecture - 78 Hardware Implementation of Mixed-Signal CMC and Experimental Results

Welcome back in this lecture we are going to talk about, we are going to discuss the Hardware Implementation of Mixed-Signal Current Mode Control with some Experimental Results.

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CO	NCEPTS COVERED
 Digital Curr 	ent Mode Control Implementation details
 Mixed-Signa 	l Peak CMC – Experimental with transient performance

So, here we will show you know we have discussed in the previous lectures, I mean 2 or 3 lectures, where we have discussed mixed-signal current mode control implementation and programming using Verilog HDL. So, now we will show implementation details, whatever we have used in our experimental setup and some experimental results with transient performance.

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Mixed-Signal Peak CMC Architectu	re Power Stage L	etails Quad
	Inductance L	1.8µH
$v_{u} \stackrel{q_{u}}{\longrightarrow} q_{u} \stackrel{q_{u}}{\longrightarrow} q_{u}$	Capacitance C	200 µF ◀
	Input Voltage V _{in}	3.3V 4
pwm_high pwm_low	Output Voltage V _{ref}	€ [1,1.1]
$R = \begin{bmatrix} r & p \\ p$	Switching Frequency f_{sw}	200kHz 🔹
	Load resistance (R_c, R_{sw})	(13.5Ω, 0.33Ω)
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So, mixed-signal peak current mode control architecture, we have discussed multiple times, and for this converter prototype that we are going to demonstrate we have considered the inductor to be 1.8 microhenry capacitor to be 200 microfarad. And, we have considered a nominal input voltage of 3.3 volt, and the output voltage is varied between 1 to 1.1 because we have shown also reference transient. So, the nominal output voltage is 1 volt, and, the switching frequency of considered 200 kilohertz.

And we have considered one continuous load resistance R C and a switch resistance point 3.3 ohm because, if we consider the buck converter output size state, you know. So, we have to consider one continuous resistance, and another switch resistance this is our switch resistance where we have considered Q load. And, we make it either load 0 or 1; 0 means it will operate at a lower load condition. And, 1 means it will operate in higher load conditions because effective resistance going down.



So, in the control architecture apart from the power stage we have considered we have shown this diagram; that means, the actual implementation in the previous 2 lectures, where, we have considered that we have a feedback gain, voltage feedback gain which is decided by the resistive divider. And, this gain is nothing but 0.27, ok. And, then, we are we have considered a 10-bit ADC which is why the ADC resolution is 10-bit.

We have considered a DAC which is a 12-bit DAC, as we have discussed, the 12 bit DAC and we are using a controller clock which is a controller that clocks to 100 megahertz, and the current sense gain because we have used the current sense resistance followed by the current sense amplifier.

So, it is coming to be 0.1 Volt per ampere because it is converting current into a sense voltage. And, that is compared directly with the output of the DAC. And the DAC V P can vary between minus 1 Volt to; I mean I would say minus 1 to. So, it should be in the closed bracket which is the lower limit to 1 Volt, ok. So, that is the detail and we have considered this PI controller where the proportional gain is 4.75 and the integral gain is 0.4, ok. And we have discussed the current reference dead time in all this detail in the previous lecture.

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So, for the digital controller, and PI controller gain that we have discussed in the actual code we have taken 4.6 and 1 point, sorry, it is in the 4.6 Q format and Q 1.9. And the proportional gain we have discussed, is how much it is? 4.75 and 0.4. 4.75 and this appears to be 0.4.

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So, these are the gain now we are showing load step-up transient. So, we have applied; that means, we have considered the output capacitor size, the site we have a continuous load which is 13.5 ohm and then we have R SW and this R SW is 0.33 ohm. And, we are considering one external load that is, sorry, low MOSFET to turn on and off. So, this is the

condition at this is 1 volt and this is under lower load condition; that means, here your load resistance. So, effective load resistance either can be a simple R C under light load condition or under high load condition it is a parallel combination of R C and R SW.

 Load Step-up Transient

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So, we are making a load transient and if you look at the load transient response, the undershoot which is here this undershoot is coming to be roughly around 175 millivolt to like roughly 16, 170 to 180 millivolt and we are getting a load, I mean reference, sorry, settling time of around 80 microsecond.

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And if you go to load step-up transient step-down. So, we are getting again the delta v the overshoot is roughly around 170 millivolt and the settling time is coming to be here. So, like 60 microsecond. But again, we will discuss the design aspect by which we can shape the transient response and this seems to be quite good, quite fast, because you see the current is ramping down fast.

So, this overshoot is something that we have to accept because the load has gone down. So, you will have an excess capacitor charge that has to discharge by the inductor.

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So, reference transient also we have considered where we have, set the load resistance to be at R C that is to be 13.5 ohm that is the load resistance, fixed load resistance. So, in this case, it is a 1-volt reference and here it is 1.1 volt. So, we will have some additional overshoot in the output voltage.

So, this additional overshoot which is coming delta v that is equal to; so, on top of this 1.1. So, we are getting around 50 millivolt overshoot. For 100 millivolt is the load reference step transient. Similarly, we are getting undershot here also. So, which is delta v this is also around 50 millivolt. (Refer Slide Time: 07:08)



And, if we go to this is the more detailed response. The settling time is coming to be this much; that means, around 50 to 60 microsecond, we can take up to this point. So, if we consider up to this point, sorry. So, this point is 50 microsecond and over the shoot is around 50 millivolt.

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And, if you consider the undershoot; it is also around 50 milli volt. But, in this case, this is coming to be roughly around 40 microsecond, ok so; that means, we can load transient and reference transient response we have discussed in current mode control.

And in the subsequent lecture, we will discuss the design aspect.

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So, in summary, we have discussed digital current mode control implementation using a mixed-signal domain, where the current inductor current is analog, implementation analog loop and with analog current loop and digital voltage loop. And, we have also discussed mixed-signal peak current mode control, experimental results with some transient performance.

So, in the next lecture, we are now going to consider, what will happen in discontinuous conduction mode and we will be discussing pulse skipping modulation. That is it for today.

Thank you very much.