Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
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Module - 08
Digital Controller Implementation using Fixed-Point Arithmetic and Verilog HDL
Lecture - 75
Top-Down Design Methodology in Mixed-Signal Current Mode Control

Welcome, we are going to talk about, Top Down Design Methodology in Mixed Signal Current Mode Control.

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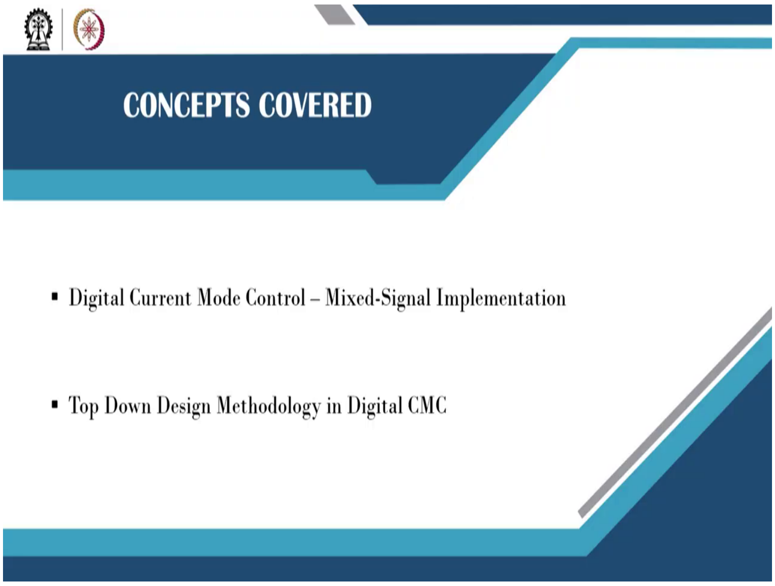

CONCEPTS COVERED

- Digital Current Mode Control – Mixed-Signal Implementation
- Top Down Design Methodology in Digital CMC

So, in this lecture, we will first talk about digital current mode control and its mixed-signal implementation; and what is the top-down design methodology, in digital current mode control.

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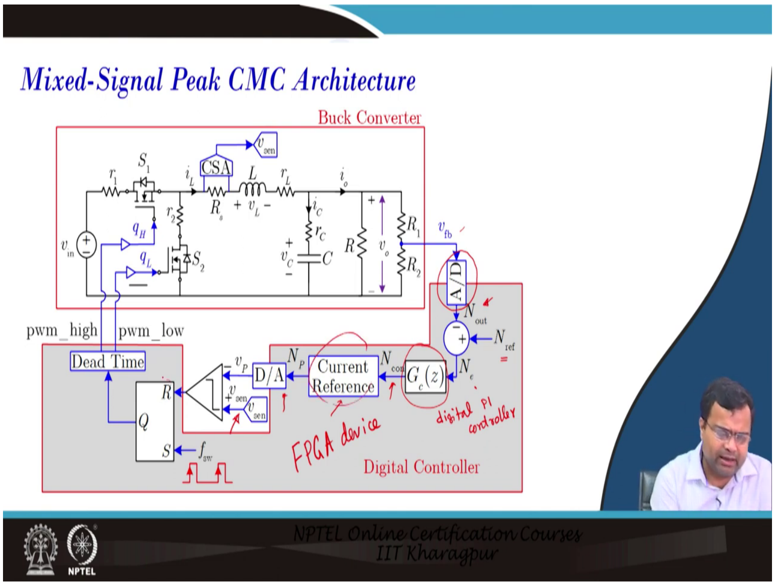

Mixed-Signal Peak CMC Architecture

So, we have discussed the mixed signal current mode control architecture, this is one of the architectures of digital current mode control, and this, we have discussed in sufficient detail in week 2, as well as week 3 in the MATLAB simulation. So, in this architecture, we have the current loop in analog and that is the sense, voltage inductor current; that is, we call as a V sense and then, we also have, the feedback voltage loop which is in digital.

And, we need A to D converter for voltage sampling and you are sampling the feedback voltage, where there is a resistive divider. And then, this is coming inside the controller, because before we go into detail about the FPGA. So, here, we will be using an FPGA device for implementing this digital control.

And the FPGA device will take the digital data from ADC, and this N out is the digital number, corresponding to the output voltage, feedback voltage; that means, the analog signal. Then we have a reference command, then error voltage, then it goes to the compensator and we are talking about a digital PID, PI controller; for current mode control, digital PI controller; then the controller output again is a number, then there is a current reference generation, which ensures that we should first of all whatever the controller output, the data format has to be consistent with the DAC input data format.

So, that means, that for the compatibility issue, and compatibility purposes, we are using this block, and also, we are putting a peak current limit. So, all this block, will be taken care of by this current reference block. Then again we have, APWM and the dead time block ok.

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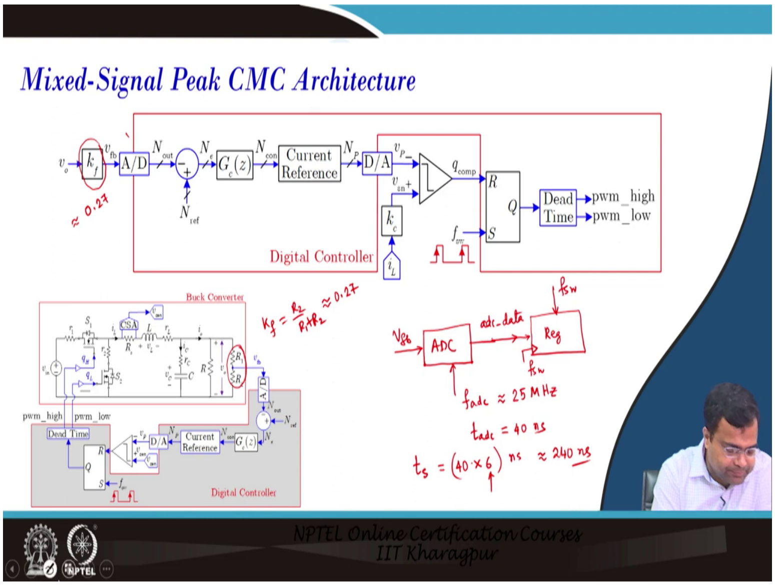

Mixed-Signal Peak CMC Architecture

$K_f = \frac{R_2}{R_1+R_2} \approx 0.27$

$f_{adc} \approx 25$ MHz

$t_{adc} = 40$ ns

$t_s = (40 \times 6)$ ns ≈ 240 ns

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So, if we take the realistic implementation of the mixed signal current mode control, this is a feedback gain; and we have discussed, in the previous lecture, when we are talking about digital voltage mode control, because there is a resistive divider, and this is coming as a feedback gain. So, feedback gain here, is R 2 by R 1 plus R 2, for this resistive divider; and it is approximately coming to be 0.27 for this case. So, this is 0.27 approximately; our calculated value.

Now, this data which is coming inside the controller, we are calling an ADC data that we have discussed; that means, we have, let us say, the feedback voltage which is voltage feedback, we have ADC and, this ADC, we are getting adc data, and this ADC, is sampled using a clock.

And this ADC clock we are using, 25 megahertz clock, and we have, we have discussed in detail in the digital voltage mode control, that when you are sending 25 megahertz clock; that means, the t adc will be 40 nanoseconds, 40 nanosecond; that means, and it takes about; so, what is the sampling delay? The sampling delay here, is the 40 nanosecond, into 6 units that we have said, we have shown right, a nanosecond.

So, it is roughly around 240 nanosecond, this is simply because of sampling because, this is a pipeline ADC, where there is a 6-cycle delay, 6-cycle delay and we are using a high-frequency clock so that, we can reduce the overall conversion time. So, in pipeline ADC, we see the conversion can depend on the number of cycles; and, when it comes inside the digital platform, we are using a clock which is our switching frequency clock, this is a register. So, this clock is like you know, this is our switching frequency clock.

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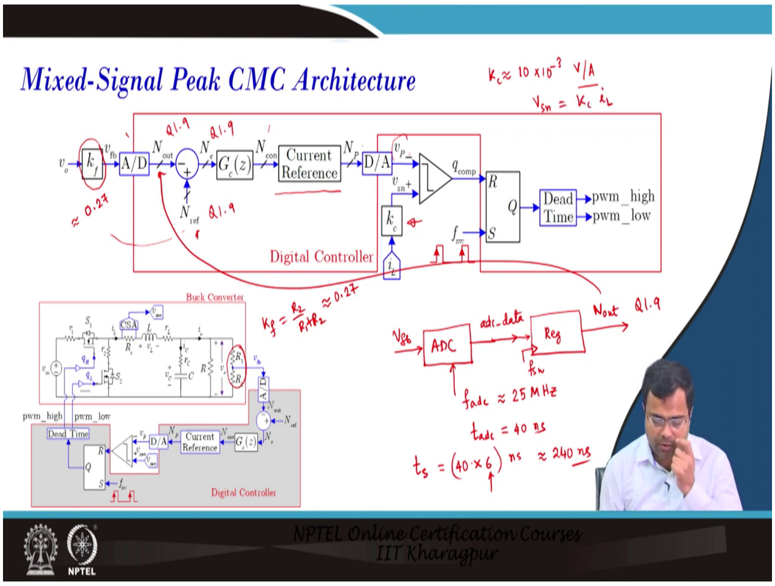

Mixed-Signal Peak CMC Architecture

$K_c \approx 10 \times 10^{-3}$ V/A

$V_{sn} = K_c i_L$

$K_f = \frac{R_2}{R_1+R_2} \approx 0.27$

$f_{adc} \approx 25$ MHz

$t_{adc} = 40$ ns

$t_s = (40 \times 6)$ ns ≈ 240 ns

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So, this register is updated and this data we are getting N out. So, this is, is here. And here, we are talking about N 1 dot Q 1 dot 9 ok, it is a sin number, 1 dot 9 format ok. Now, after that, the reference signal has to be and has been scaled according to this and we are talking about again Q 1 dot 9; this is Q 1 dot 9, this is also Q 1 dot 9 ok.

Now, this controller, when you go inside the digital controller, we have a separate lecture for that, we will discuss what is the format sizing. What is the requirement? So, we are using, so, we will talk about this bit size in detail. So, let us first understand the overall thing. So, this is a digital part, then the current reference is in digital, then we are giving digital data to the DAC and DAC is generating the analog voltage and that is directly compared.

Now, there is a current sensor, because you are using current sensor registers, followed by a current sensor amplifier; and this k c is coming to be around 10 into 10 to the power milli; since it is converting current to voltage, so, it will be volt per ampere, right. Because, the output is ultimately a voltage; kc. Because v sn is what v sn is k c into i l ok.

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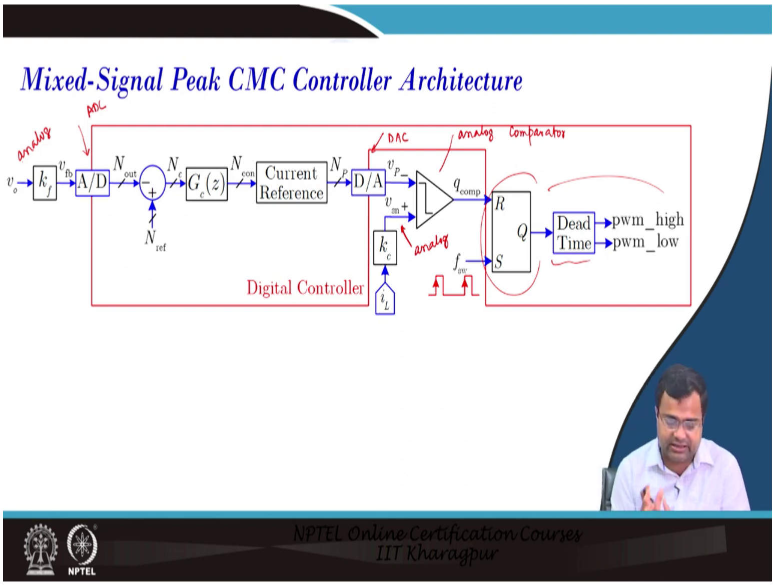

Mixed-Signal Peak CMC Controller Architecture

Next, this current mode. So, we understood that this part is analog volt, analog voltage. Again, this voltage is in analog. So, this is digital. So, naturally, for this interface, we need an ADC, for this block, we need a DAC ok. So, after this, there is an analog comparator. So, this is our analog comparator, comparator; the output of the comparator goes to a latch circuit. So, this again is the digital block and the dead time factor. So, we have discussed the dead time circuit in lecture number 70.

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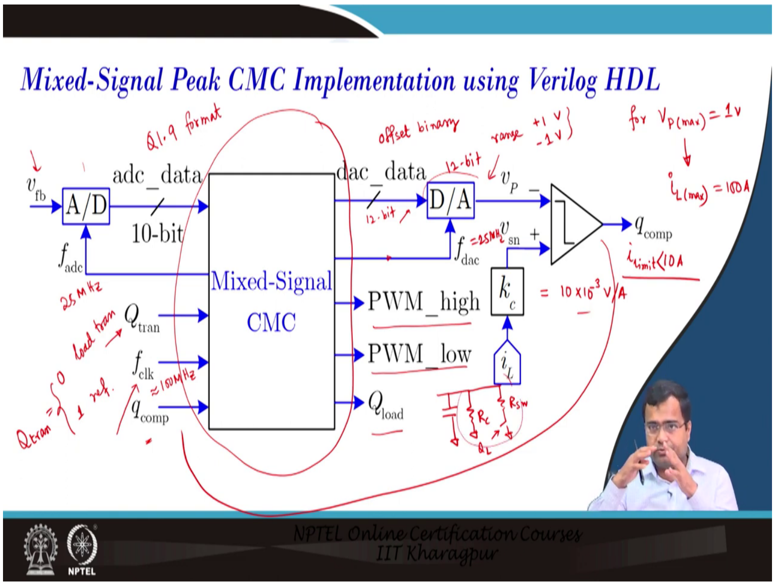

Mixed-Signal Peak CMC Implementation using Verilog HDL

So, this is the block, that we are going to discuss. So, in the FPGA, we want to implement this block, that we have discussed. What is this? So, we have discussed that we have a feedback voltage and there is an ADC, ADC requires a clock and this is we are sending like 25 megahertz clock, 10-bit data it is Q 1 dot 9 format ok, Q tran is the type of transient; whether you want to use load transient or the reference transient, that we have discussed.

If Q tran is; that means, what we are considering, if Q tran is 0, then we are talking about load tran. If it is 1, then we are talking about reference transient. f clock is a switching frequency clock and this is a 100 megahertz clock; the Q comparator is the output of the analog comparator. So, it is also coming inside; because it is a digital number, it is on the off path. Then. The output of this mixed signal is because we have a DAC. So, DAC data; is coming to be an offset binary, offset binary.

And it is 12-bit data and the DAC voltage, the span of this, span I would say, the output range. Instead of span, I would say range. So, the range, analog range that we are considering with the driver, including the driver; because, there will be a DAC plus, there is a driver also there, DAC driver. So, it is coming from plus 1, minus 1 volt to plus 1 volt. So, this is the range, that we have and, this gain is what? It is like a 10 into 10 to the power minus 3 volt per ampere.

So that means if we set a maximum of one volt, which corresponds to; that means, for v p max; to be 1 volt, this implies, if you set, the actual current limit max, max will be 100 ampere; because, this is there. And this is not acceptable; so, that means, we need to set, this value accordingly, which we want to limit to 10 ampere, or less than that. So, we want the current limit, to be less than 10 ampere; that is our requirement.

So, we need to accordingly, defined in terms of the current difference; then another output is the DAC clock, which is coming out of the controller, FPGA and again it is 25 megahertz clock; and DAC data is a 12-bit data, we have discussed, this is 10-bit data. Then, we have PWM high signal, PWM low signal, and this goes to the load; what is the load? If you take the buck converter, this capacitor. So, we have a continuous load, I will say r continuous, and there is a switching load; this is like R s w load and this is our Q L.

So, if Q L is 0, the switch is off; if the Q L is on, the switch is on and the switch is on these two resistance come in parallel. So, the effective resistance will be smaller. So, it will make a load step of the transient.

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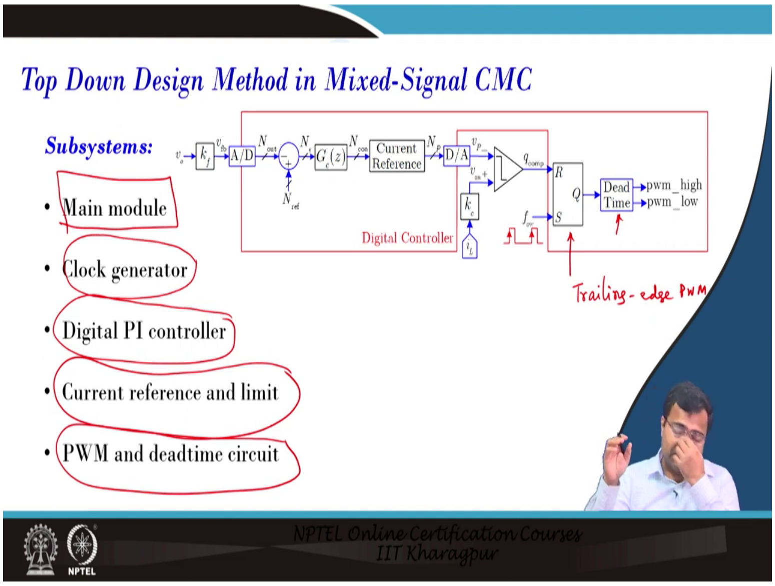

Top Down Design Method in Mixed-Signal CMC

Subsystems:

- Main module
- Clock generator
- Digital PI controller
- Current reference and limit
- PWM and deadtime circuit

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So, in this particular design, we need, we have multiple modules. The one module is the main module. So, this is the main module, which will mix the digital current mode control; inside the module, we will have a sub-module clock generator, digital PI controller, current reference, and the current limit that blocks PWM and the dead time.

Because, you are talking about fixed frequency control and here, we are talking about trailing edge modulation; we have discussed, trailing edge PWM ok and there is a dead time circuit. So, we are around 15 nanoseconds or 16 nanoseconds, we are setting the dead time.

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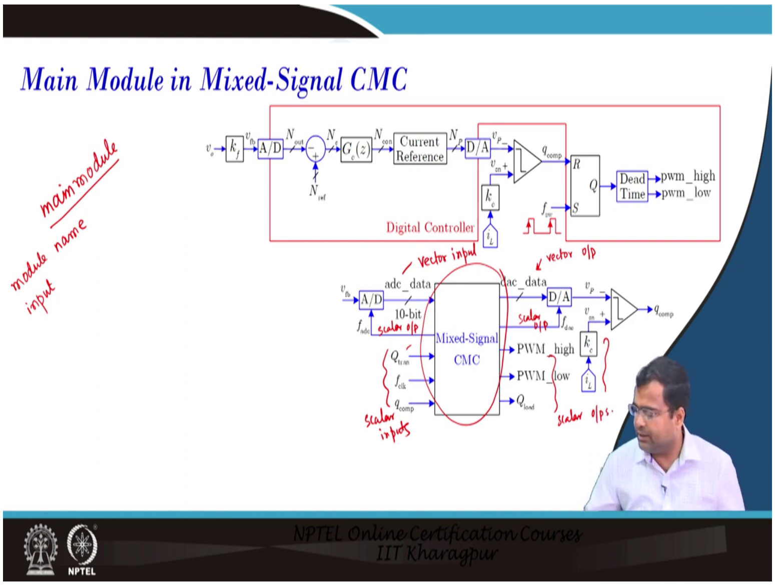

Main Module in Mixed-Signal CMC

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Now, the main module, if we go the main module will; that means, it is consisting of this is the main module. So, the main module name may be mixed-signal underscore current mode control, what is the input to the main module? Main module, if I say the main module, because we will discuss the Verilog code next, but before going that in this lecture, main module; what are the inputs to this? We need to give. So, we need to provide the module name, and module name, which will discuss, then we have input data.

So, what is the input ADC data is input, Q trans? So, this is a vector input; then these are all scalar inputs ok. Then, this is the vector output, this is a scalar output, this is also scalar output and these are all sorry, these are all scalar output ok. So, you need to create the main module.

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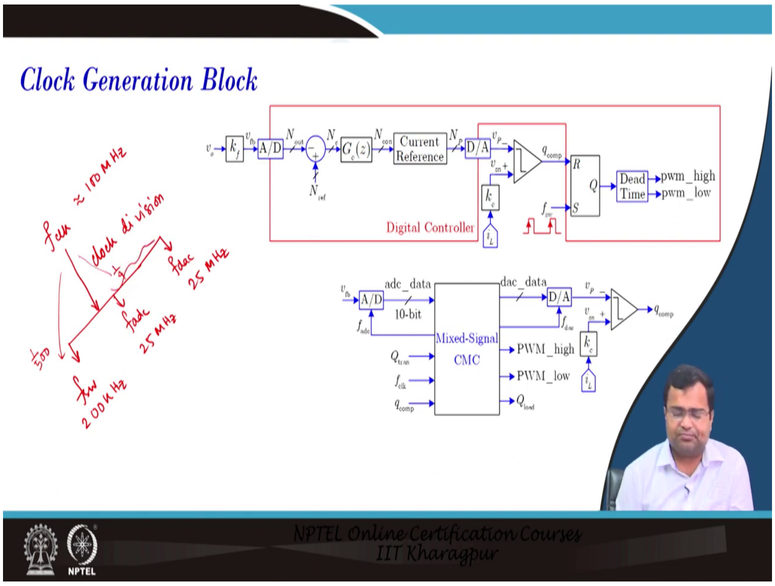

Clock Generation Block

Now, regarding the clock generation block, we will discuss this. So, what does it do? It takes the highest frequency clock. So, its job is to take the high high-frequency, then clock division; and it is going to generate, one for switching frequency clock. So, this is like a 100 megahertz clock and here, we need you to know 2 to 00 kilohertz, then we are using f ADC; which we are taking here 25 megahertz and there is one more f DAC; this is also 25 megahertz; that means, what is the division ratio we need?

This will be, 1 is to 500 division. This will be 1 to 4 for both cases ok. So, clock division.

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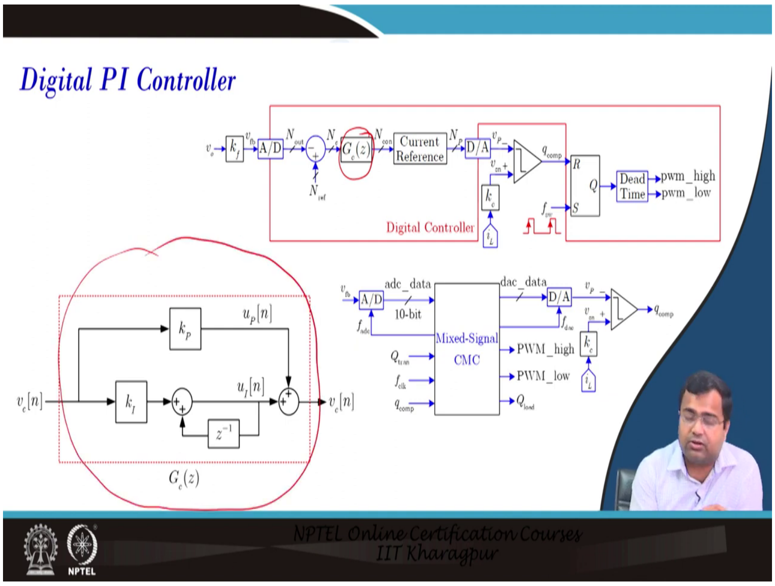

Digital PI Controller

Then, we need a digital PI controller. So, here we are using a digital PI controller and we have discussed this structure earlier; what does the digital PI controller look like?

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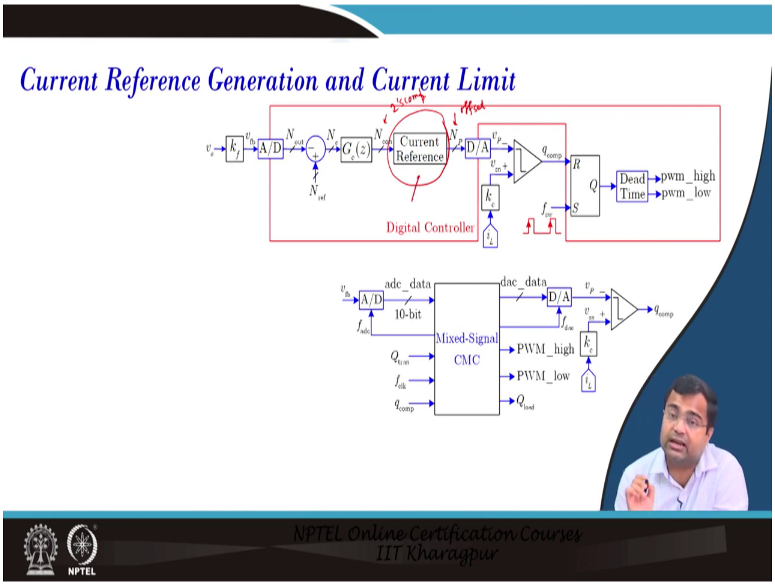

Current Reference Generation and Current Limit

Then, we also need a current reference generator. What is the job of this? The format of N P and the format of N con is different; first of all, there will be the size. So, we need to resize it, we know about the Q format; this data is offset binary, and this data is a 2 s complement. So, that means, we need a codifier that will convert one code to another code; including the resizing of the data ok. And, here we can also set the current limit ok.

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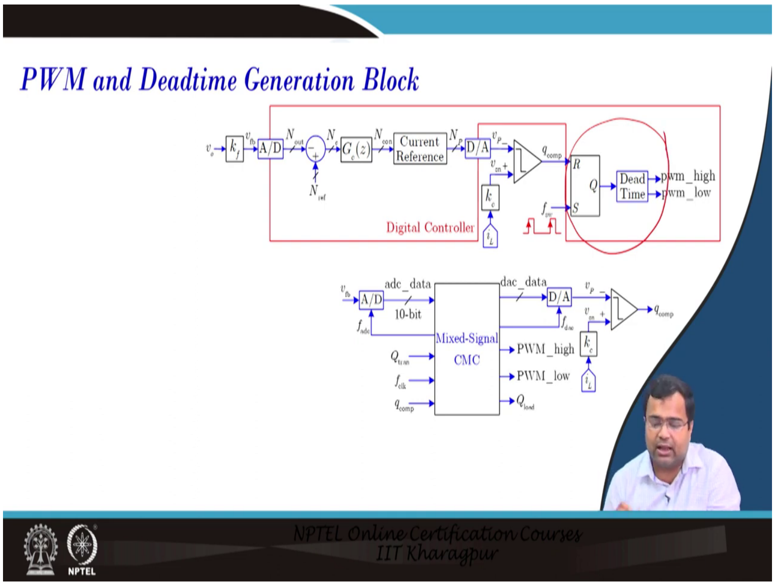

PWM and Deadtime Generation Block

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Next, the PWM and dead circuit. So, this part will be PWM trailing edge modulator, with dead time and we will be discussing this.

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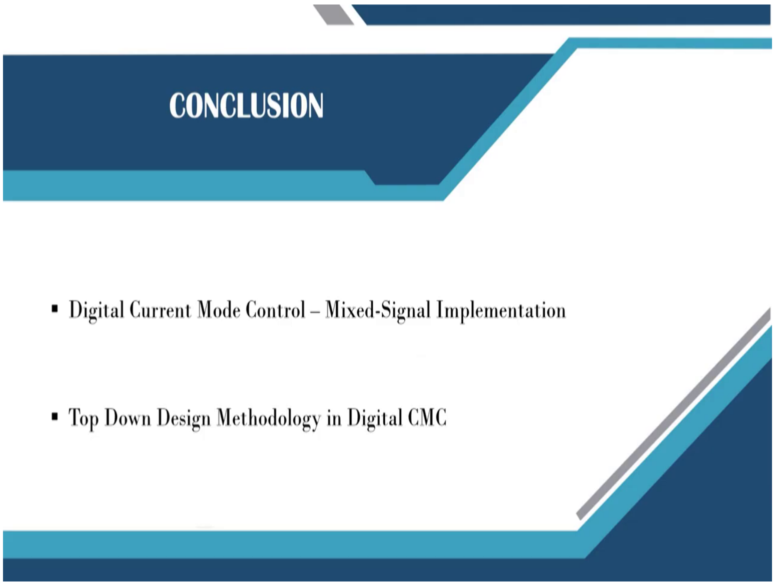

CONCLUSION

- Digital Current Mode Control – Mixed-Signal Implementation
- Top Down Design Methodology in Digital CMC

So, in summary, we have discussed digital current mode control, and mixed-signal implementation; and we have also discussed the top-down design methodology, digital current mode control, and we will be discussing, in the continuation of the next lecture, in more detail, the implementation as well as the Verilog course; that is it for today.

Thank you very much.