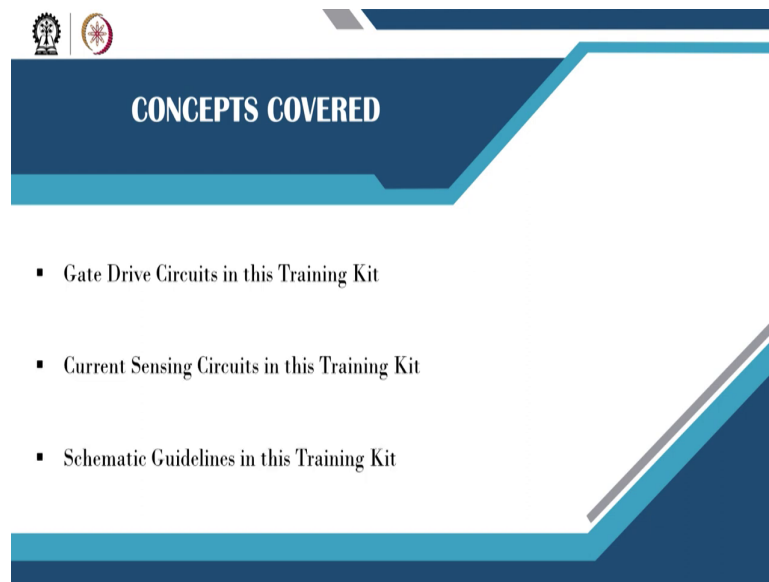


Digital Control in Switched Mode Power Converters and FPGA-based Prototyping
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Module - 06
Digital Control Implementation and FPGA-based Prototyping
Lecture - 56
Reference Power Stage Design and Schematic for Buck and Boost Converters - II

So, welcome back this is the continuation of the previous lecture.

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The slide features a dark blue header with the text 'CONCEPTS COVERED' in white. Below the header is a list of three bullet points, each preceded by a small square icon. The slide is decorated with light blue and white geometric shapes on the right side.

- Gate Drive Circuits in this Training Kit
- Current Sensing Circuits in this Training Kit
- Schematic Guidelines in this Training Kit

In this lecture, we are going to talk about the gate drive circuit in this training kit, the current sensing circuit as well as some schematic guidelines for this training kit.

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Complete Test Set-up for Extensive Demonstration using FPGA kit

Complete closed-loop test set-up for this online course

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So, this is the complete test setup and which is used in our course and I will be showing multiple demonstrations, experimental demonstration case studies, this is a power stage and we have already demonstrated the mixed signal conditioning circuit.

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Basics of CMOS Gate Driver

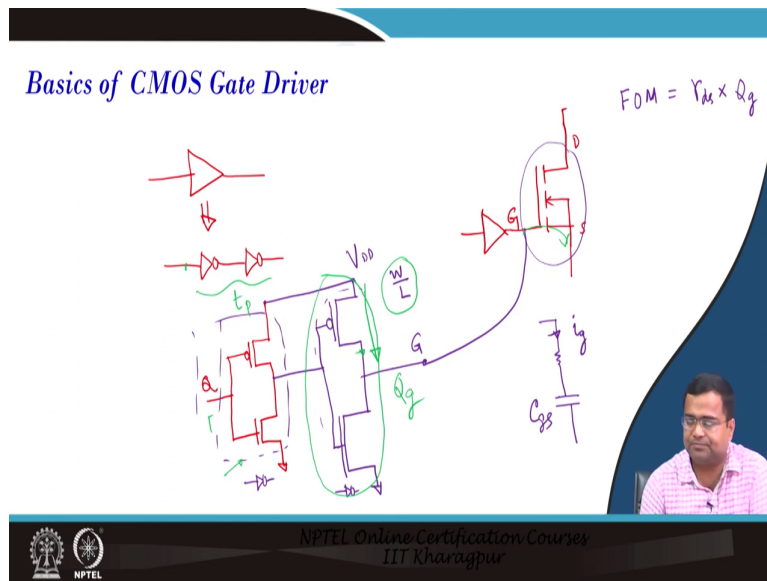
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So, now here are the basics of CMOS gate drive. So, before we undergo through the gate drive circuit we first understand that you know if we consider a MOSFET; that means, you know if we are talking about a MOSFET this is the drain, source and this is gate. So, to turn on, turn off any MOSFET right. So, we need to provide sufficient; that means, it requires a

buffer circuit. What is the buffer circuit? That means this buffer circuit is nothing but back to back inverter CMOS inverter this is a very basic gate drive.

And what does it do? So, if we take a CMOS inverter I think we have discussed this in the earlier lecture. So, it is nothing but a very simple circuit. So, this is our let us say gate signal Q and this is the inverter then we want to connect the other inverter; that means, what we want to show is that this is the first inverter.

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This one represents one inverter then followed by this there will be another inverter, now I am drawing a bigger scale. So, this is V_{DD} and this is going to your actual gate this is going to the gate; that means, this is nothing but this term. So, what does it do? This is also another inverter, but the size of; that means, the W by L ratio is much higher; that means, why? Because the MOSFET requires a certain amount of gate charge to turn on; that means, we need to make the change we need to the fast charge right.

Because if you take the MOSFET very fast you know characteristic there is a capacitor. So, we need to charge the gate capacitor because the gate will have a capacitor so you need to charge the capacitor since the capacitor is largely depending upon suppose you know if you consider the figure of merit of the MOSFET which is the product of $r_{ds(on)}$ into Q_g that is a gate chart.

So, if the $r_{ds(on)}$ is small typically Q_g is large; that means if you are trying to reduce the conduction loss your switching loss increases because Q_g is large and if the Q_g is large; that means, the gate capacitance is large. So, you need a faster charge rate; that means, the driver current requirement is very high; that means, you need this is the gate current has to be sufficiently high to fast charge and discharge the gate capacitance. So, this is I am talking about C_{gs} gate capacitance.

So, the gate capacitance has to be charged very fast to turn on and turn off this device; that means, you need to provide sufficient current and that is why you know this path should carry much more current and W by L should be very high. So, the basic of the gate drive is a two-stage like a two back-to-back inverter the last stage inverter consists of a larger size CMOS transistor, which can carry the high current to fast charge and discharge the gate capacitance of this MOSFET that is the basic starting point of the gate drive.

So; that means, the gate drive is a CMOS technology that first will invert and then finally, invert. So, naturally, this process of back-to-back will also have some propagation delay; that means if you see the actual gate signal Q and here whatever is coming out to Q_g there will be a slight delay because of this back-to-back transistor back-to-back inverter.

But we can understand that this CMOS transistor is responsible for charging and discharging the gate capacitance of the MOSFET and if the Q_g of the MOSFET is high then the peak current rating of this driver circuit has to be large high to fast turn on, turn off this MOSFET.

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Basics of Half-Bridge Gate Driver

The diagram shows the internal circuitry of the STDRIVE600 half-bridge gate driver. It includes a logic section with interlocking and overtemp protection, followed by two level shifters and two driver stages (each with a PMOS and NMOS transistor). The output nodes are labeled HON, HOFF, OUT, LON, and LOFF. Power pins include VCC, VCC(OVLD), BOOT, PVCC, and SGND. Input pins include LIN, HIN, and SD/OD.

Handwritten notes on the right side of the slide show a MOSFET switching circuit with the following equation:

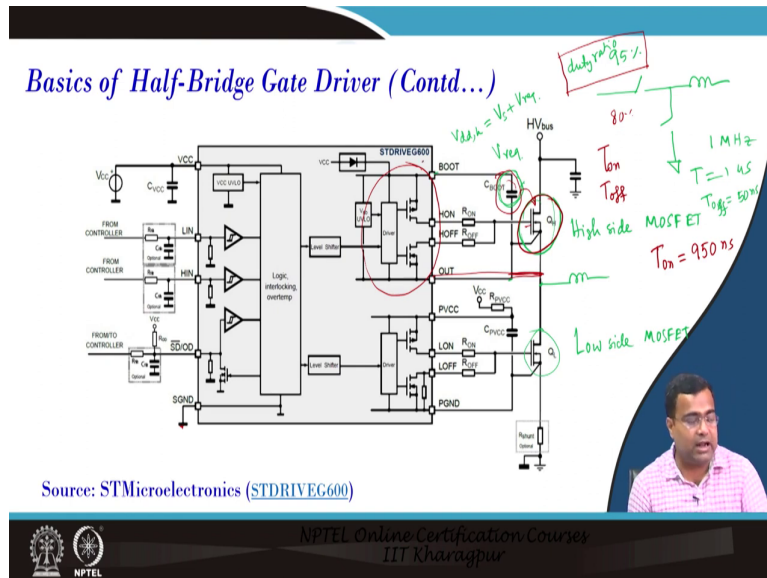
$$V_{dd} = V_s + V_{reg}$$

The notes also include the label "Switching" and a diagram of a MOSFET with a gate voltage V_{in} and a source voltage V_s .

Source: STMicroelectronics (STDRIVE600)

Now, when you go to half-bridge gate drive so, this is one product from ST microelectronics. So, these are the power stage you know will get connected.

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So, I will just connect to the power stage so; which means, this is a complete picture here this is a high side half bridge switch, and the high side switch high side MOSFET, it can be MOSFET or any other device and this is our low side MOSFET; that means if we are talking about a synchronous buck converter from here we generally connect the inductor right, for the synchronous buck.

But here this is a driver. So, we need to turn on and turn off this high side and low side gate drive so; which means, the job of this particular device in the previous. This is a back-to-back transistor that I told you will turn on, and turn off; this is a back-to-back transistor ok. Now, for the low side, the ground is a reference. So, it is easy. So, we can create the gate drive voltage and you can turn it on and turn it off.

But what will happen on the high side where, the source of this MOSFET is floating so; that means, you need to do something; there are two ways either you can create; means, the gate drive voltage; which means, I am saying that you have a MOSFET, which is like this. This is a high-side MOSFET where the source is floating, it is floating the source voltage can vary based on the switching condition and this side can be input voltage or something else.

So, now I want to create a driver. So, the driver will be the driver's ground. So, the driver ground should be connected here, now than driver also needs a supply V_{dd} . So, the driver supply should be such that the V_{dd} should be V_s that is this voltage plus your I would say the required voltage; the required voltage to turn on or turn off the MOSFET.

So, the voltage in the case of the low side is 0. So, let us say the MOSFET gate voltage is 12 volt, 10 volt. So, this will be the 10 and 12 volt, but this volt. So, you have to create a voltage here which will be a look that will add this voltage over the source voltage which is floating. So, how to achieve that? So, this is a gate drive circuit ok.

That means, this driver how to do that? So, one way is that we can use a bootstrap arrangement because this is a bootstrap capacitor. So, this capacitor will be charged to that required voltage; that means, this will create the required voltage, this will add up with this source voltage and it will finally, generate the create the V_{dd} .

So, your V_{dd} for the high side gate drive will be V_{source} plus $V_{required}$, and this required voltage will be you know stored I mean it will be created by the bootstrap. So, this bootstrap capacitor is responsible to create that additional voltage required voltage for turning on and turning off.

So, this capacitor if it should be somewhat large at the same time should provide a certain on and off time to balance the charge and discharge, otherwise, you know if your off time is too small or if you turn off the switch continuously. Sorry, if you turn on this switch continuously; that means, in a buck converter we have this high side switch and the low side switch. Sorry, we have this high side switch and the low side switch, this is the inductor.

Now, suppose we want to achieve let us say 95 percent duty ratio is 95. That means if you are operating a switching period of 1 megahertz; that means, your T is 1 microsecond then what will be your on time? If it is a 95 percent duty ratio so, it will get only 50 nanoseconds, sorry 99, off time is the off time, and what is your on time? T_{on} so, T_{on} will be 950 nanosecond. Now, during T this capacitor has to supply to this gate; that means, this will be charging the capacitor of the MOSFET the gate to source capacitance as a result this bootstrap capacitor discharges.

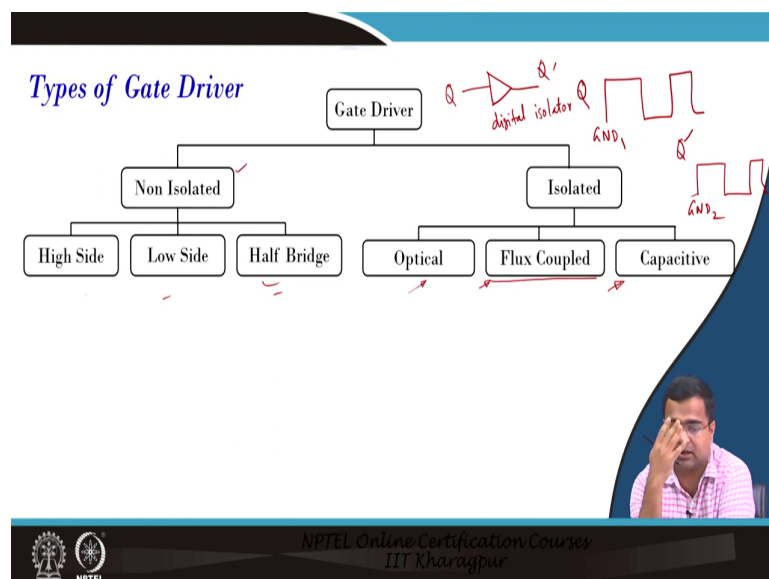
So, if the bootstrap capacitor is not too large then it will actually discharge and it cannot provide sufficient voltage and the MOSFET can turn off, but if you put a too large bootstrap capacitor then the time constant can be large and that will create another problem.

So, that is why in the majority of the current commercial product they put a constant in terms of duty ratio; that means, you may not reach 95 percent some products may go like 80 percent or so, it all depends on what is your time period and what is the absolute I would say on time or absolute off time.

So, those will decide the bootstrap capacitor design, but in summary, I would say the high side circuit we may require a bootstrap capacitor to solve. But there is another approach we may not need a bootstrap if we can generate the driver supply through an isolated power supply; that means, here the driver and everything is generated from the common ground which is the same as the power ground.

But if we can create isolation with the supply of the driver and the supply of the power state, then we can easily connect this here of the driver ground, which is an isolated ground that can be connected to the source, and then we have to simply generate the additional voltage here so, that also require isolation.

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That means the type of gate drive can be non-isolated which is a bootstrap, high side, low side, or half-bridge, we have discussed half-bridge, the low side is much simpler this is just a

back to back the simplest one is the back to-back inverter we have discussed and the high side we may need a bootstrap arrangement and half-bridge we have discussed. Isolated how do you isolate so; that means, there are isolation can be optical isolation, but this will also have a limit in terms of switching frequency because, it cannot be so fast turned on, turn off may not be possible because of the bandwidth limit.

Similarly, if you go for magnetic isolation using flux so, it can use a high-frequency transformer it still has a limit in terms of switching frequency. Now, people are going for capacitive isolation, which can be faster and you know like a digital isolator.

Suppose you want to know because this is for an isolated converter, suppose you have a gate signal let us say you have generated gate signal Q, but this gate signal concerns some ground 1, but you want to generate a gate signal dash, which will be same, but it is with respect to some ground 2, then what will do? Between Q you need a digital isolator and Q dash.

So, this is something like a digital isolator. So, this can be a capacitive isolator which can be much faster and can support 10s of megahertz switching frequency even far. So, these are the challenges now coming when you are going for a half-bridge gate drive for gallium nitride devices as well as silicon carbide high frequency where you may not simply go for a traditional isolated device. So, how to deal with gate drive and there are many research as well as the commercial products are coming up.

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Gate Driver (Bootstrap)

In the training kit, bootstrap half bridge gate driver is used.

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So, the gate drive booster arrangement we have discussed. So, the bootstrap has to supply to this gate. So, we need to make sure that sufficient off time is maintained and the time constant should be so we have to decide the on time of this switch and the time constant there should be some kind of balance otherwise it may discharge. So, in this training gate, we have used a half-bridge gate driver with a booster arrangement.

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Current Sensing Circuit

• Shunt based current sensing offers high bandwidth sensing with minimum time lag

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Now, the current sensor so, here we have used a shunt inductor; that means an inductor with a resistive sensor. So, I have used a resistive sensor, but when you want to sense this we have to step it down depending upon what is the voltage level and if you do that then there can be some parasitic inductive effect because of this. So, we need to put compensation in the capacitor.

So, this is a compensation network and these two will go to the two differential arrangements, this is a differential amplifier and it will convert into a single end voltage so; which means, we are getting a voltage that is R_G / R_1 into the shunt resistor that we are using.

So; that means, we need compensation in the capacitor to because what we will see if this is your actual inductor current then you may find that the sensed inductor current might will have some kind of noisy stuff switch node stuff. So, to reduce this effect we need to put this capacitive network, but if you put a large capacitor there can be phase lags. So, you have to be very careful about this selection.

So, in this you-know training kit, we have used this resistive sense sensing with capacitive compensation and a differential amplifier.

(Refer Slide Time: 16:23)

Voltage Sensing Circuit

$$V_{OUT} = (R_G / R_I)(V_O - V_{PGND})$$

- Differential sensing eliminates switching noise at the output

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So, for voltage sensing also we have used respect to the power ground a differential arrangement and converted it into single-ended. So, here; that means, we have used the actual output voltage and we have tried to match. So, this is to reduce the common mode noise. So, eliminate the switching noise at the output because we need to also try to avoid trying to reduce the noise effect.

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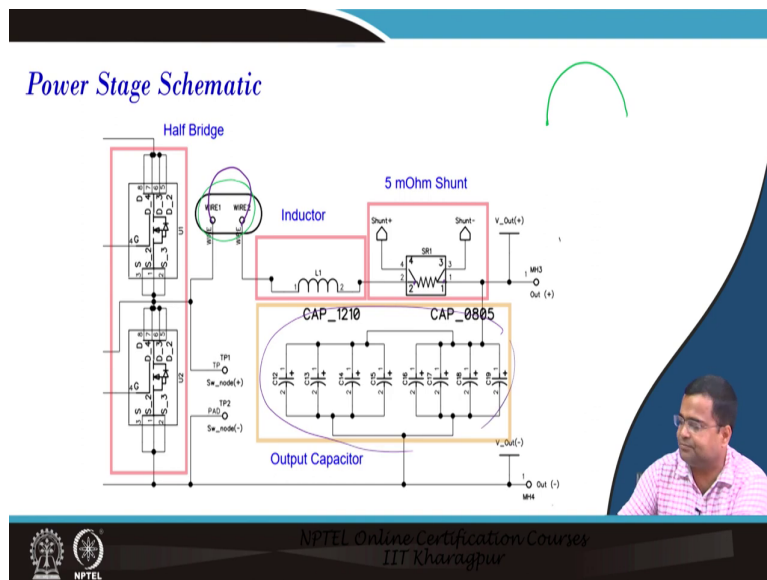
Power Stage Schematic

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So, the power stage schematic here is the input side bank of the capacitor then we have. So, this is the input stage then after the input because you are talking about the buck converter this is the half-bridge MOSFET that you have used, then the MOSFET gate drive circuit is used here, the bootstrap arrangement all these things we have used here.

And after the high bit gate drive we have put a gate resistance; that means, we have this gate drive circuit this is like a buffer circuit we have discussed, then you put a resistance gate resistance and this goes to the actual MOSFET, which has this kind of arrangement ok. So, this is gate resistance for both the MOSFET. So; that means, this is a half-bridge bootstrap gate drive we have used.

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Then after this half-bridge now this is a tapping point; that means, we need to put a wire; that means, we have created a loop and if we go back to our teaching kit; that means, let us go back, we want to show that this is a loop we are talking about this is a loop; that means if we take a different color. So, we are talking about this particular loop so, that we can tap the current probe here.

So, for that, we have made an arrangement here and there that we can connect this wire so that we can connect our current probe. This is an inductor and this is a sense resistor, the shunt that we have discussed for the current sensing and this is the output side capacitor.

or disconnected if you want; that means, we have some continuous resistance let us say this is the capacitor of the buck converter, this is the inductor and we have kept another resistance with switch.

That means if you turn on the switch this two resistance will come in parallel and then effective resistance will be reduced. So, it will make a load step-up transient and if you remove it, it will get a load step-down transient.

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Voltage Sensing Circuit

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So, voltage sensing is the voltage sensing circuit we have discussed which is a differential amplifier used that tries to reduce the noise.

So, we have discussed somewhat detail about our you know teaching kit you know and, but again this experimental development and hardware prototyping is not mandatory for part of this course, one can use their existing teaching kit, but in the subsequent lecture we will show how to implement digital control using FPGA various step. So, it is more important to understand the algorithm and basic concept of different architecture; that is it for today.

Thank you very much.