Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

Prof. Santanu Kapat
Department of Electrical Engineering
Indian Institute of Technology, Kharagpur

Module - 06
Digital Control Implementation and FPGA-based Prototyping
Lecture - 54
Signal Conditioning Circuits and PCB Design for Mixed-Signal Implementation

Welcome. In this lecture, we are going to talk about Signal Conditioning Circuits and some aspects of the PCB schematic for Mixed Signal Implementation which we have used in this you know hardware prototype in this course.

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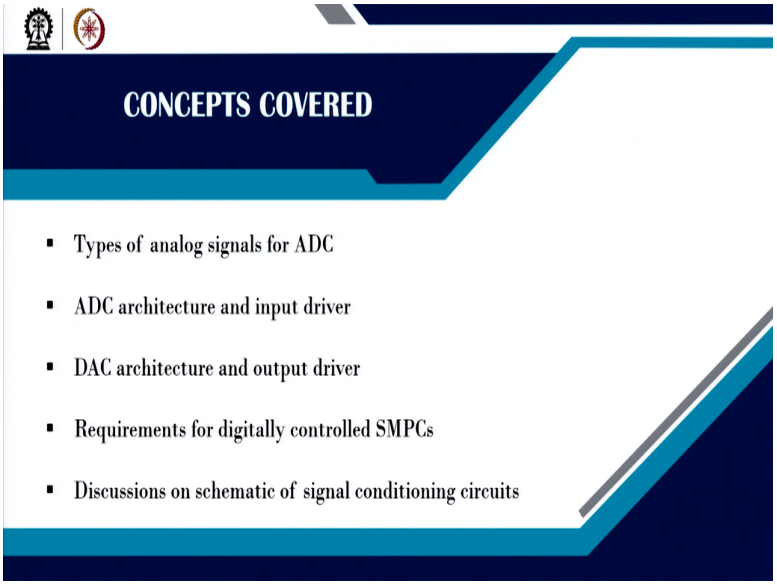

So, we will first talk about the type of analog signal for ADC, then ADC architecture and input driver. Then, the DAC architecture output driver, the requirement of digitally controlled SMPC, and some discussion on the schematic of the signal conditioning circuit.

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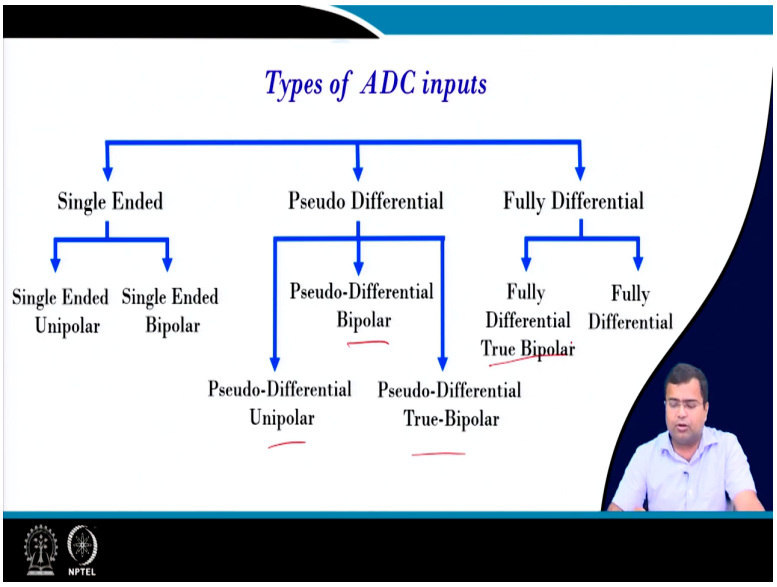

So, here types of input. ADC input can be either single-ended or it can be pseudo-differential or fully differential. So, under single-ended, we can have also single-ended unipolar, and single-ended bipolar. Then, similarly under pseudo differential, you can have a bipolar, unipolar or true bipolar or you can have a full differential in terms of true bipolar or just the full differential.

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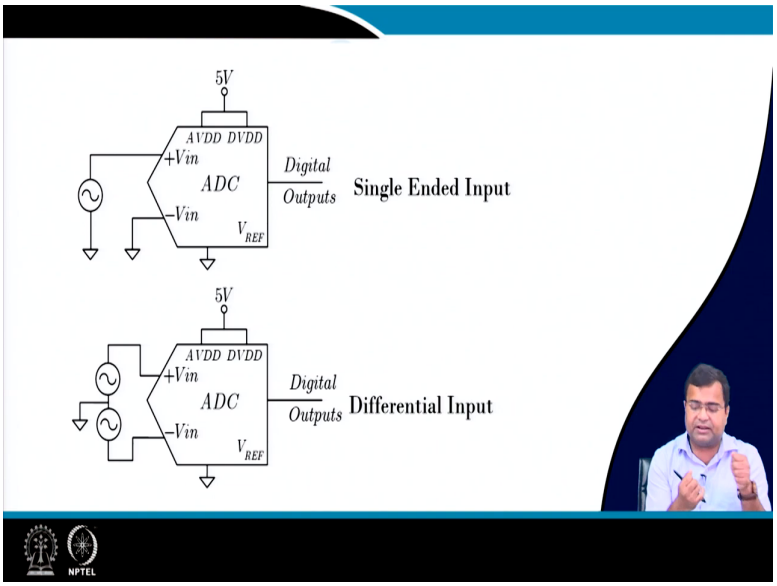

Now, if you take a single-ended input; that means, generally the ADC input is set and the negative terminal of the analog input is set to 0 ground and the positive terminal we apply the

input signal. Then, in the case of a differential signal, we use you know differential signal; that means, the midpoint and then we generate the difference. So, you need a differential converter; that means, single-ended input differential conversion or if you have direct directly available differential data, you can just plug it in here.

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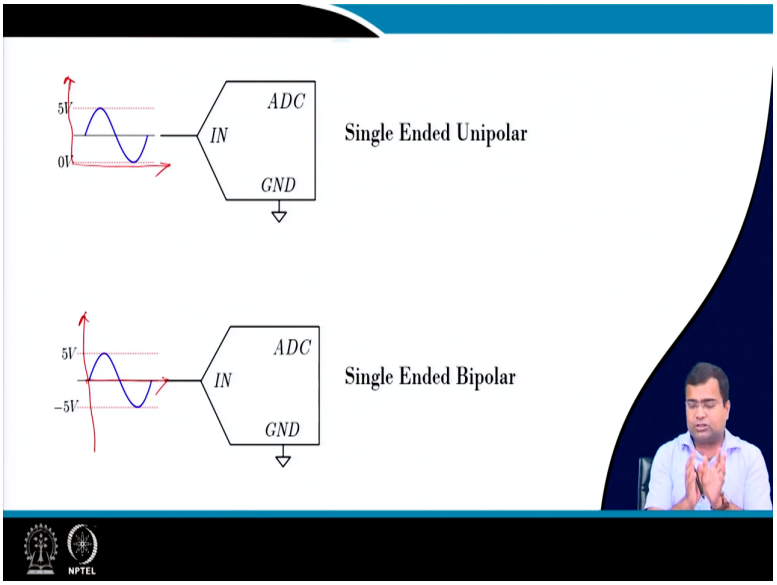

Now, in single-ended we are talking about the signal will vary from 0 to some positive. So, it is unipolar; that means, the signal will always vary between 0 to you know 5 volt or 2 volt. In general CMOS architecture, it is generally 2 volt, 0 to 2 volt. The IC we are using is 0 to 2 volt. Then, the single-ended also have a bipolar; that means, you can have the signal varying from minus 5 volt to plus 5 volt, which is also single-ended ok.

So, also you have to check whether all ADC support that or not because whatever we are discussing these are common discussions. We are touching most of the input cases, but one has to check and go to the datasheet whether such possibilities exist for that particular ADC or not.

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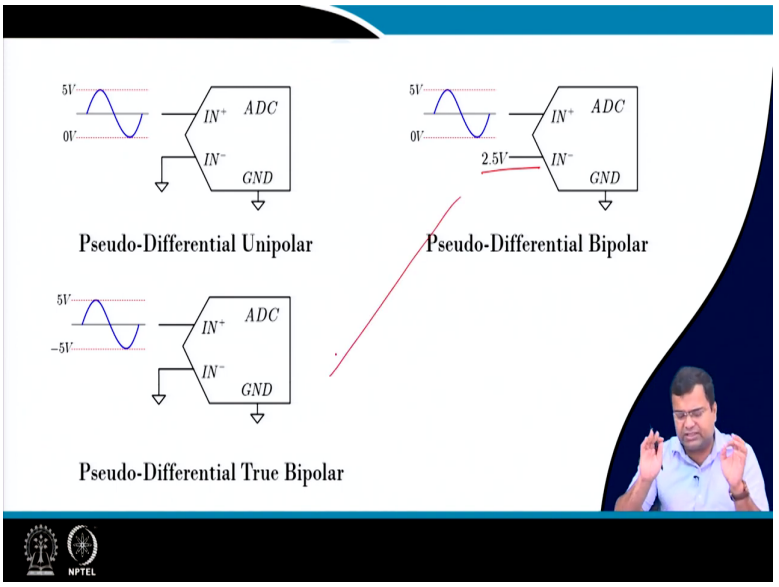

Next, pseudo-differential. In the case of pseudo differential, again we are using an input where the input negative terminal is grounded and the positive terminal you can have you know a pseudo-differential with bipolar. Then, we can set 2.5 volt in the input voltage. Again, these are all specific to that particular ADC and this you know instruction will be given to the data sheet of the ADC. So, here we are showing some generic cases.

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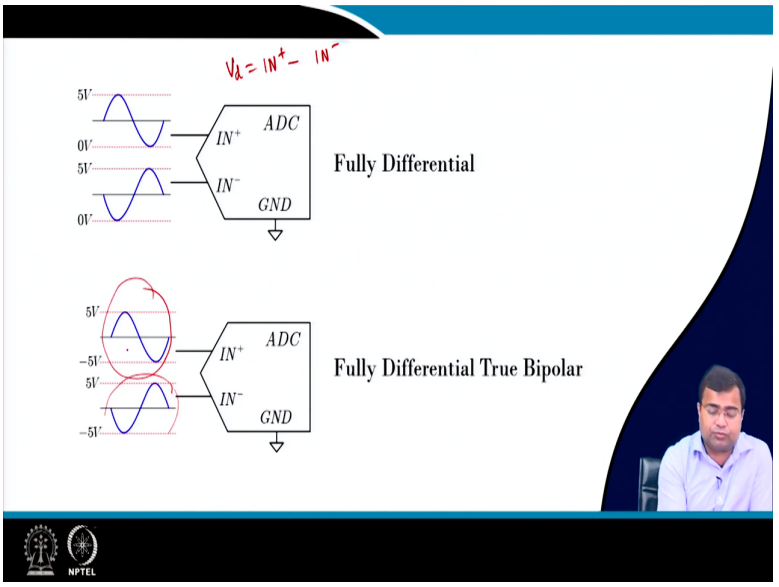

Fully differential, if we are giving two signals one side is the positive swing both are positive swings, but they are anti-phase, you can see out of phase. Then, we will get a differential

signal as if it is input plus; that means, here the signal will be differential signal will be input plus input minus ok. Fully differential true bipolar; means, the signal of each channel can have a bipolar plus minus 5 volt for each channel. But of course, there has to be out of phase, both of them are out of phase.

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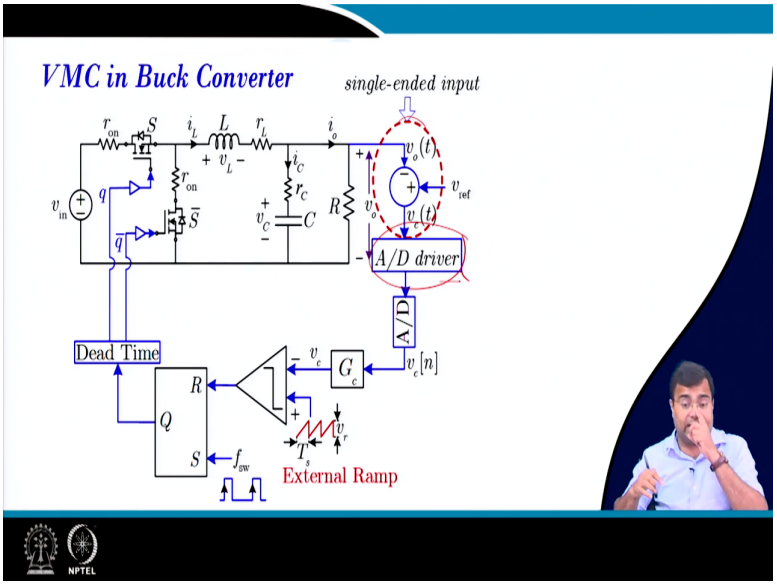

Now, in the case of the voltage mode control buck converter, we are talking about the error voltage right? So, if we sense that we put the ADC here. So, here ADC is set as the error voltage.

So, ADC has to support negative and positive both; that means, you know here we can use a differential ADC or single-ended ADC. If it is a single-ended ADC, then also the single-ended ADC should support both bipolar signals that we have discussed. And, if we sense the inductor current right so, inductor current we are sensing a sense of resistance. So, it is a differential input.

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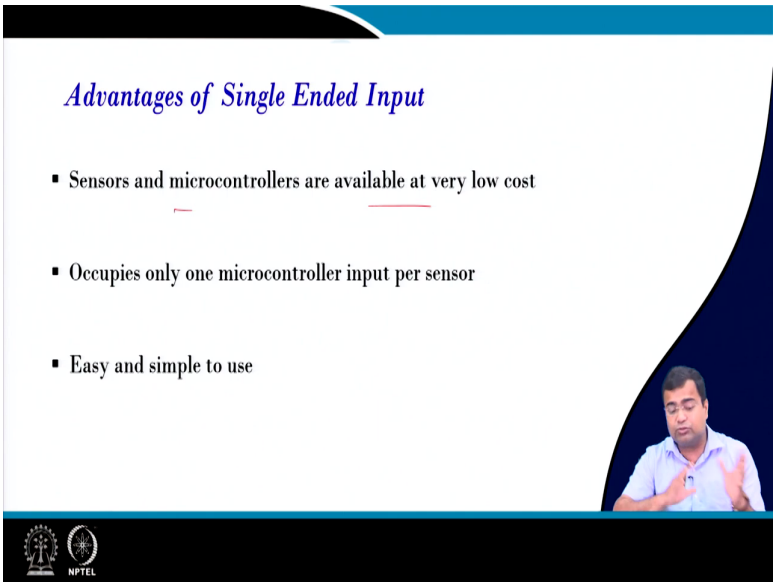

So, we can use a differential ADC and or we can have a differential driver which will convert the differential signal into a single-ended, and then we can give it to ADC. And, we will be talking about the ADC which before that we need to have an ADC input driver ok. The advantage of single-ended single-ended inputs is available and are very cost-effective.

And, you know you can have only one input terminal and there is no differential; I mean there is no requirement to have a separate you know op-amp for converting single-ended to a differential signal.

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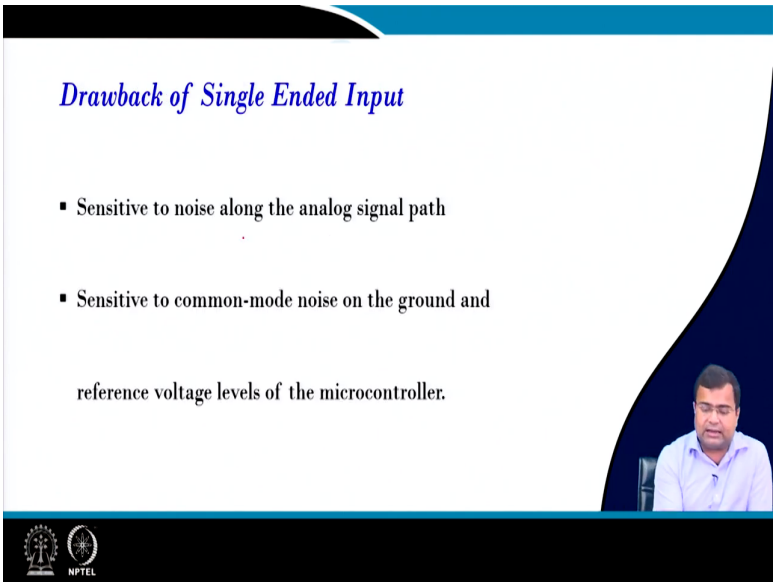

But, it drawback at it is noise; that means, a common mode noise is a problem for a single-ended signal and it can affect the signal SNR.

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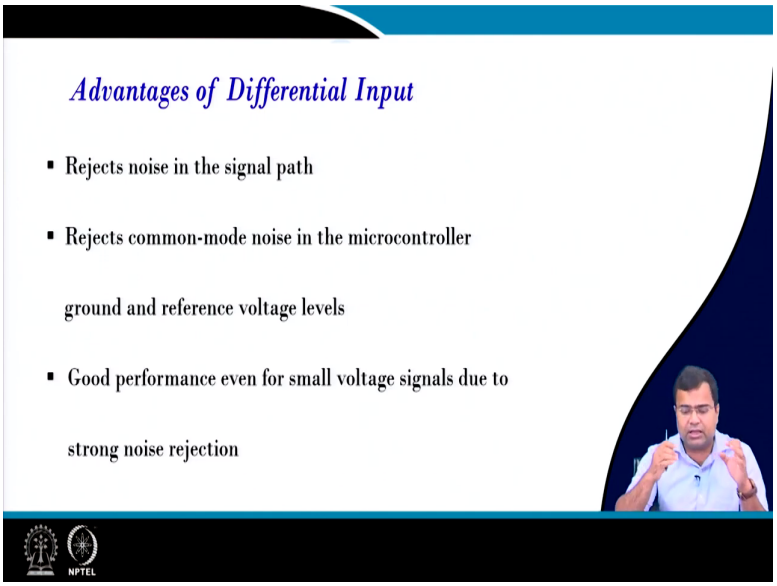

But, if you take an analog differential signal, it rejects the common mode noise. So, you can get a clean signal, and also it has a good performance, particularly when we are dealing with a very small signal. Particularly, when we are talking about biomedical signals or other signals where the signal can be corrupted by noise. So, we need it is better to use the differential configuration.

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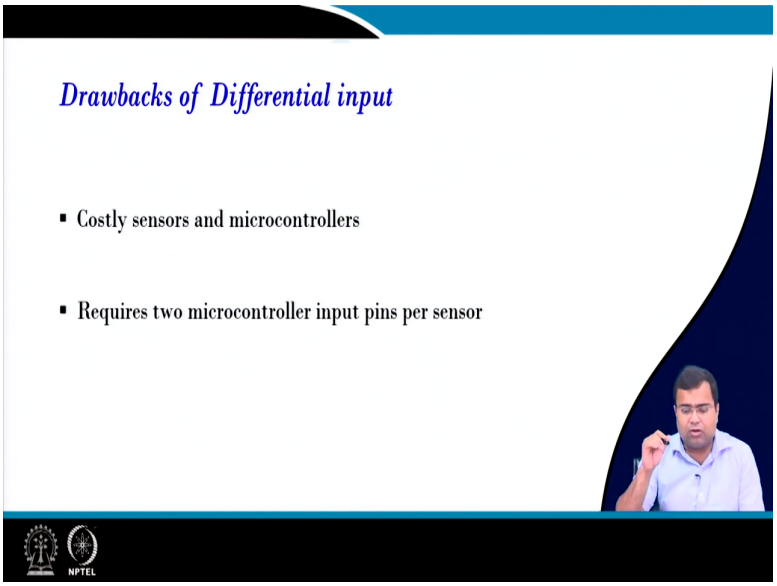

But, the drawback is that it is costly. You need a separate you know arrangement for converting single-ended to differential and also you need two pins of the ADC.

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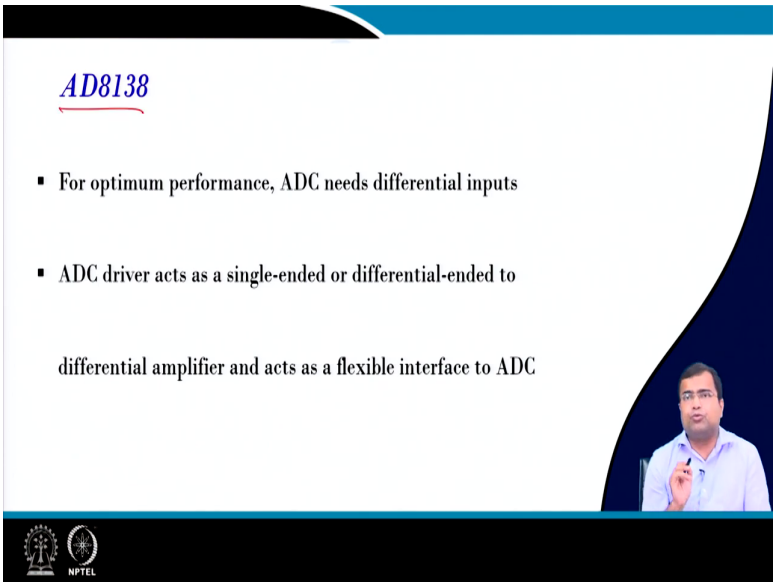

Now, the AD8138 is the ADC driver input driver of the analog-to-digital converter. So, to optimally use the ADC; that means, we need various things; that means, we need to ensure that the ADC terminal should not be loaded. And, if we use a differential ADC configuration then this has to be a differential conversion that should be possible; that means, this ADC driver acts as a single-ended or differential ended too.

So that means, it is it can convert into differential and it acts like a flexible interface between known actual signal and sense signal to the ADC.

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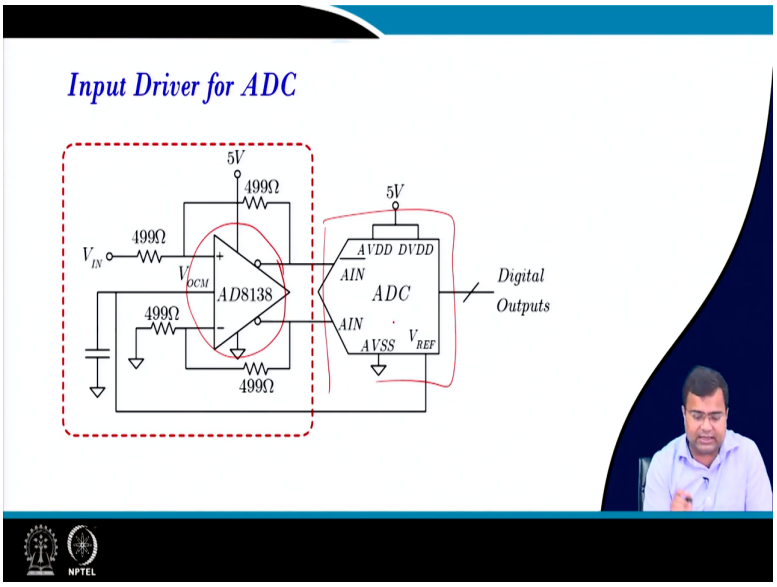

So, the input driver of the ADC that we are using in our course, is the hardware kit. We are using AD8138, which is the input driver for the A to D converter that we will be talking you know what is the architecture of ADC, that we will be we will discuss. But, this is the driver that we have considered for our hardware.

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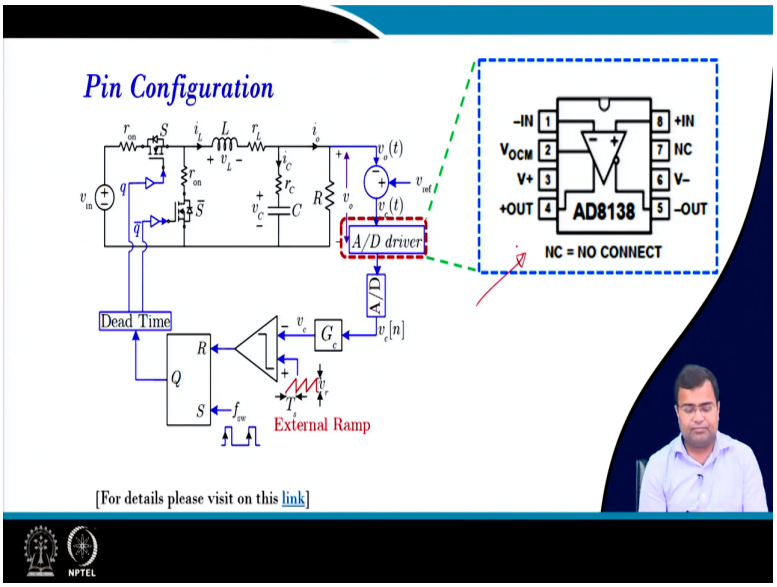

Regarding the pin configuration, if you go to this now we are talking about the ADC driver. So, this is AD8138 and we can accordingly set the pin and this pin configuration will be available in the datasheet.

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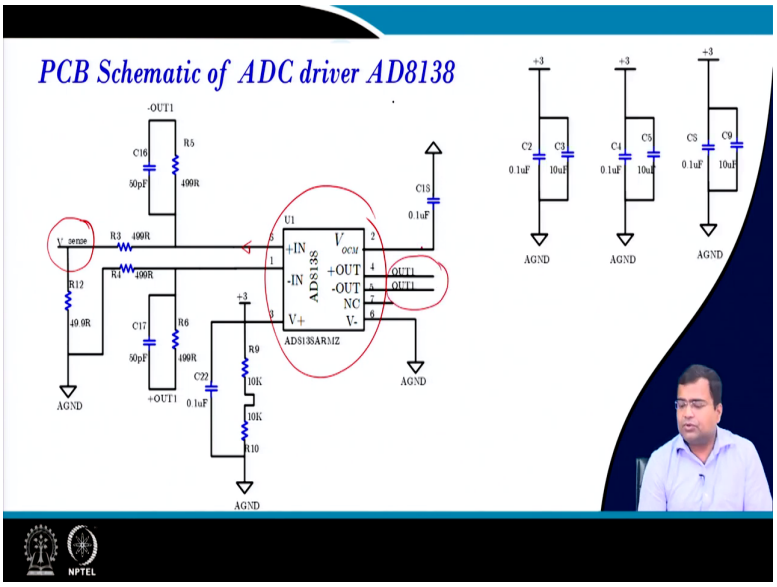

Now, if you are talking about the ADC driver schematic. So, this is the schematic that we have used for making our PCB of the schematic conditioning board. So, this is the driver circuit and we have used a positive terminal. Suppose, if you are using a sense output voltage and then we have used a negative terminal as a ground terminal which is the analog ground.

And, then we have used some filter arrangement to make sure that you know we can attenuate some noise, because you know we are talking about the sense voltage, and sense voltage we can we may use a resistive divider at the output terminal. But, after that, we should put a low pass filter so, that we try to attenuate the effect of high-frequency noises and switching noises. Then, the driver and the output of the driver go to the ADC.

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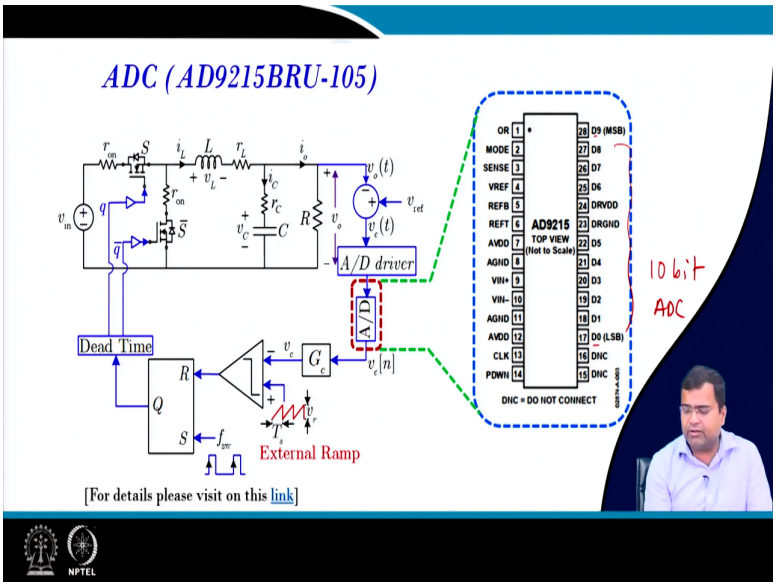

Then, if you talk about this is the ADC that we have considered for our hardware case study. And, this is the analog device AD, you know 9215, and this driver has a digital interface which is the parallel interface and it is a 10-bit ADC. You can see 10-bit ADC, where it has D0 to D9, D0 is the LSB and D9 is the MSB. Then, for detail, you can go to the product data sheet.

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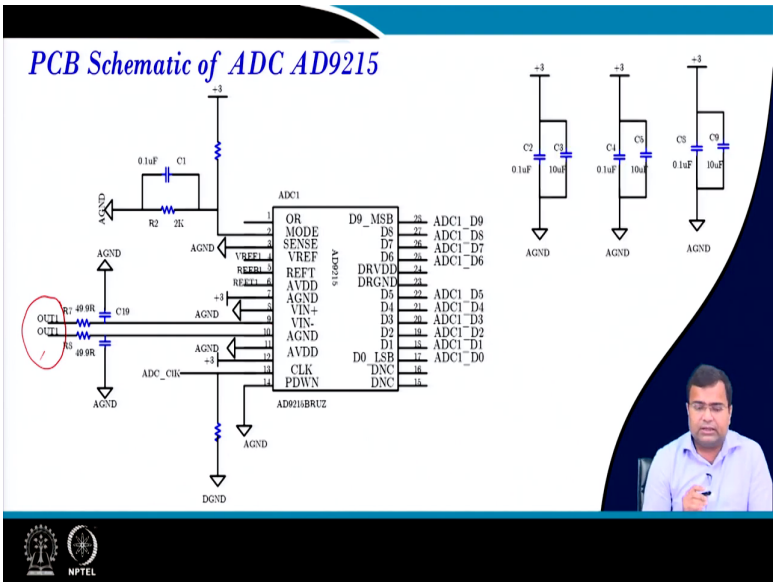

So, for the schematic of the ADC, we are taking the two signals from the ADC driver. Now, these two are the differential signal and they have connected accordingly their V in plus and

V in minus terminal. And, then the remaining circuit that we have made according to the recommendation made by this particular device, particular part number, and we have made this PCB schematic and that is used to making our PCB.

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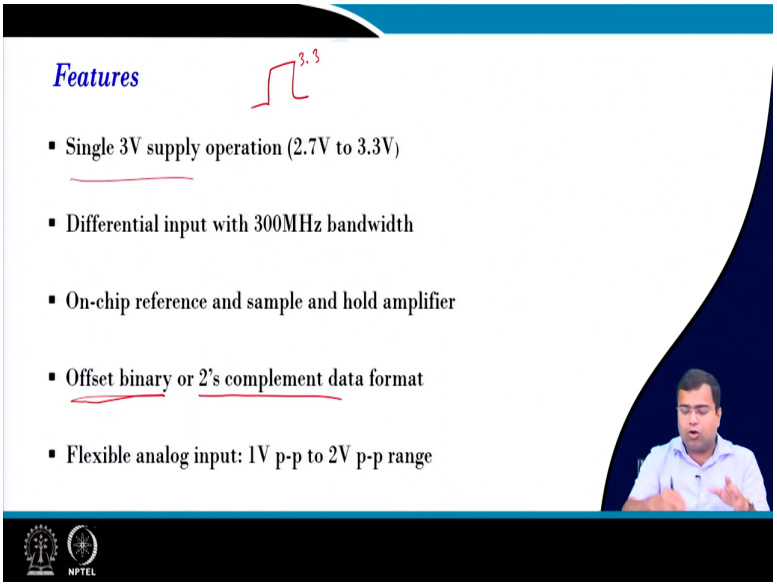

Next, the feature. This ADC offers 3 volt supply single supply; that means, this supply is common for both analog and digital, because you may find a different type of ADC. Some ADC may have a dual supply rail. One rail for the analog channel and another rail for the digital channel because sometimes we need a different logic level and logic voltage level for the digital. So, some ADC may have a dual rail supply.

But, if you have a single rail; that means, the output is higher voltage; that means if you have a logic out 1 which corresponds to 3.3 or 3 volt. So, if you want to convert it into 1.8 volt logic voltage, then you need to use an additional buffer circuit where you can have two different rail buffer circuits, which is possible. That means, you convert one CMOS technology to another technology, and you can use a digital buffer that can convert the voltage level to another voltage level.

But, this ADC has a single rail and it accepts differential input signals with high bandwidth it has and it accepts the offset binary or 2's complement depending upon the setting that we are making at the ADC. And, you have to be very careful to this understand how to set offset binary or 2's complement; one needs to go to the datasheet of this particular device. But, in our case, we are using 2's complement.

And, flexible analog voltage, analog channel generally we have a 2-volt peak to peak that is why it is a CMOS technology. But, if you use a differential configuration, it can be from minus 1 to plus 1 volt, or in single-ended, you can set it to 0 to 2 volt also.

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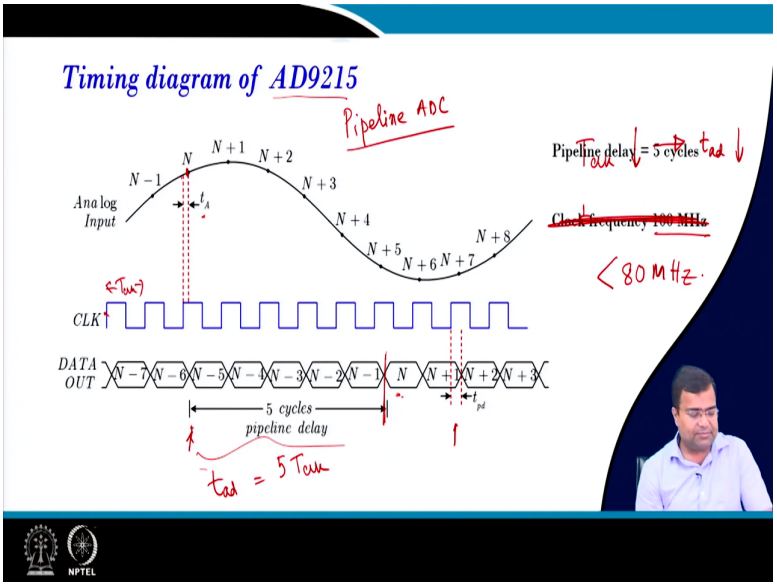

The timing diagram of the ADC. This ADC is what AD9215 is, we are using a pipeline ADC. This is a pipeline ADC. For this ADC we have made a pipeline because if we want to use convert multiple you want to digitize multiple signals, it is possible you can put an analog mux at the input. And, then you have to synchronize the output side of the digital and analog, you have to synchronize. But, intan interesting point here in the pipeline we have discussed the conversion time depends on the number of pipeline cycles.

It is not absolute like in like a flash ADC or SAR ADC, where the conversion time is more or less you know given in the datasheet. But, here the conversion time depends on the pipeline cycle. So, if we use a high-frequency clock; that means, let us say it is a 5 cycle of the T clock, where this is the time period of the T clock.

So, the 5 cycle is the ADC conversion time. For example, I am just taking the raw data, but it may be larger. If you use a high-frequency clock, the T clock can if we reduce; that means, we are increasing the clock frequency.

Then we can reduce the ADC conversion time; that means, this will lead to t ADC conversion time will also get reduced. But, at the cost of a higher sampling rate, the power loss of the

pipeline ADC can increase; so, you have to be careful. Similarly so; that means, if you try to sample here, first there will be an acquisition time. So, if we are taking the sample here, the data will be available here. Here the data will be available that the Nth data.

That means, we have a delay and we have discussed that what is the effect of delay we have considered MATLAB case studies, how to model the delay, and how to match it with the large signal discrete-time model. We have discussed this in lectures 35 and 36. So, such delays are coming one of the reasons is the ADC conversion time, and the other is the DPWM time.

So; that means if we are using here 100 megahertz clock or sorry we can reduce the clock. 100 megahertz is too fast depending upon this ADC that architecture using, it supports like 80 mega samples.

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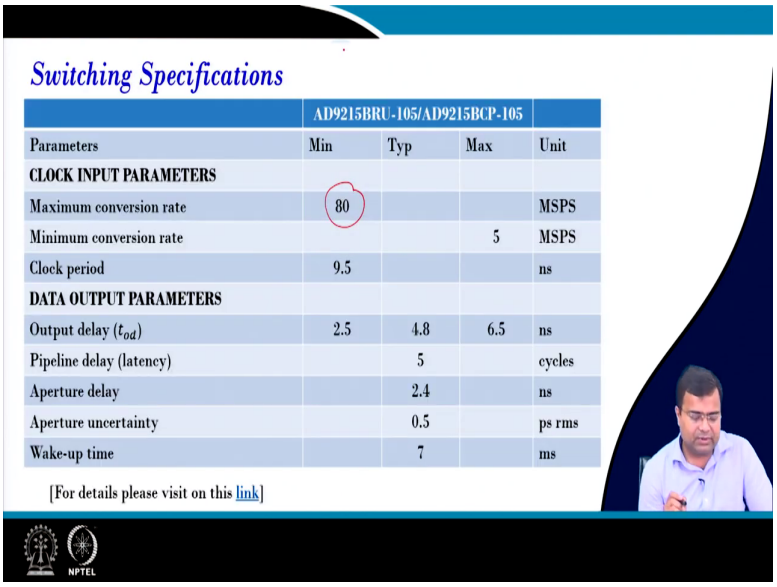

So, it is supposed like a minimum 80 mega sample conversion rate, it can. So, it can you can increase the conversion rate, sorry maximum is 80 mega samples per second. So, we are using an even lower sampling rate. So, this 100 megahertz clock frequency should not be used. It should be smaller than 80 megahertz because the ADC conversion rate is less than that. And, this is the specification that you can get switching specification for the product data sheet and the part number is AD9215, which we have used in our hardware kit.

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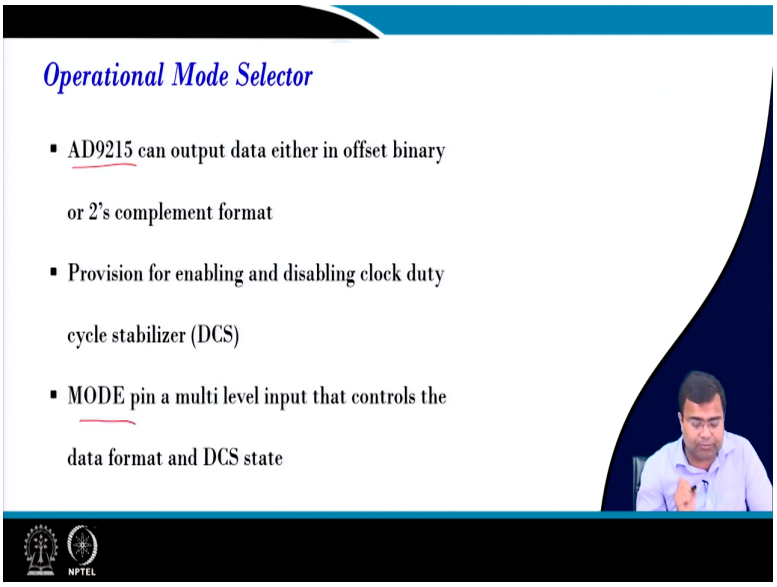

Next operational mode, if you go to the datasheet you know how to set offset binary 2's complement. Then, you can also enable or disable the duty cycle stabilizer and there is another pin that can control the data format; that means, what data format you want whether it is an offset binary or 2's complement.

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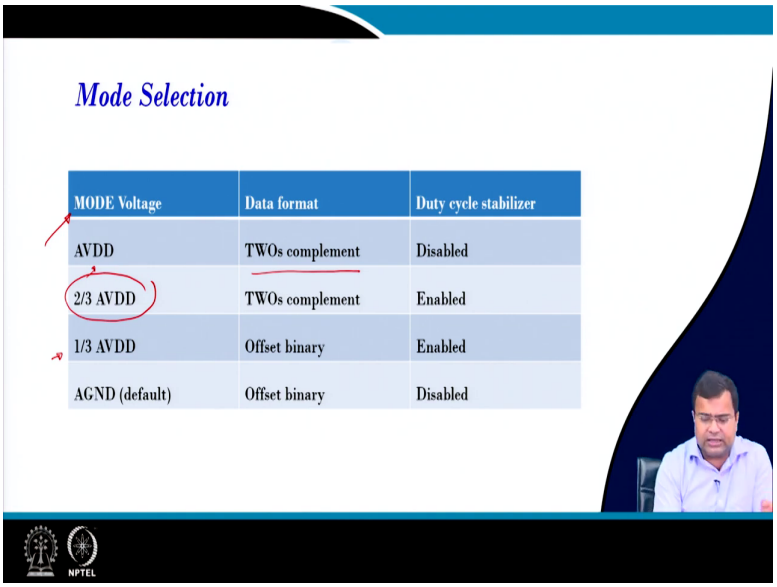

The mode selection. Now, here if we set the AVDD voltage, data-centered twos complement form. Then that means, the mode voltage if you set two-third of that, then the duty cycle stabilizer. So, all these features are given. If we reduce this voltage to one-third, then it will

act like an offset binary. So, the mode selection depends on the mode voltage, what voltage you are setting, are you using two-third or actual VDD. Then so, generally, we use twos complement.

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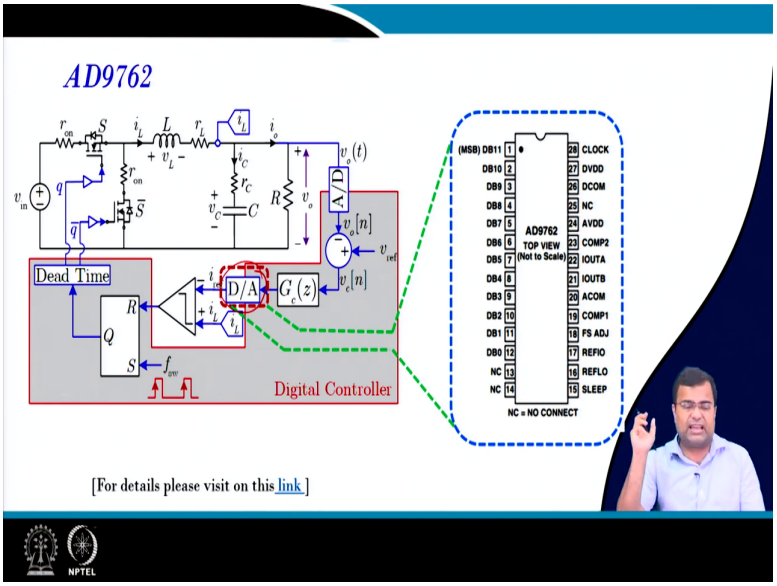

Now, we are talking about the DAC. We need a DAC for the digital current mode control mixed-signal, where this is the DAC, and this DAC we are using here 12-bit DAC. Because, the DAC resolution should be higher than the ADC, otherwise it may end up with limit cycle oscillation.

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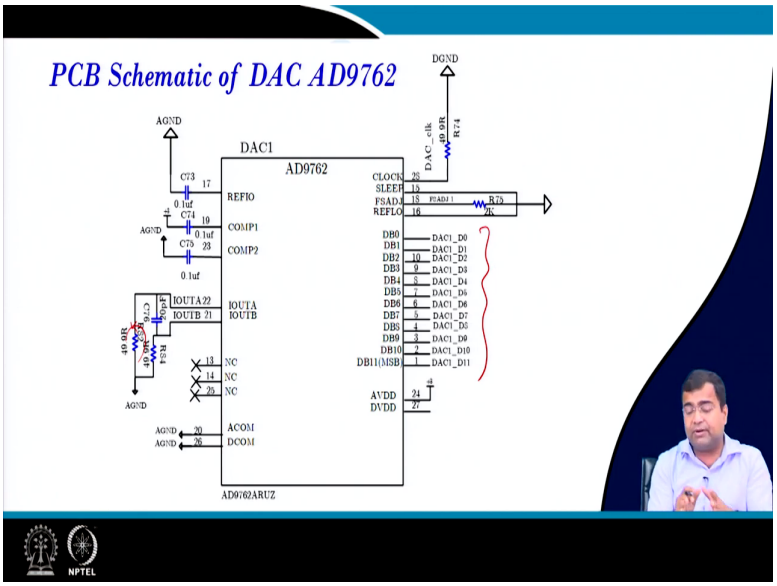

So, the PCB schematic for the DAC. Again, this DAC accepts the digital data which is coming from your digital controller. And, then this DAC output is current and it has to be converted into voltage by placing a resistance. But this DAC has a very low driving capability; that means, if you want to use the output of the DAC and try to compare it with the comparator, then your device may not function properly.

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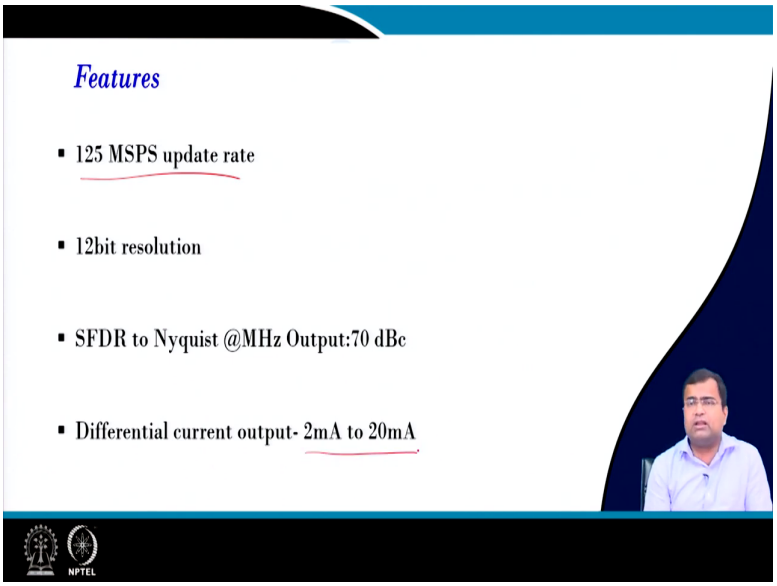

So, to support that, this DAC is very fast. It supports up to 125 mega samples per second, 12-bit resolution and the, but the current carrying capability varies from 2 milliampere to 20 milliampere.

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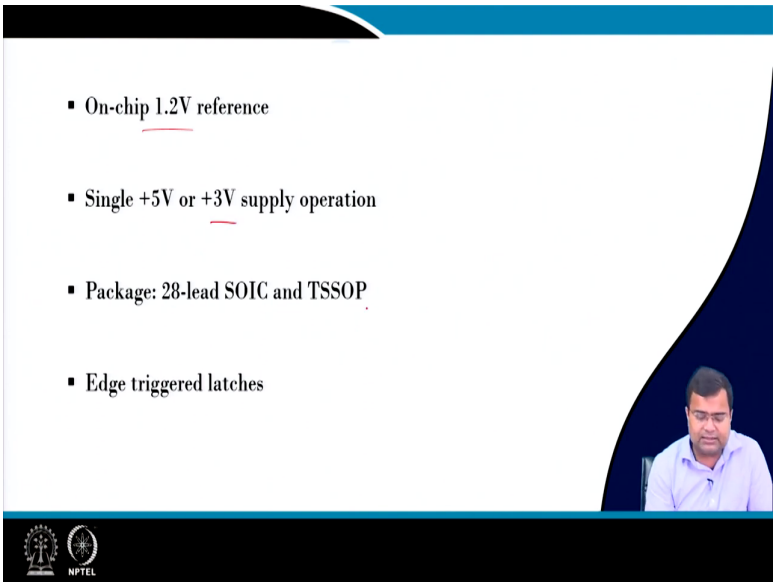

So, it is also an on-chip reference. So, it has a single supply, we can use 3 volts and we are using SOIC or TSSOP package, edge-triggered latches.

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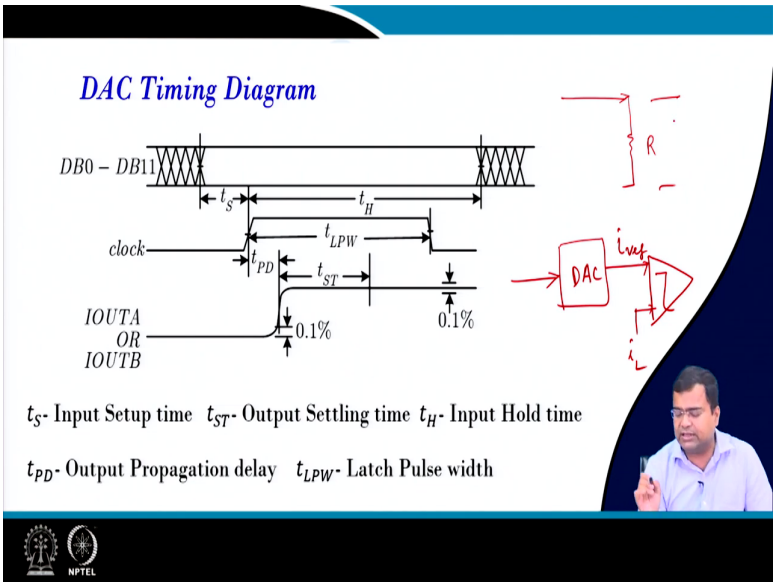

But, I have discussed that if you use this DAC, where it takes the digital data and it converts into the current. So, the digital data is converted into the current, and this curry is coming, it has to pass through a resistance. And, this voltage we are sensing.

Now, this is current and these are the timing parameter. These currents, this voltage cannot be directly driven and we cannot consider this voltage you know, let us say we are talking about the reference current because we have a DAC. And, DAC output is our peak current reference, our reference current which has to be compared with our analog comparator which is like a sense inductor current.

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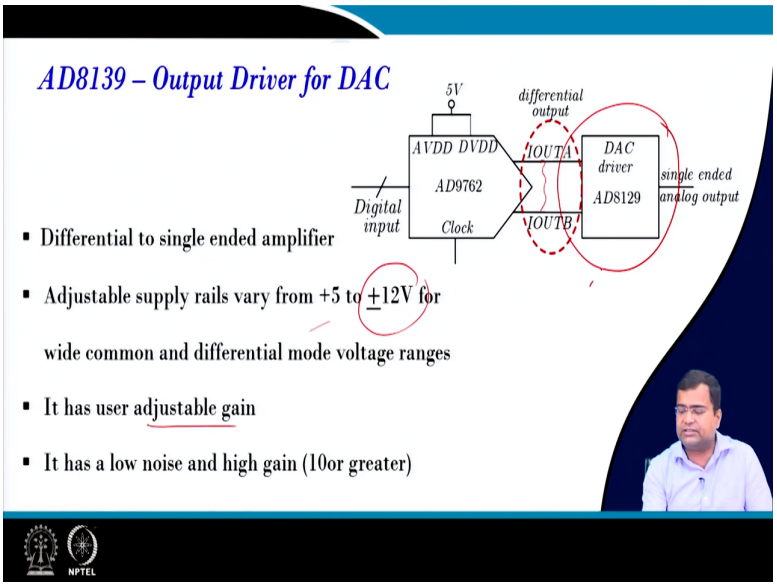

So, we want to use this output of the DAC to the comparator and it is not recommended to directly use this because we need to use a driver. So, we need an output driver and this is the DAC driver which will ensure that sufficient driving capability of this signal. And, we can also amplify the signal because the output voltage level can be very small. So, this is the differential to single-ended.

And, then because the output of the DAC is a differential one, its actual supply volt can be adjustable. Because, the DAC we need to also get a bipolar signal so; that means, the supply rail should also be bipolar. And, we should be able to adjust the DAC output so, that you can amplify the signal. So, these possibilities are there, adjustable gain. So, this driver we are using for our hardware.

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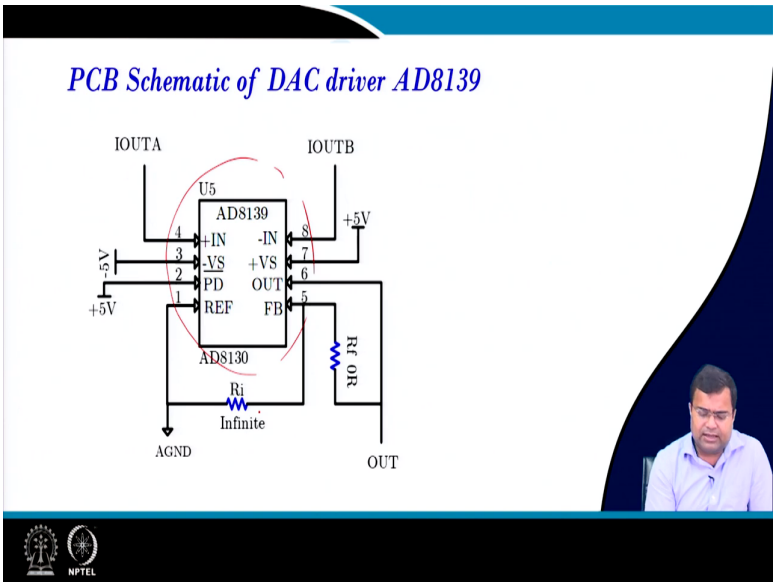

And, if you are the PCB schematic, this driver circuit we are using and then we are amplifying the signal. And, these details are used for our schematic design.

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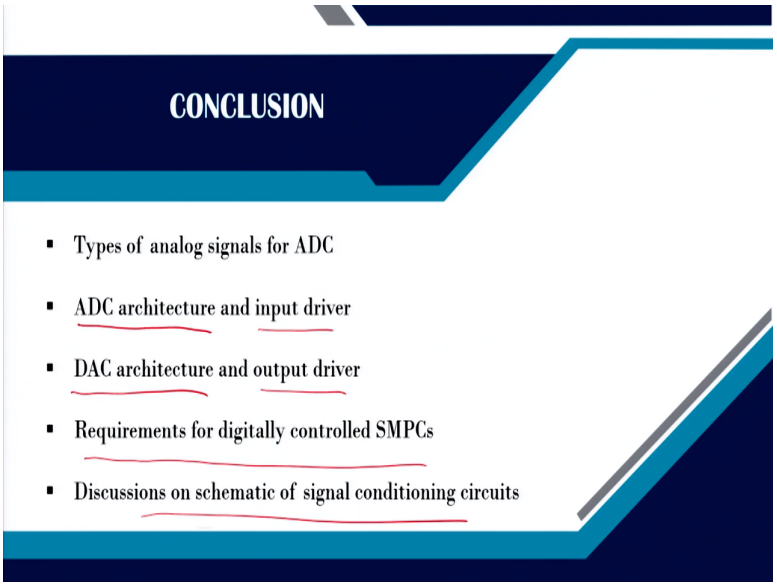

So, in summary, we have discussed various types of an analog signals for ADC. We have discussed various architectures of ADC and input driver requirements. ADC architecture that we have used for our you know hardware setup, that we have discussed and along with the input driver. We have also discussed the driver DAC architecture that we have used and the

output driver. And, we have also discussed the requirement of the digitally controlled converter, then we have to be careful about what is the bit size of the ADC, DAC.

And, we will discuss some aspects when we will talk about when we will discuss hardware demonstration. And, we have discussed some aspects of the schematic for the signal conditioning circuits. And, we will be demonstrating hardware in more detail when the actual prototype and the demonstration will come, that is it for today.

Thank you very much.