Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 06
Digital Control Implementation and FPGA-based Prototyping
Lecture - 51
Selection of ADC and DAC in Digitally Controlled SMPCs

Welcome. In this lecture, we are going to talk about the Selection of Analog to Digital Converters as well as Digital Analog Converters in Digitally Controlled Switch Mode Power Converters.

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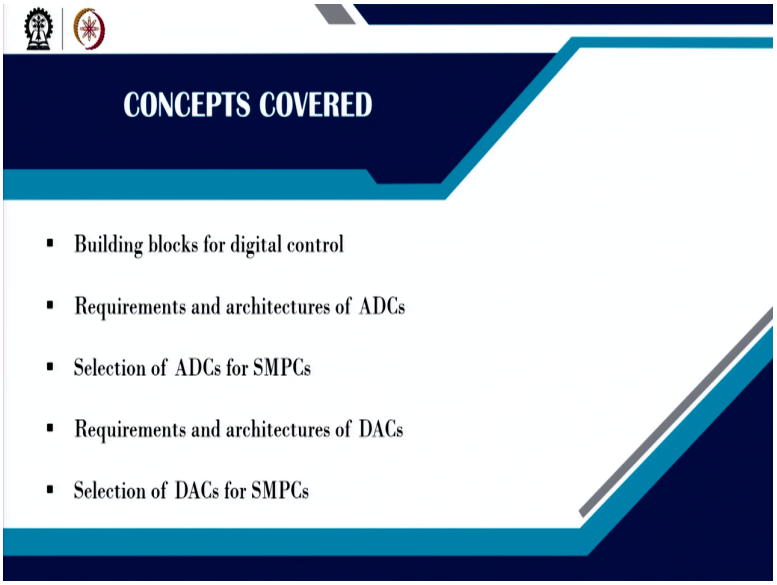

So, here we will first talk about some building blocks for digital control, then what are the requirements and architecture of ADC. Then, the selection of ADC and the requirement and architecture of DAC. And finally, the selection of DAC for the switch mode power converter.

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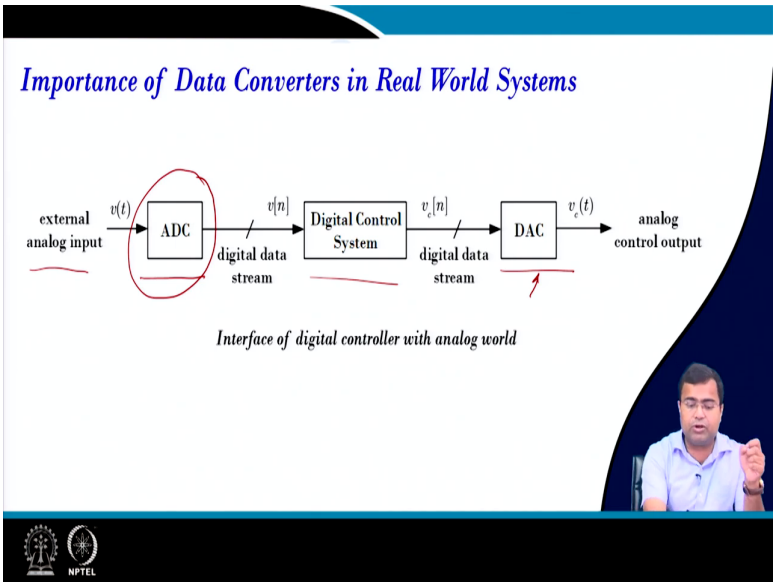

So, this is what you know if you want to consider a digitally controlled system whether is a power converter or any other converter. So, we need to consider an analog signal, then it has to pass through an A-to-D converter. Then, the digital data come, then the digital control system, the implementation platform, and then whatever signal comes out, it has there will be a D to A converter and it goes to analog.

But, not all applications may need analog output in the like this form. Like in a power converter, we may need just the gate signal which is like a digital. So, you do not need an analog. But, in some architecture in our switch mode power converter, we will find that DAC may be needed. Now, there are a few aspects I want to highlight. First of all, in this power converter point of view, if you consider an ADC; we have to first consider whether this ADC will have a parallel interface or the serial interface.

Then, whether what is the data format of the ADC, whether it is a 2 s complement or you know offset binary right? Then, when you talk about analog, how are you know the resolution of how much resolution can be achievable? What is the analog span? What is the propagation delay right? So, all this actually how much sampling rate it can handle? What is the power consumption of the ADC? All this will come into the picture when you talk about power converters.

Then, we discussed a lot about the digital control platform and we will be discussing more this. Then, in some cases, we may need DAC. So, then we have to consider what is how many bit of the DAC is needed. How many bit of the ADC is needed?

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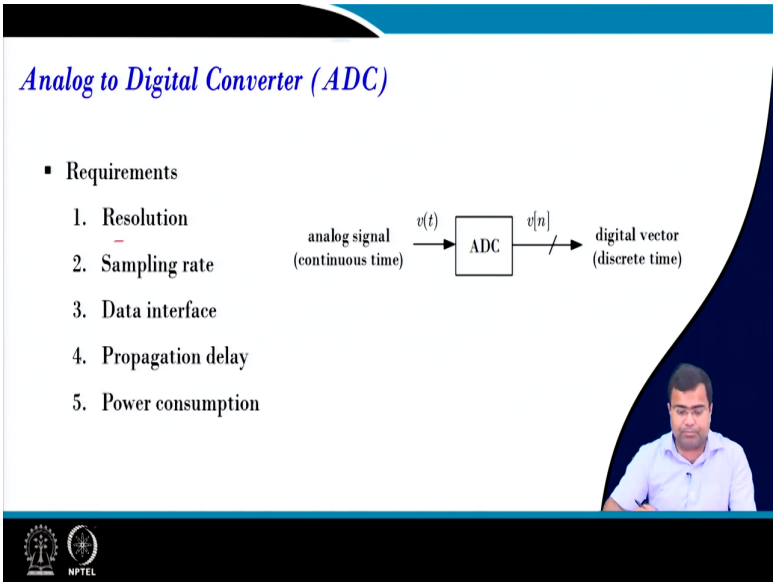

So, if we talk about the analog-digital converter, the data are generally vector, but we can have an interface in terms of serial interface or parallel interface. But, the requirement of this, the resolution of the ADC should be sufficient; so, that it meets certain requirements. For example, in the power converter, we will see in the subsequent lecture, that ADC resolution also you know decides whether there can be the possibility of the existence of a limit cycle or not.

If you do not take that into account, then you may end up with some non-linear like or instability so; that means, the resolution is very important. Another aspect is the resolution; if you do not take high resolution then you may end up with; this means, your voltage resolution may not be sufficient. Because you need to meet a certain voltage because, we are talking about the voltage regulator, and the voltage resolution is also important.

But, too high resolution can cause you to know it will penalize in terms of the size of the DC, their power loss, then the size of the digital controller like big data size. It may also affect the, it may end up with a limit cycle so, we see this. The sampling rate is important I told. The data interface whether it is a 2 s complement or the offset binary, again whether it is a serial interface or the parallel interface, propagation delay, power consumption.

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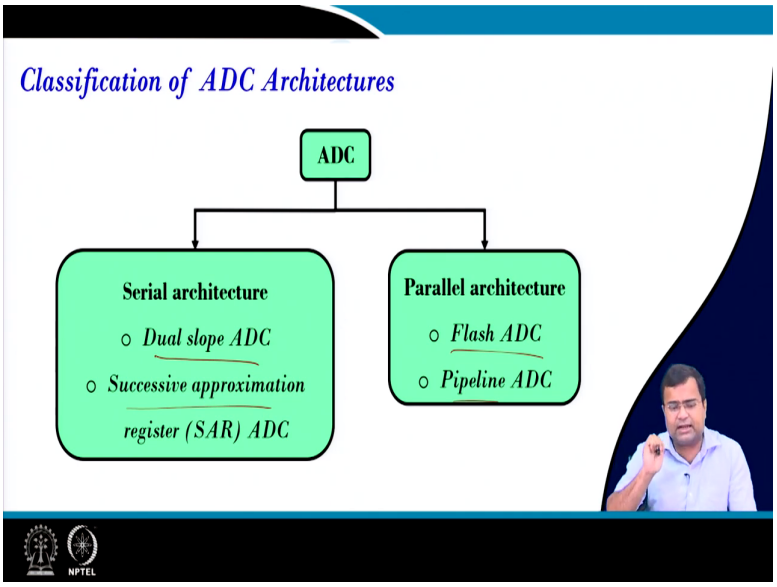

So, the ADC can be classified into two categories. One is a serial architecture, and another is in parallel. And, we are taking some you know I would say some well-known architecture like a dual-slope ADC, successive approximately ADC. Under parallel flash ADC and pipeline ADC. We have not considered here a sigma, delta ADC, like you know that is also popular architecture, but it is just for the basic understanding of ADC.

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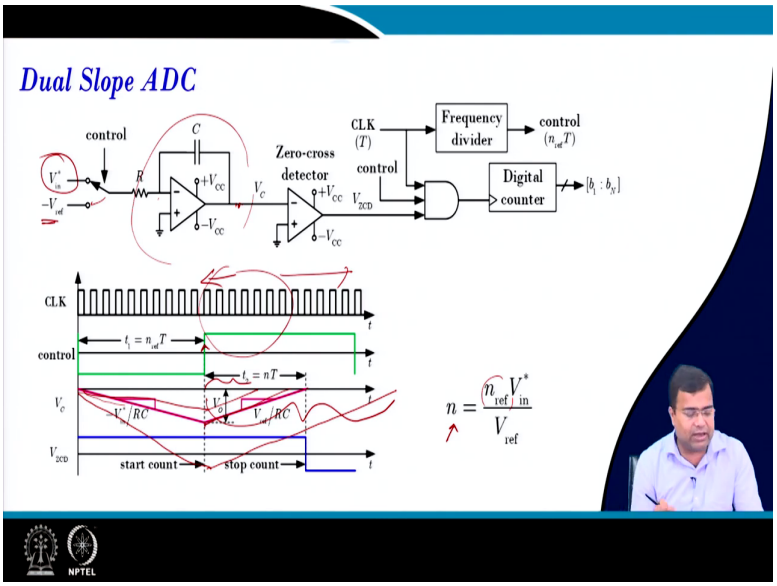

So, in dual slope ADC, if we consider you know what is the strategy? We have an input voltage that needs to be sampled. So, initially, this input voltage is connected and you know

then it passes through an RC circuit, where the because since it is connected in the inverted terminal. So, the output will be inverted. So, it will slowly decrease because RC time is constant; that means, it is just like you know RC time; that means, it will slowly if you take them since it is negative, it is slowly decreasing with a slope of minus V in by RC.

Now, once actually; that means, we allow this voltage and it depends on the timer clock. When the clock comes, then we simply disconnect and connect this V in. And, when this clock comes then it connects to minus V ref and this side will be plus V ref. So, we will have a positive slope, the voltage will rise that V C voltage. And, if the voltage rises and when it becomes the earlier voltage; that means before the input voltage was connected or it becomes 0.

Then, that is the time it converts into an equivalent digital number; that means, the conversion here; that means, number of depending on the number of the cycle, this clock cycle. And, then n into V ref sorry V in by V ref, that will give you the digital number; that means, how many clock cycles it takes. That means, if you have a higher input voltage, it will go down and this rising slope is common; so, it will take a longer duration.

As a result, you can see this is the duration that will give you the number corresponding to the digital value. That means, if the input voltage is large, this number will increase, the number of cycles will increase and as a result equivalent digital number will be higher. If the input voltage is smaller, then it will end up here; then it will take it and go slowly. So that means, it will take fewer cycles to r cycle 0 states. So, in that way, we can convert it into a digital number.

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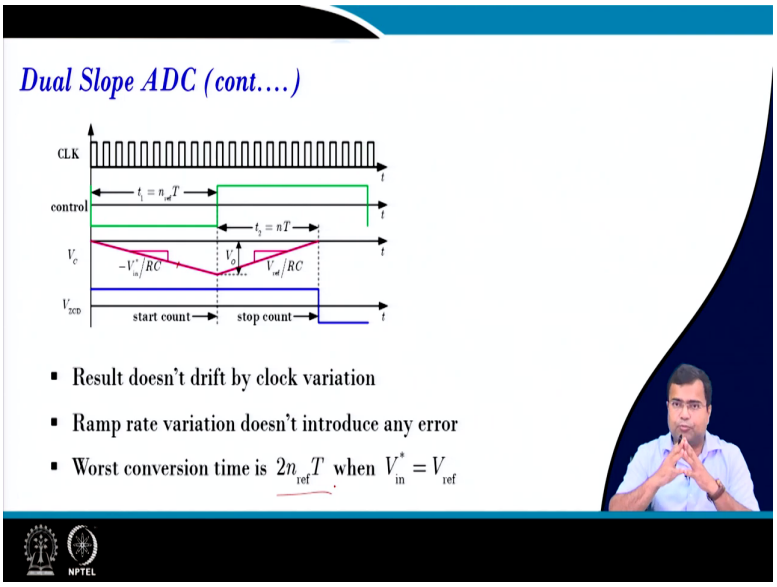

Here the advantage is that if there is some drift in the clock, it will not drastically affect the resolution result. And, the ramp rate variation does not introduce any error; that means if you have some variation in the ramp rate because it is ultimately mapping between V in and V ref. So, that means, the RC time constant will not drastically affect it. So, it is like you know it is just a number that we have to map.

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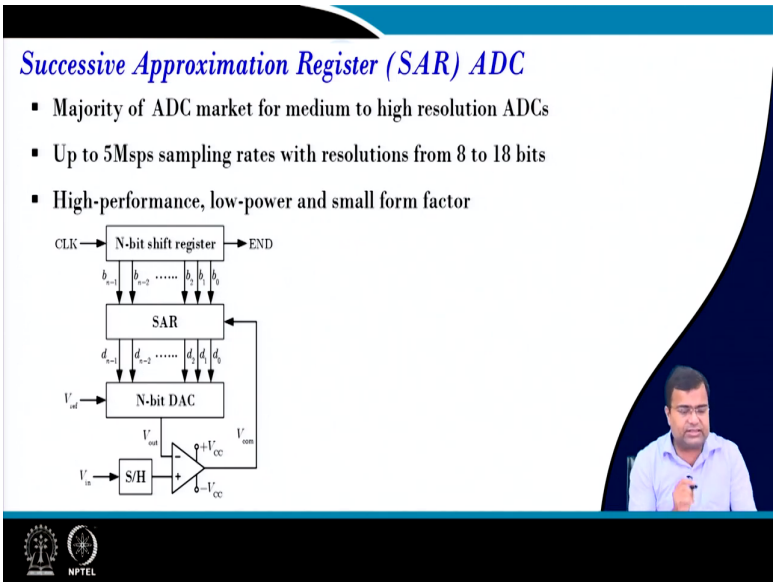

Now, another architecture is a successive approximation, where we know that the majority of the ADC you know for medium to high-resolution ADC when the sampling rate is up to 5

mega samples and the resolution can be 8 to 18 bit. So, these are primarily dominated by successive approximation registers and these are high performance, low power, and small form factor.

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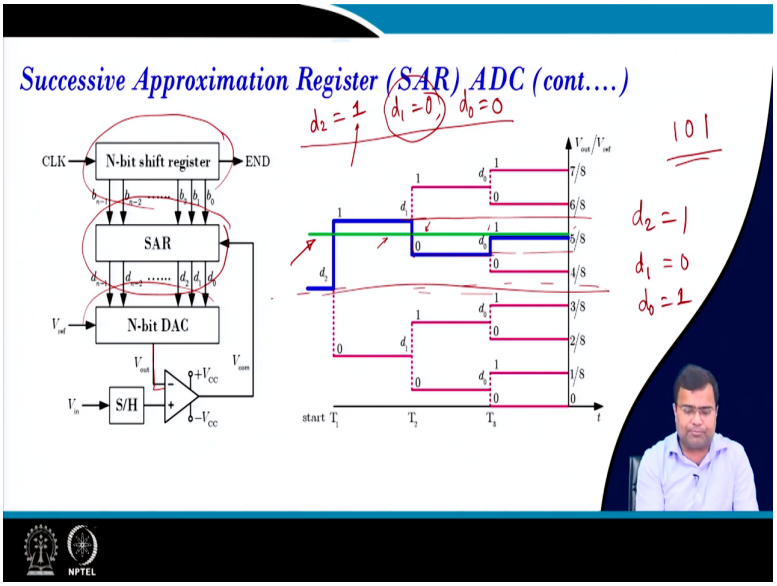

Then, what is the strategy in this successive approximation? It has a shift register and this is the successive approximation logic and there is an N-bit DAC. And, the output DAC voltage is compared with the sample voltage of the input that we want to convert. And, it starts with let us take if we take a 3-bit number which has d 2, d 1, d 0.

So, it starts by setting d 2 equal to 1 which is the starting point, and then d 1 equal to 0 and d 0 equal to 0. So, it starts with this logic. When it starts; that means, this voltage will be set at the mid-voltage. So, this is the mid voltage ok; so, mid voltage. Now, we are talking about an analog voltage which is a green color, that has to be converted into a digital number.

Since this green voltage is above 50 percent of this you know the voltage is coming due to the setting of d 2 equal to 1 1 0 0; that means, the first-bit d 2 will be 1. So that means, whatever d 2 we have taken, will be finalized and it is get locked and then it goes to the next bit.

Then what it does do? So that means, d 2 is set to 1. Since, after that your voltage is still higher, then it has to reduce the next bit; that means, the next bit has to come down because you see this voltage is because this will come for the next 50 percent. So, the next 50 percent

is sitting here. Since it is above below; that means, your analog voltage is below this level, so the next bit is set to 0.

So, next bit; that means, first d 2 will be set to 1 then d 1 will be set to 0, then it goes to the next bit. Again, it takes 50 percent. So, here is the next bit 50 percent is here and your analog voltage is sitting above that. So, as a result, your d 0 will become 1. So that means, you will get 1 0 1 and that number will be the digital value corresponding to the analog signal. So, these logics are well known and pretty straightforward.

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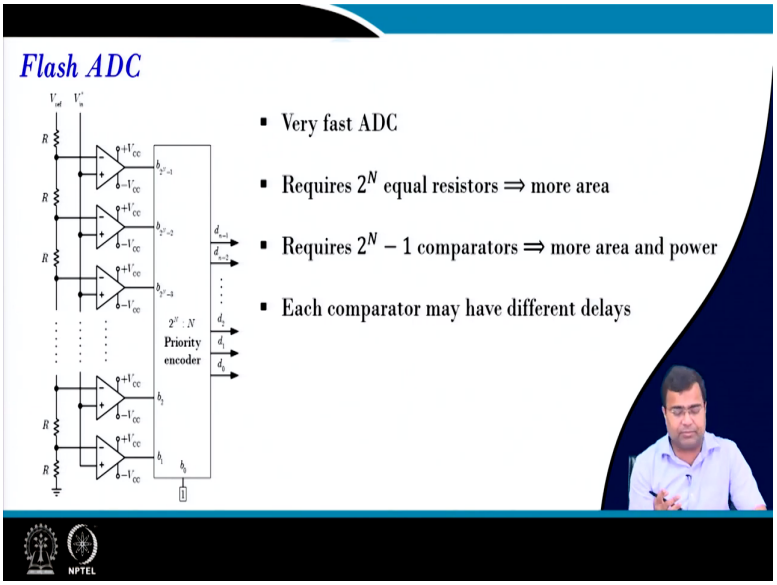

Then, the next is the parallel DC, we are talking about the flash ADC. For the flash ADC, any N-bit flash ADC, we need 2 to the power N minus 1 number of the comparator and you need so many registers and that is why each comparator has a different time delay. So, it may cause some issues.

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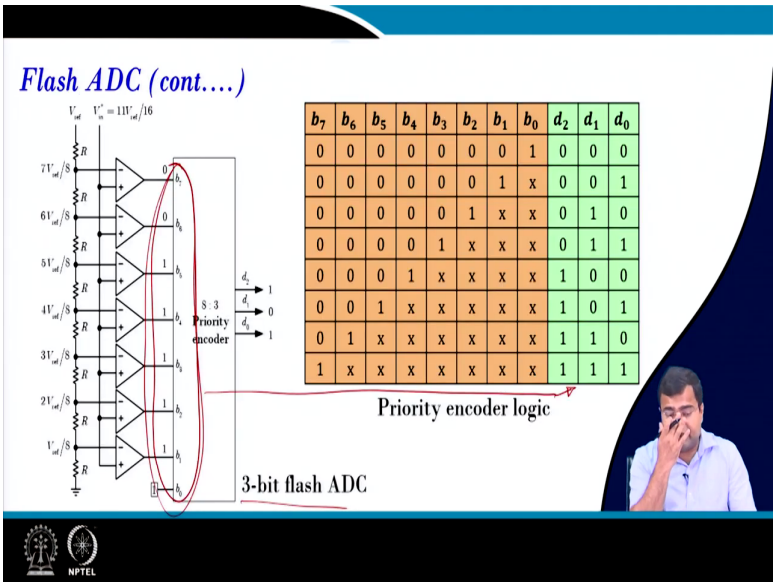

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	d_2	d_1	d_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

So, one of the major difficulties in the flash ADC is because of the huge comparator requirement; we are talking about only 3-bit comparator ADC, flash ADC. But, after all this comparator output, then we need to use an encoder and that priority encoder will convert that into a binary number. So, ultimately we need a binary number depending upon the status of this comparator output.

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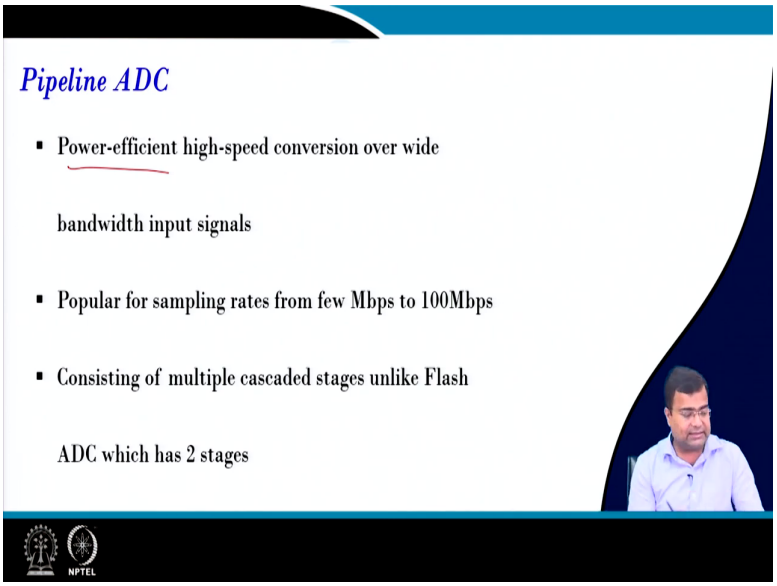

But, one of the major limitations of the flash ADC for 3-bit ADC, you need 7 comparators. What will happen for a 6-bit ADC? So, that comes to the pipeline ADC, where the pipeline

ADC is more power efficient, high-speed conversion and it is very popular for the sampling rate of you know few megabits per second, per sample, then it can be 100 Mbps. Now, the flash pipeline ADC consists of multiple cascaded stages. So, how do you operate?

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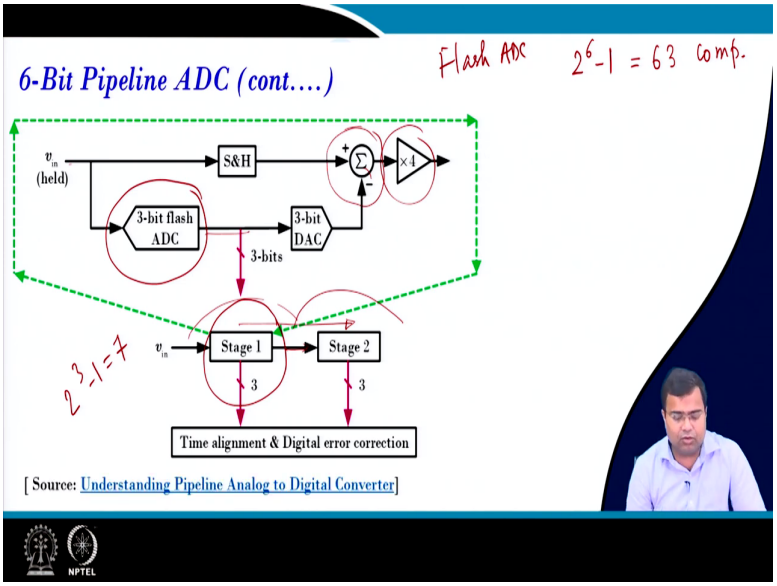

So, we need a 6-bit pipeline ADC. In the case of 6-bit flash ADC; so, how many comparators do we need, for flash ADC? For 6 bits, we need 2 to the power 6 minus 1 which means 2 to the power 3 is 8, 4 is 16, and 5 is 30 to 60. So, 63 comparators is a pretty large number. Now, when you go to flash ADC if you look at the first stage. So, the first stage it uses a 3-bit flash ADC to convert into a.

So, this will set the MSB, then it will pass through a DAC and get the corresponding voltage and then whatever analog voltage you got; since the resolution is poor. So, it will amplify the different signals; that means, after you set the 3-bit DAC, there will be a shortage of resolution problem and that particular error will be amplified. And, that amplification will pass through the next stage. And, again next stage there will be a 3-bit, the same architecture 3 bits flash ADC.

So, for a 6-bit pipeline ADC, you need two 3-bit flash ADC and of course, two 3-bit DAC. So, each flash ADC required 2 to the power 3 minus 1; that means, 7 comparators. So, you need 14 comparators plus DAC, DACs are much simpler and we will go to the architecture of DAC. So, in that way you can achieve a 6-bit resolution. And, since it works on a similar

principle to flash ADC; so, the throughput of pipeline ADC can be made almost close to the flash ADC.

But, the penalty will come in terms of propagation delay because it has to pass through multiple stages. As a result, in the flash ADC the delays are conversion time, you know it is in terms of several stages, and cycles. So, it is not absolute, it depends on the number of cycles and at what rate each stage is operating ok.

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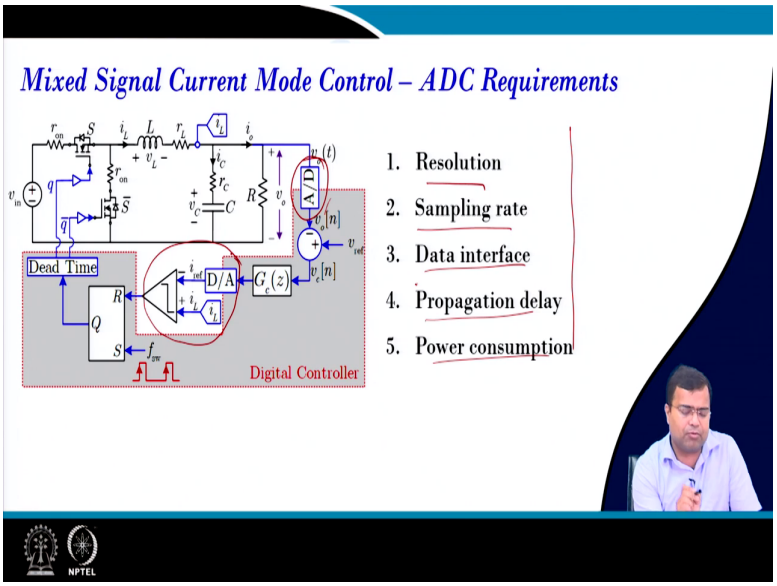

So, that is one of the drawbacks of the pipeline ADC. It has a high throughput, but the propagation delay is high and large. So, now in the case of a DC-DC converter, if you take a mixed signal current mode control; we are talking about this ADC. So, you have to meet certain resolution requirements, sampling requirements, what is the data interface that will come to the digital controller, propagation delay, and power consumption.

And, we will be talking about a practical case study when we go to hardware, we will talk about what we have considered. But, these are the important aspect that we should keep in mind.

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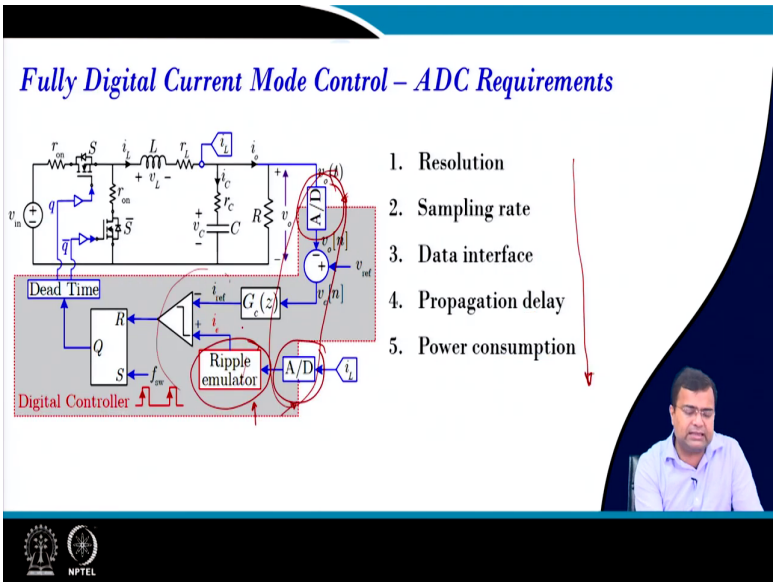

Next, if you go to fully digital current mode control, apart from this ADC for the output voltage we also need an ADC for the inductor current. And, typically if we take 1 cycle if we take one sample of the current per cycle and one sample of the output voltage per cycle. So, we can merge these 2 ADC like a pipeline ADC. So, that 1 ADC is enough, we can do a time multiplexing.

But, since we are taking one sample, we need to emulate the current ripple just inside the ramp. And, that we have discussed in multiple architectures, multiple lectures what is the architecture of fully digital current mode. But, here in this architecture, the selection of ADC is very critical because the propagation delay has to manage.

Then, you know the resolution of the current and voltage both have to be maintained and it should be in such a way, we should avoid any limit cycle oscillation ok. So, this architecture can get rid of the analog comparator as well as the DAC which was there here, because here we need an analog comparator as well as a DAC. But, here you can eliminate it so, we can make the inside digital architecture much faster.

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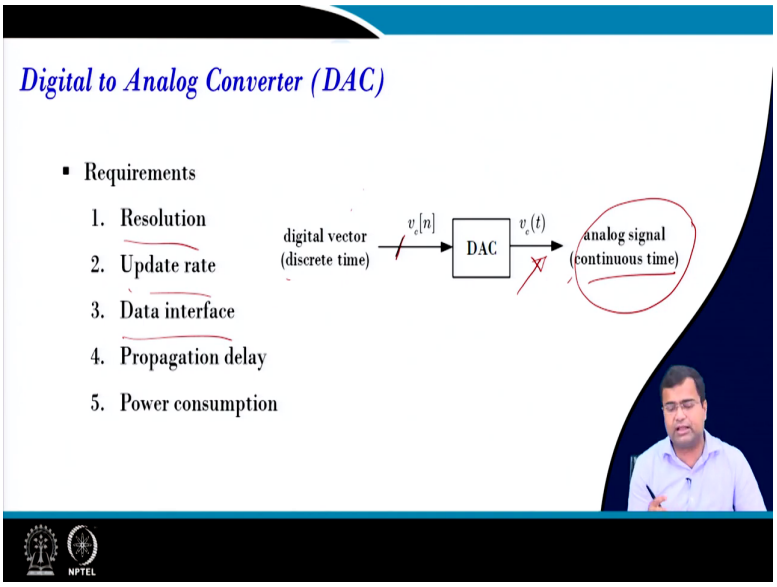

If you come to D to A converter; that means, we need a digital data analog. So, we need to know whether the digital data is a 2 s complement or offset binary. Then, the analog signal will be the actual range of the voltage. Sometimes, we need to amplify the analog voltage, but you cannot straight away use a simple amplifier. So, the DAC should come with the DAC driver at the output stage. And, we will be discussing this in the subsequent lecture.

So, here the requirement, the resolution should be sufficient, the update rate should be fast, and the data interface depends on what type of data and what is resolution comes from the digital controller. Sometimes, the DAC resolution needs a high resolution to avoid any limit cycle. So, propagation is also important and power conservation is also important. Because, if you are talking about the integrated circuit these things will all go inside the IC.

So, you have a data converters controller, as well as you know if you are talking about the control you know digital control IC, let's say for multi-phase application. Then, we have a centralized digital control algorithm; that means, there is a core, a digital control core. So, you have to be very careful about the power consumption of the data converter. So, that it cannot it should not be very high compared to the other losses of the converter, because you need to achieve high efficiency.

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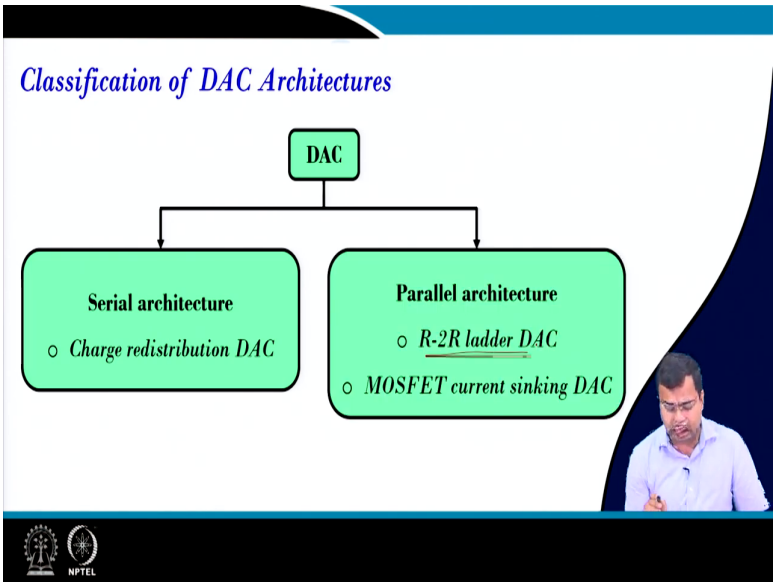

Now, the DAC can be classified as serial architecture using charged redistribution and parallel architecture.

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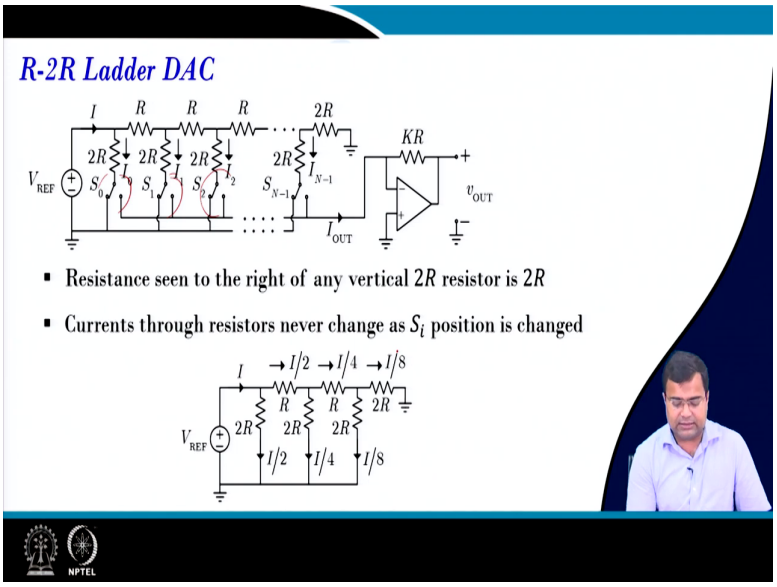

And, we are only will touch upon the R 2R ladder which is a very popular solution. And, this architecture is well known where we connect R and 2R combinations just by drag and drop and there are multiple switches. And, this switch status will decide your actual conversion between digital signal to analog. And, it requires R 2R and R, you know the right side of any

vertical 2R will look like a 2R resistance equivalent. So, the current through the register never changes, and then this is the particular case study.

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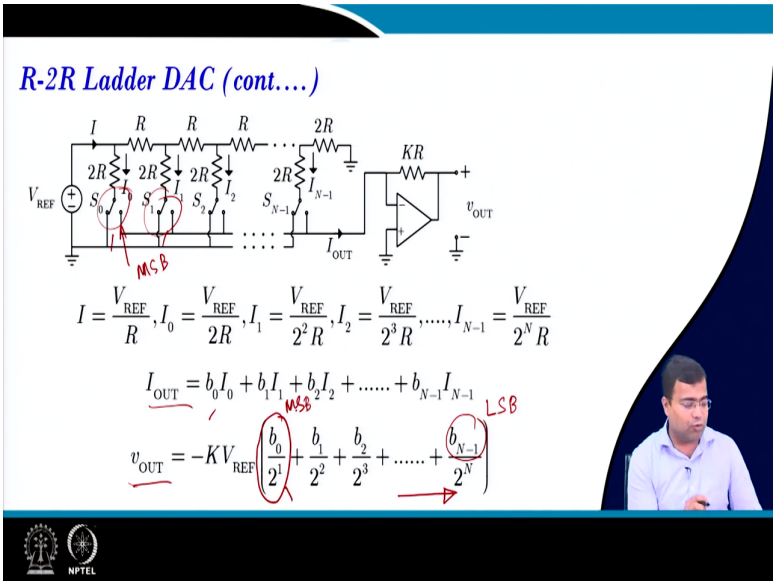

So, in the R 2R ladder network, if we take in terms of current; the output current will be a function of you know this bit position; that means, what is the bit position? Bit 0, bit 1. So, starting from bit 0, bit 1, bit 2, and then accordingly these numbers are scaled ok. So, we are talking about whether it is LSB or MSB.

Then, it converts into output voltage; that means, depending upon that, we need to convert it into an output voltage. So, I think this should be MSB because this has the maximum effect. So, I am sorry, the b 0 here is the MSB because this has the highest effect on the voltage change. And, as you go towards the right side, this bit has so, this is like an LSB and this is the MSB of the digital data which can affect the output voltage drastically.

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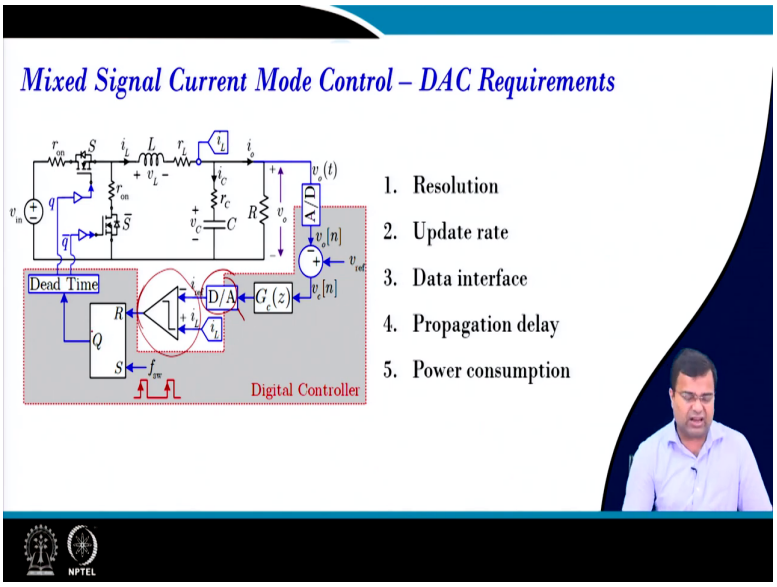

Now, in the case of mixed signal, we need this DAC because this DAC has to convert the digital current difference into an equivalent analog current difference. Then, it will be compared directly with the analog control with the sensed inductor current and then the output will go to the (Refer Time: 18:03) circuit.

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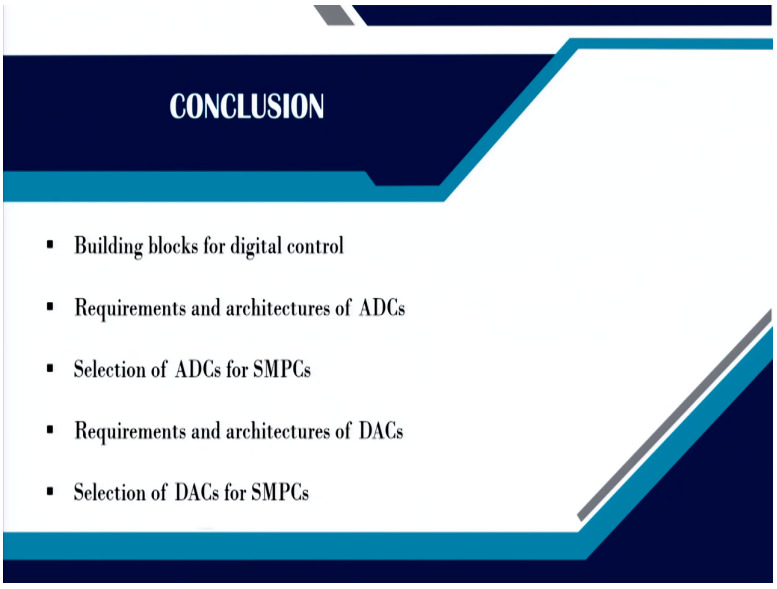

So, in summary, we have discussed the building block for digital control. We have discussed the requirement and architecture of the ADCs. We have discussed selections of ADC as well as the requirement of DAC and some aspects of selections of D to A converters or switch

mode power converters. But, not all SMPCs require digital control required DAC, maybe few are selected. But, ADC is mostly required by the majority of the digital control architecture.

So, you need to be careful about the architecture of the DC, particularly when you are going for an integrated solution and their resolution as well as the sampling rate. And, we will be discussing some analytical, theoretical aspects, how they can affect stability as well as their voltage resolution along with the hardware history. That is it for today.

Thank you very much.