Digital Control in Switched Mode Power Converters and FPGA-based Prototyping

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Module - 05
Frequency and Time Domain Digital Control Design Approaches
Lecture - 50
Digital Pulse Skipping Control and MATLAB Simulation Case Studies

Welcome, in this lecture, we are going to talk about Digital Pulse Skipping Control and some MATLAB Simulation Case Studies.

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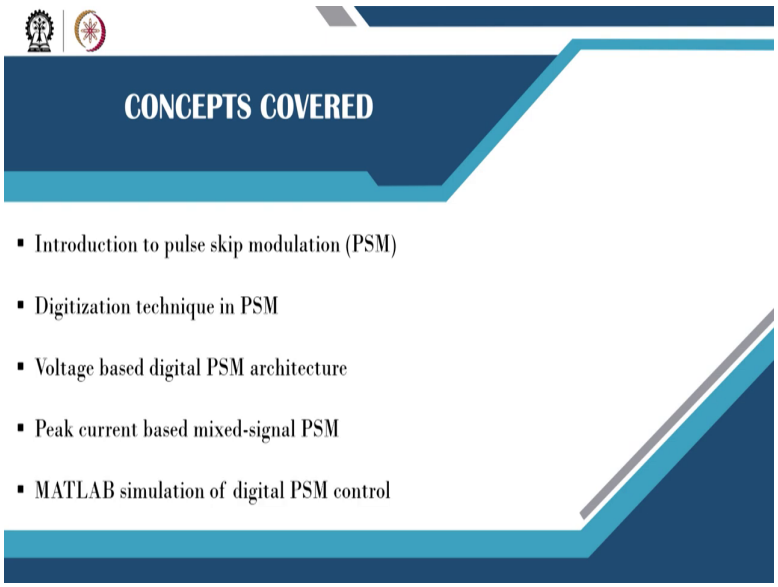

So, in this lecture we will first introduce the pulse skipping modulation, then the digitization technique in pulse skipping, then voltage-based digital pulse skipping architecture, peak current-based mixed signal pulse skipping control, and MATLAB simulation.

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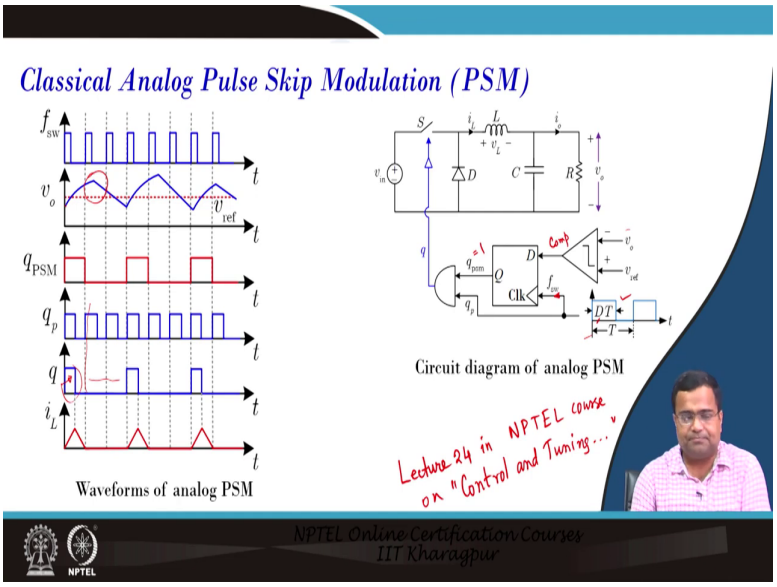

So, here is the classical analog pulse skipping modulation, this is the diagram. So, in this diagram, you see what we have discussed in lecture number I think 24, lecture 24, in our NPTEL; that means, control and tuning method. This is in the NPTEL course. So, this we have discussed in pulse skipping control. So, here you know, so for detail, one can refer there.

So, how does it work? So first, there is a D flip flop; at every rising edge of the switching clock, it checks whether the output voltage is higher than v ref or lower than v ref. If the output voltage is smaller than v 0, then this output will be 1, this component of output will be 1 and that will pass D will be reflected q, q will be high q PSM will be high and it will simply pass the same clock here.

That means if the output voltage is smaller than v 0; that means, it understands that you need to boost some energy and inject some energy, then it goes to a high pulse and that it takes the duty ratio of the clock, which is here q and that q P and that is the charge pulse and throughout the cycle, it will take this duty ratio. Once it goes above, then it will skip the pulse and at that time whatever you can see in this cycle, the voltage is higher.

So, this cycle is skipped. This cycle is it is higher, it will also. So, in two subsequent cycles, it skips. During the charge pulse, the signal q, in this case, we are taking a fixed duty ratio; that is reflected in the control. So, it means, during charge pulse, it is like a PWM control, in this case with a fixed duty ratio and during other times, if the output ratio is higher than v ref, it will simply skip the cycle.

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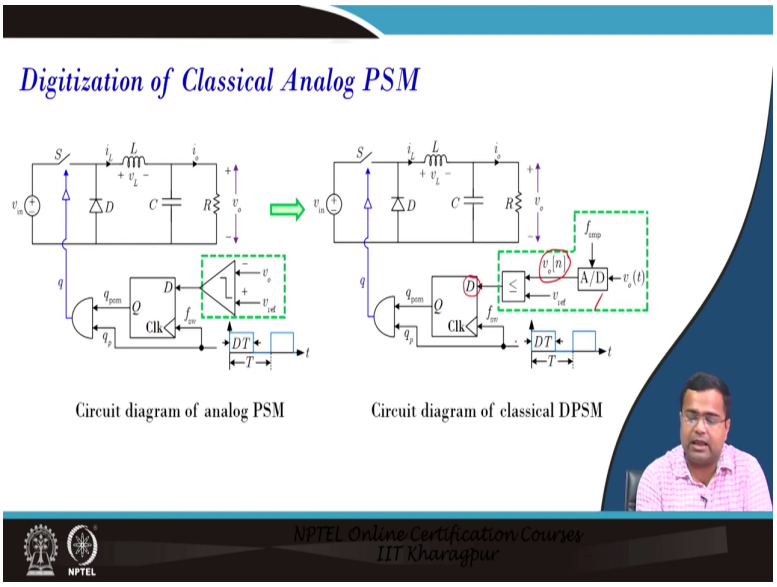

Now, if you want to digitize, what we will do? This block comparator will digitize. And instead of using an analog comparator, we can simply use A to D converter, suppose we are incorporating this PSM logic, into an existing DPWM logic. It is very simple, we will take the advantage of the ADC, take the sample there, and the sampling clock, will take some as the switching clock. So, every it is the same rate, but the instant will be different, and the sample voltage will be compared with v ref. Because it is fixed throughout the clock cycle.

And if it is smaller than v ref; that means, we need to inject charge this D become high and it will pass the duty ratio. So, we are digitizing this block and this is a digital part.

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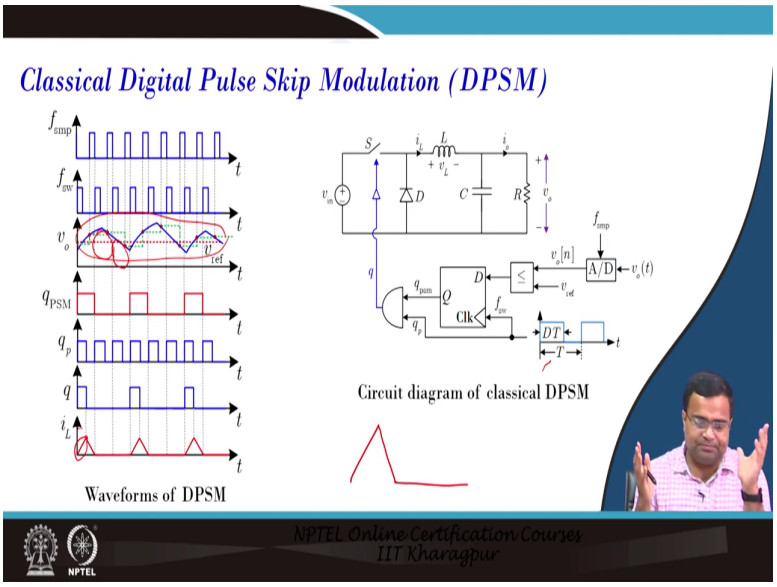

So, what does it do? That means, we are taking samples and as I said, the sampling clock and the switching clock frequency that is the same. But their edges are different. So, the sample will be captured first, before the switching clock start. That is why this sample will be held and this will check whether this voltage is beyond the above v ref.

So, in this case above. So, this cycle, this particular cycle we skip; this is also above, this cycle will be skipped, these two cycles are skipped. Then if you come, it is below it will be reflected here. So, that will undergo a charge pulse. So, here the difference is, we are only digitizing this loop. What will be the advantage? Because we are assuming the controller itself has a digital, we simply take the sample and we will decide whether it will pass or not.

Once it goes, then we can use a fixed clock duty ratio, but what is the problem during charge pulse; that means, it is giving a DCM, it is under light load. So, there is a skip cycle. So, now, the on-time of this clock will be decided by this duty ratio. How to take the duty ratio? Whether should it take a large value, or a small value, and based on that, the amount of energy will be injected. If you take a large duty ratio, if the input voltage increases, then the ripple current can be much larger and it may violate the ripple constant of the output voltage.

So, this ripple can violate the limit and that may not be accepted. If you take a two lower duty ratio, then you may encounter more frequent charge pulses with a very less number of skip cycles and that may not be productive because you are burning unnecessary power. After all, too many switching will happen. So, we need to get some better control over the duty ratio.

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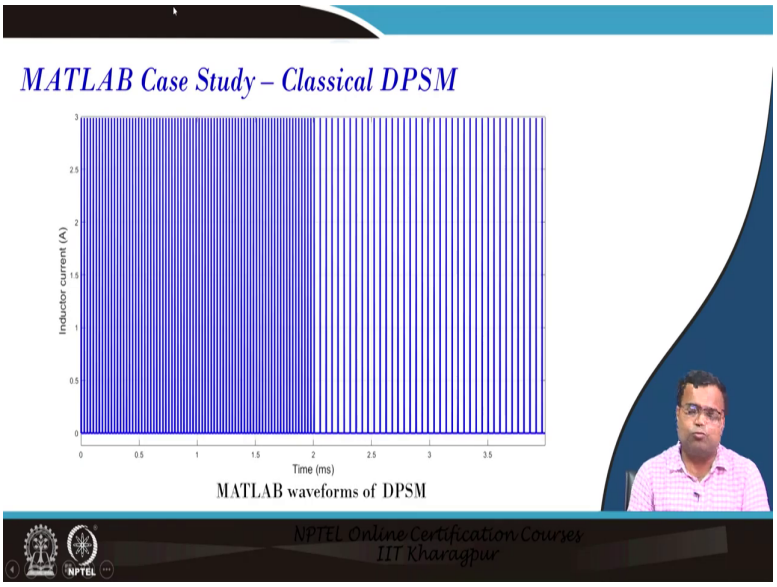

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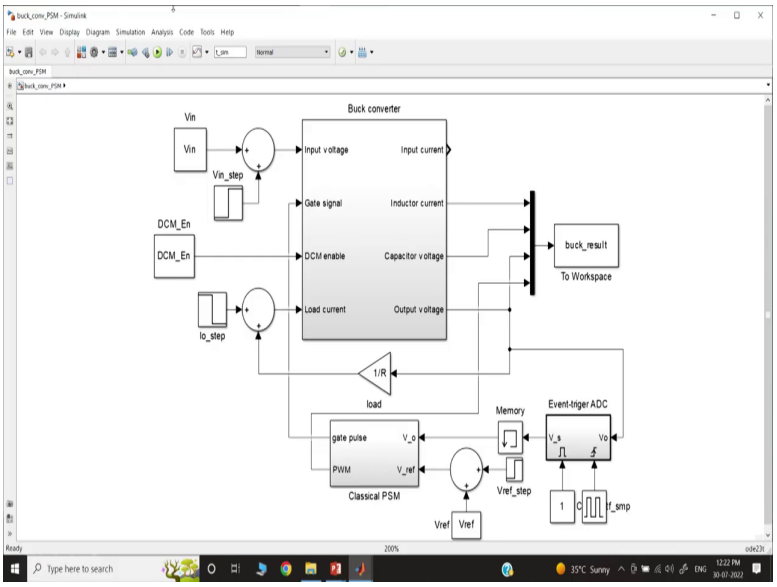

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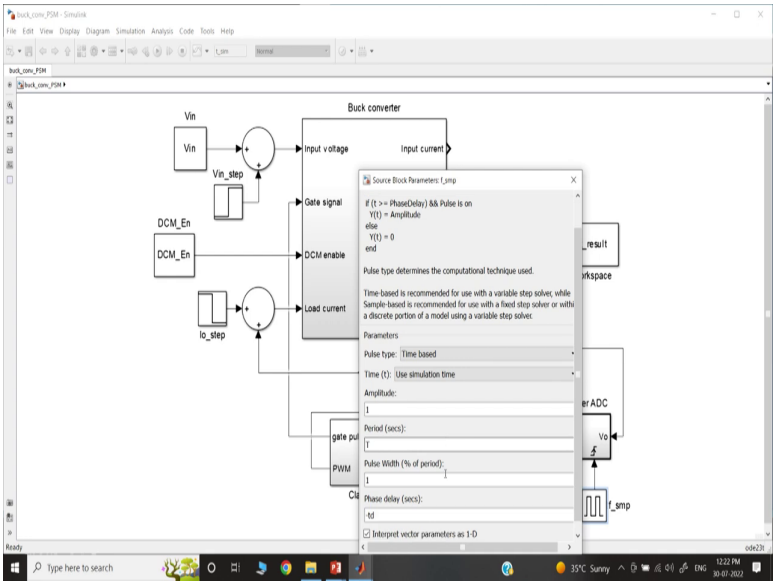

So, here we can do a MATLAB case study I am going to do that ok. So, let us go to the MATLAB case study. So, if we go to MATLAB, this is the classical pulse skipping, you can see that here we are taking the ADC voltage, output voltage sample voltage and we are using a clock with a delay; that means, we are first sampling as if before minus t d is the delay time and then, we are passing through this pulse skipping; that means, there is a reference voltage you can see.

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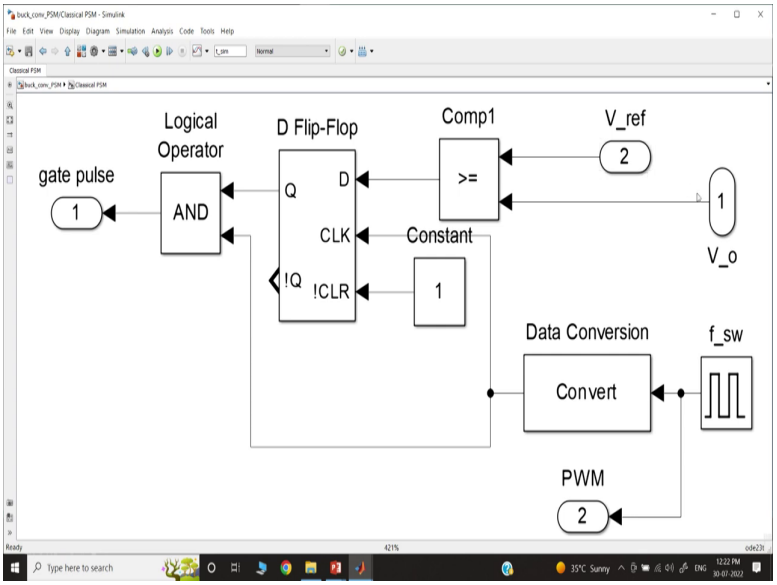

If you go inside it will show that it is smaller than the reference voltage is larger than the output voltage, it will pass to d latch and it will turn on.

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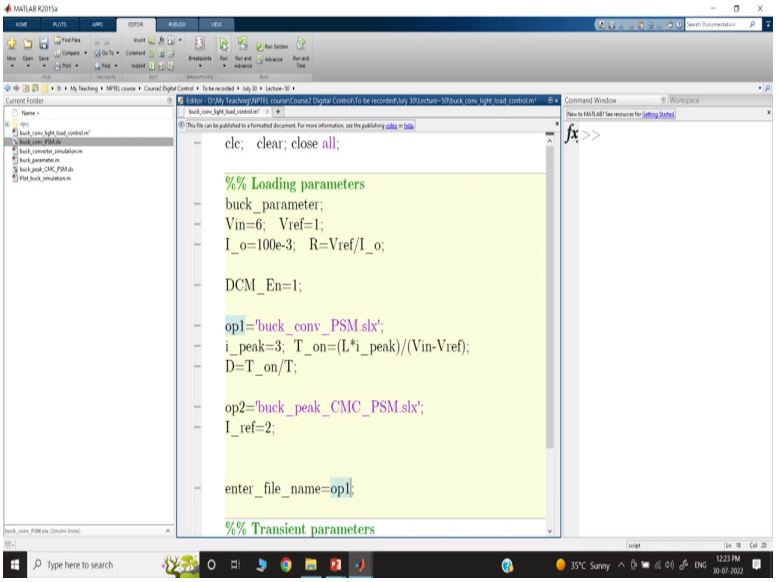

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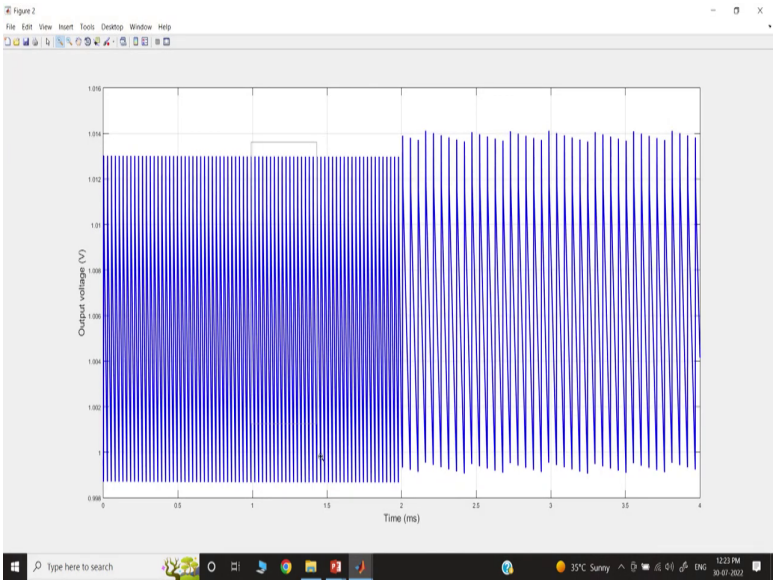

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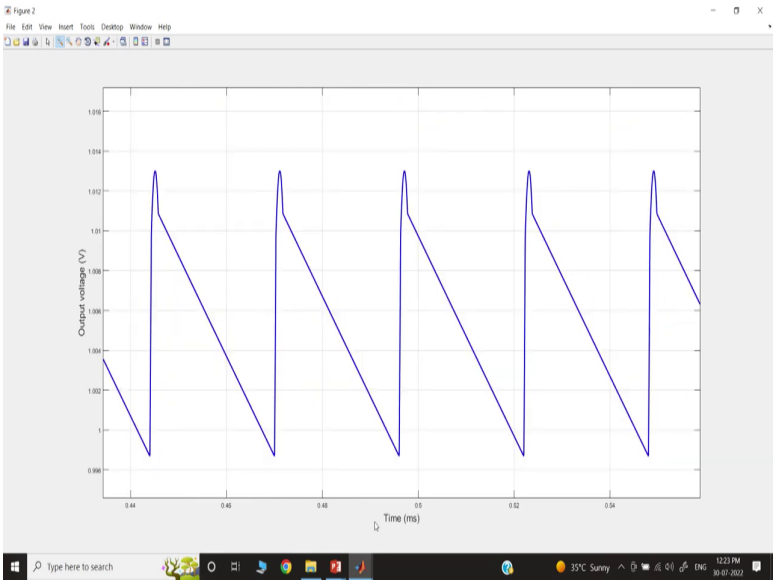

So, if we run this classical pulse skipping so this is our classical pulse skipping. So, in option one, we will run it, then we will see what happened to our (Refer Time: 06:28). So, you can see, there is a load transient additional. So, initially, the load current was a bit high; that means, you can see that we are operating at 500 kilohertz, but if you zoom this portion, you will find that this is the output voltage ripple. So, the best thing will go to the inductor current.

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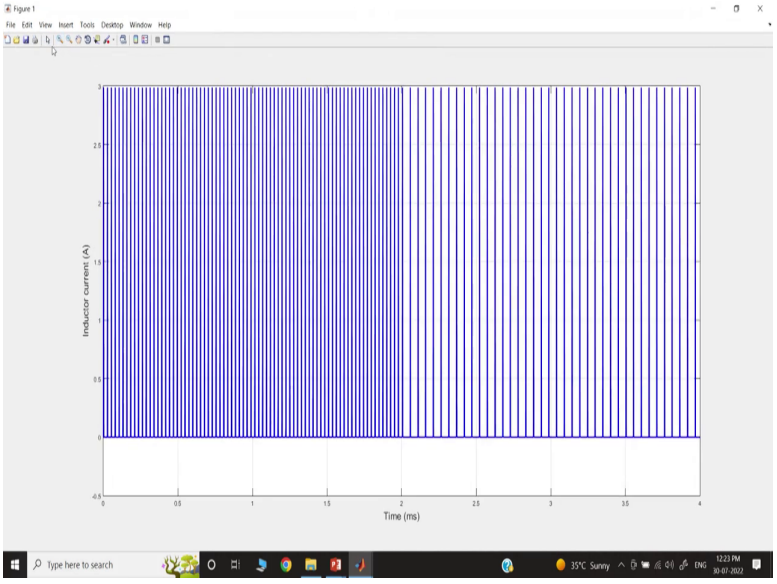

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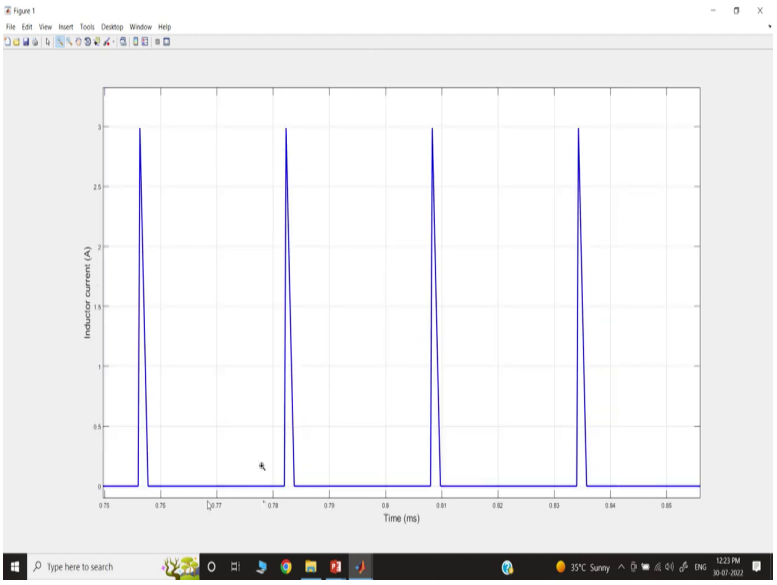

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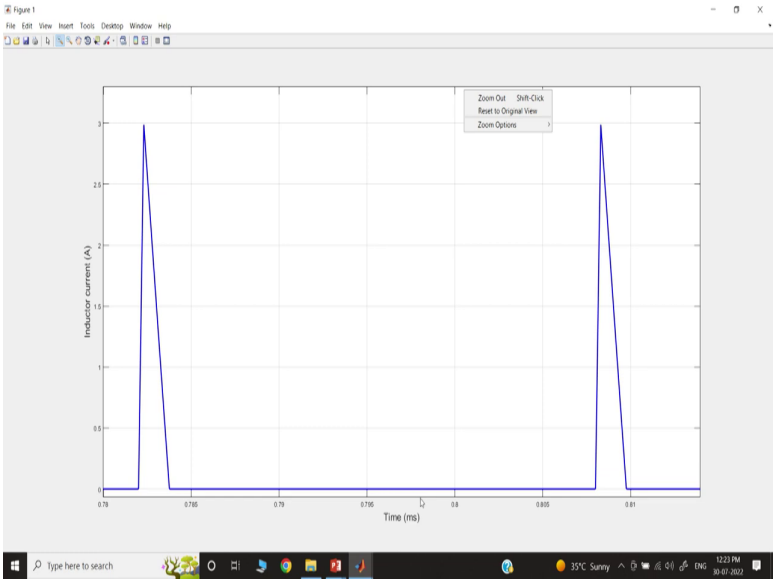

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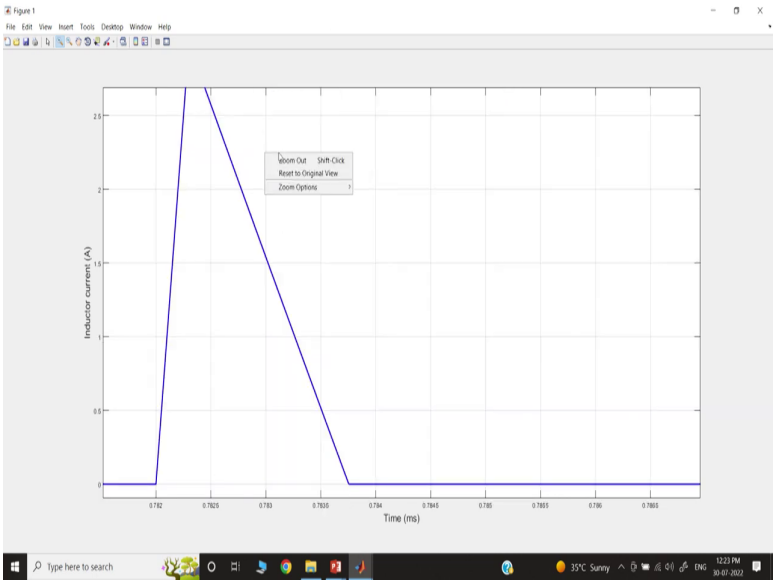

So, here is what we are trying to do if we take one particular instant. So, let us say we are talking about this instant. So, it is in a millisecond; which means, it is not switching in every cycle; that means if you zoom this portion, particular or time period is two; that means, up to this point is a 2 microsecond. So that means, these are charge pulses,s and the remaining this, these are the skip pulse. There are too many skip pulses, it is under light load conditions.

Now, if the load current further decreases the number of skip cycles further increases. So, you can see effectively between the two loads. So, this is a little bit higher load. So, we will go over what is the load current condition. So, before transient, it was 100 milli ampere.

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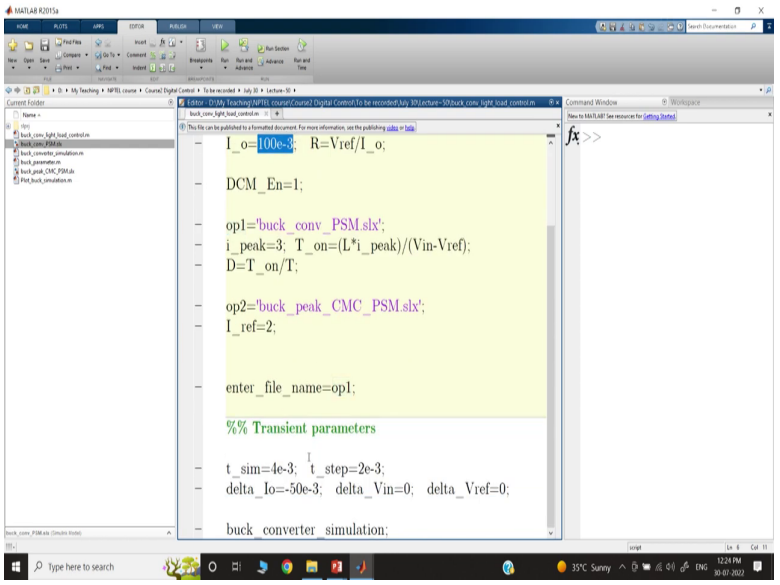

Now, we have applied a minus 50 load step; that means, we are changing from 100 milli ampere to 50 milli ampere. So, naturally, the number of skip cycles should increase and that is reflected in this waveform. And you can see the output voltage ripple, actually more or less remains the same. But what will happen, in this case, suppose instead of load transient, we make a supply transient; that means, we do not make load transient.

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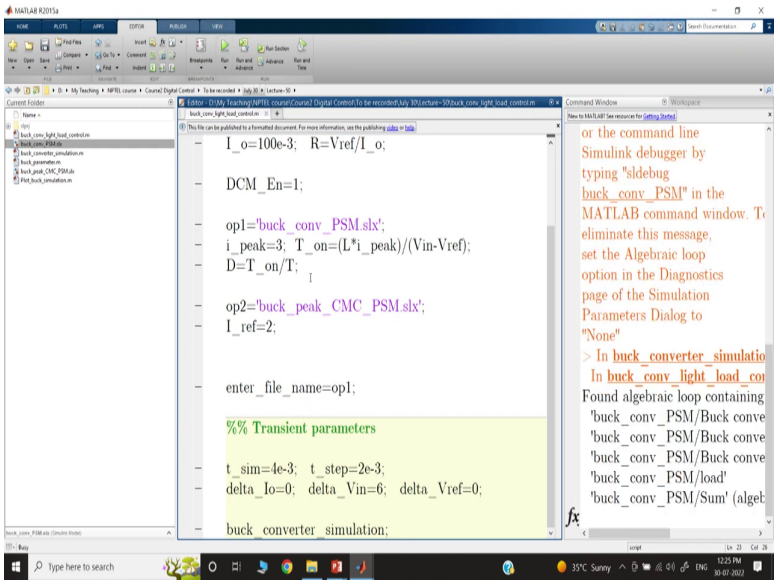

We will change the delta V in. So, it is now, let us say 6 volt. So, you want to make increase the input voltage to another 6 volts. So, 6 volt to 12 volt changes. Now, we want to see the transient.

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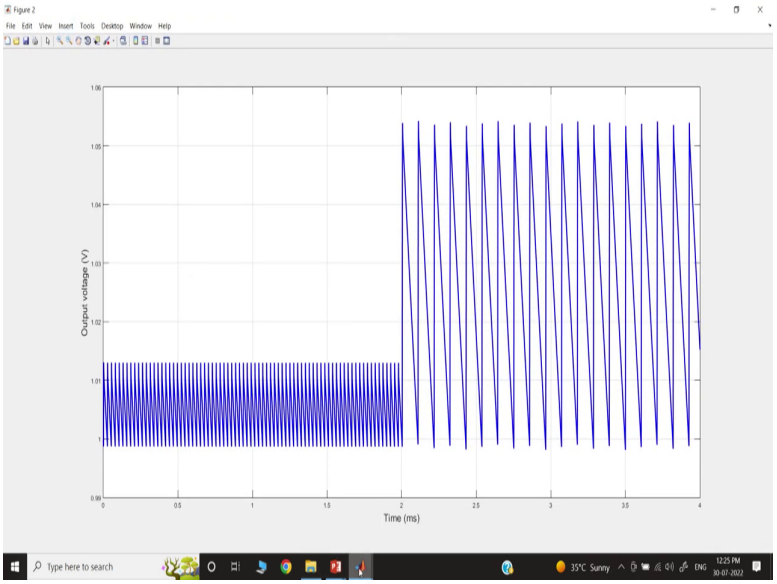

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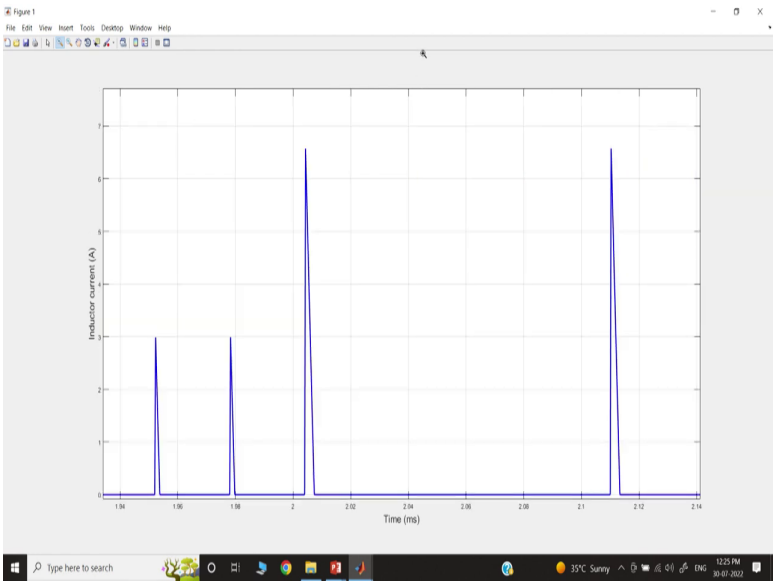

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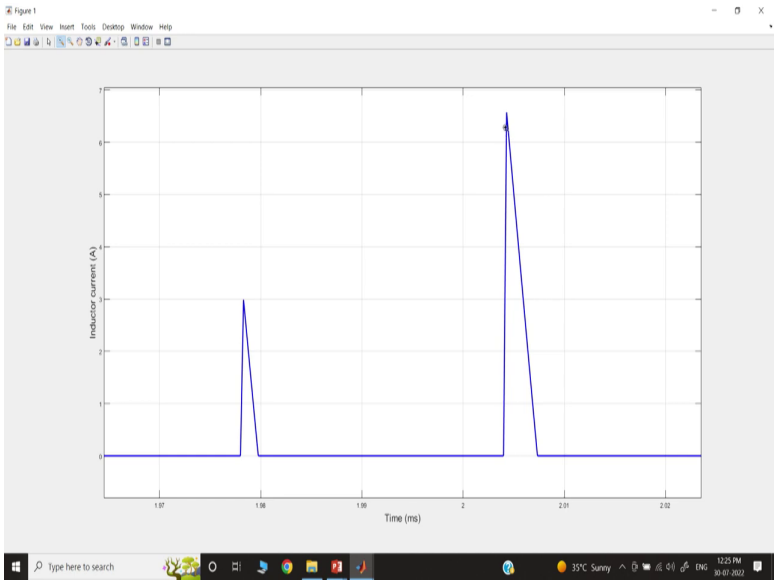

So, you can see, for lower input voltage, the pulse skipping was happening, but for the higher input voltage, since you are using a fixed duty ratio, the on-time during this on-time slope of the inductor current is much faster and as a result, the peak current has increased from 3 ampere to almost 6.5 ampere which is not acceptable because the output voltage ripple is also too large; it is too large. So, it is not acceptable, because it has increased drastically.

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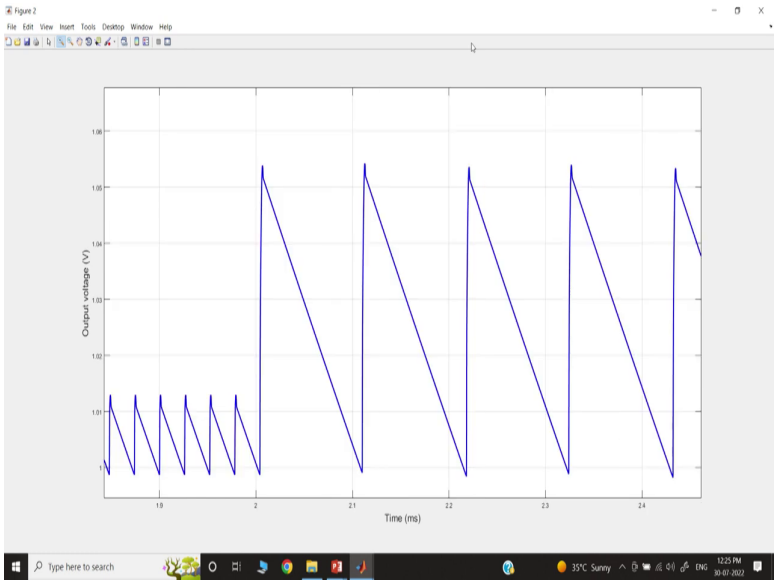

So, how to overcome this problem? So that means, we have discussed the classical pulse skipping.

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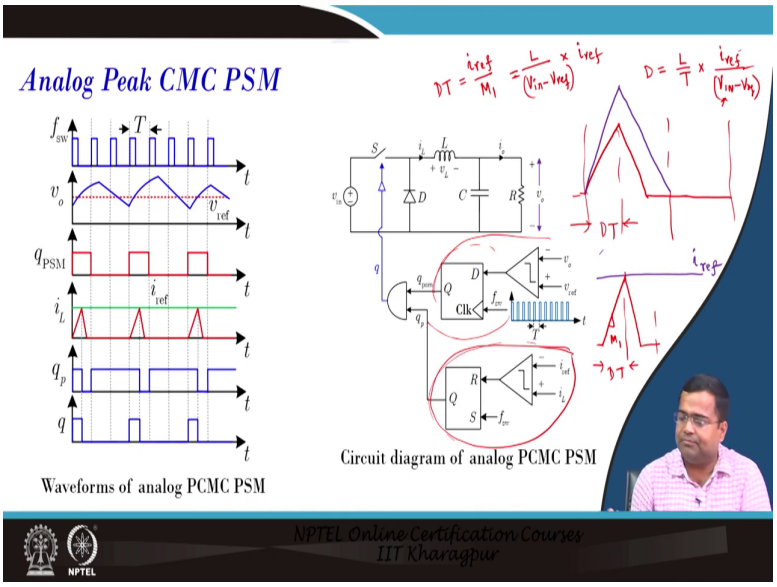

Now, we want to move to the classical pulse skipping we have discussed. So, these are the waveform we have shown. Now, in order to avoid such a large high peak current, we want to limit; that means, ultimately we have to generate the duty ratio which is the charge pulse; that is the bottom line. So, this is a charge pulse, this is a skip pulse, right? So, here during this charging pulse, we have to calculate this duty ratio.

So, earlier we are fixing the duty ratio. Now, suppose the input voltage increases then what will happen? This ref sorry, this will go up. So, if the input voltage increases, then the slope will increase. As a result, you will have a larger current right. So, this will increase so; that means, as the input voltage increases, then your peak current will increase and that will create a huge current you know peak current and that will increase the voltage level.

But, we want to adjust this duty ratio, how do we? So, alternative way, we are fixing the reference current; with a reference current, which is a constant value, and during the charge cycle, the inductor current will simply take that value and come back. So, that means, here in this case, the duty ratio D of T, what is D of T? If the slope is M 1 it is in a steady state; that means, our D of T is nothing but our I ref, that is our fixed value divided by M 1.

So, for the buck converter what is M 1 it is V in minus V 0 by L. So, it will be simply, L divided by V in minus V ref, if it is regulated perfectly, into i ref. And if we want to find out D, then we will take L by T, and T will be coming to this side into I ref by V in minus V ref. So that means, for a given L and T, given reference current, if the input voltage increases the

duty ratio will decrease. As a result, it will automatically adjust. And if we can keep this ripple more or less constant, then we can expect the output voltage ripple will be more or less constant.

So, we want to implement this; that means, now we have an additional current loop; that means, the duty ratio is instead of passing this clock to here, we are passing this clock to here ok, analog. The majority of commercial products, it has a protection circuit; or current protection. So that means, current sensing is there and protection we can utilize to generate the peak current-based PSM; that is also possible.

So, this is the diagram, where the i ref is there and the other logic of pulse skipping remains the same. We are not touching the PSM enable a disabled clock; when to decide charge cycle, when to decide skip cycle; this is decided by the earlier logic, but only during the charge cycle, the duty ratio will be decided by this loop ok.

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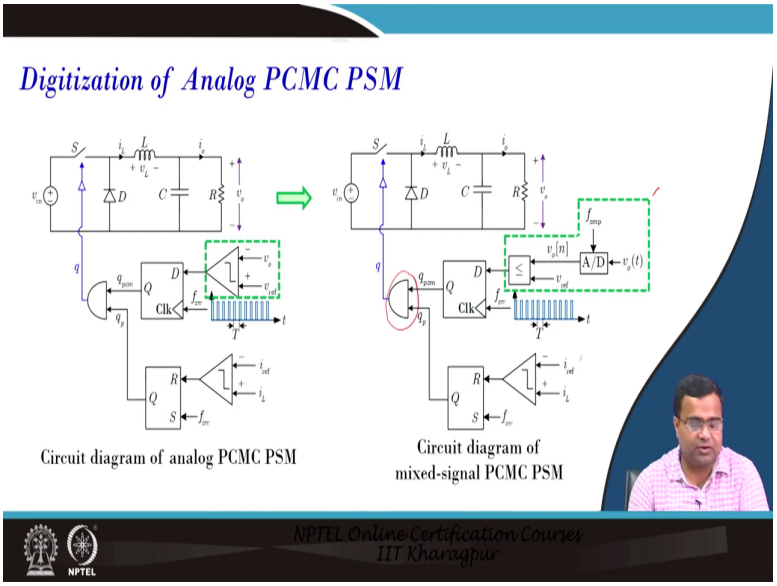

As you can see, this is the i ref, and if you want to do digital control then what will do? Only this block will digitize ok. And this will only it will there be ended with the gate signal coming from the current reference ok.

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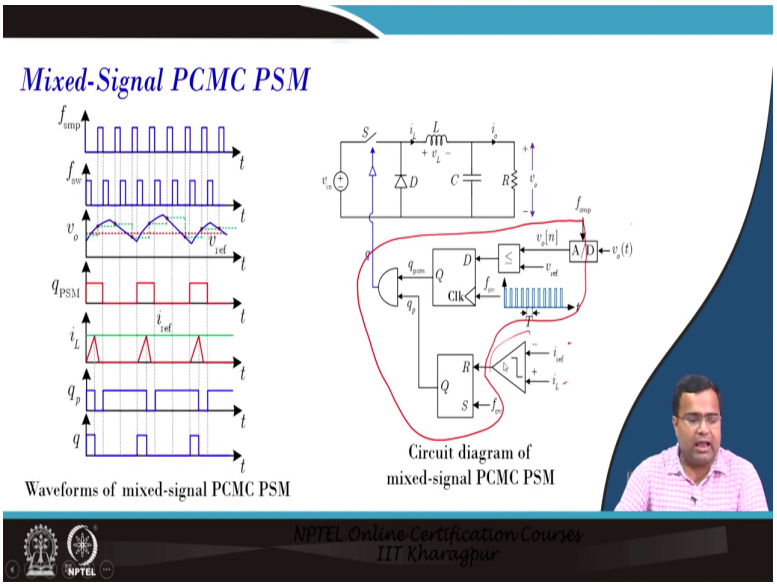

So, in mixed-signal, this is our ADC this part is digital, and everything is digital. So, here all blocks are digital. These whole clocks are in the digital domain. Because the lab circuit and circuit are everything digital domain, only output voltage and this output voltage assumes that it is already a digitally controlled converter and I want to improve the (Refer Time: 13:09).

So, here it is your sense current for protection purposes, this may be protection current and then you have an analog comparator. Because in the protection circuit also if the current exceeds some limit, it has to stop. So, this circuit can be utilized to do this implementation.

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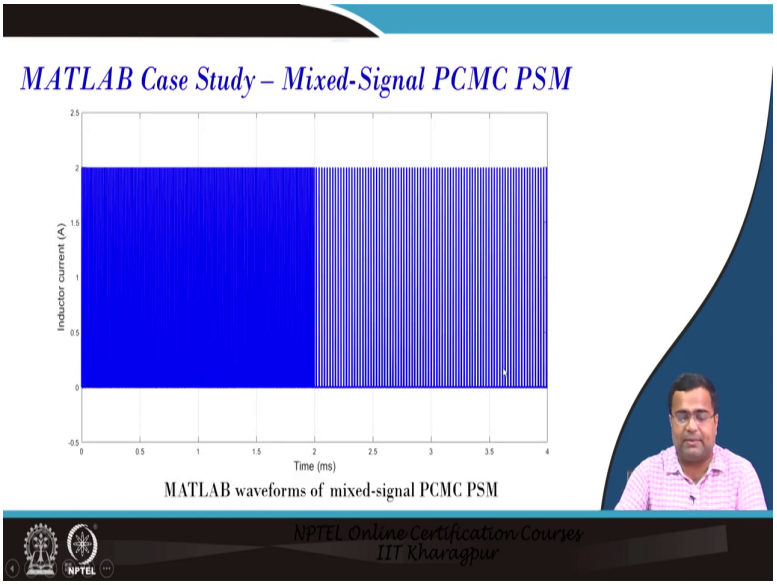

And we want to see the MATLAB case study. So, let us go to MATLAB and see the case study here.

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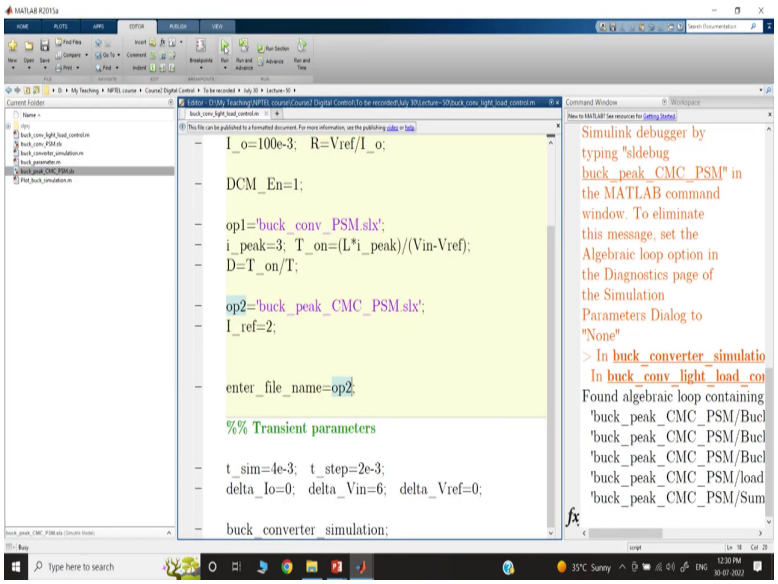

So, in this case, now we want to go for option 2. What is option 2? Option 2, is the current mode control case study, here you can see, these blocks remain the same; there is no change in this block.

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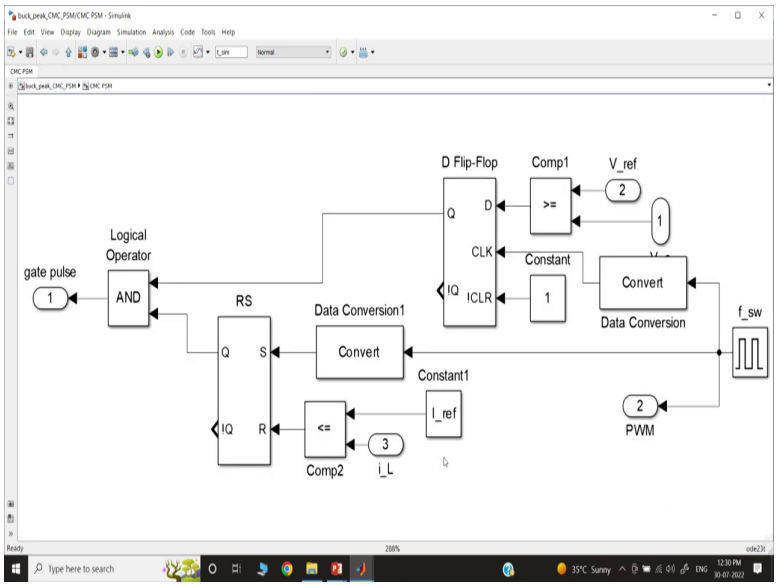

Now, if you go inside. So, you will find, now this block remains the same, but this block is additional. So, this is like a peak current base PSM and that gives the duty ratio. So, this duty ratio generation block is a new addition and that is in this case; that means, you are incorporating it here.

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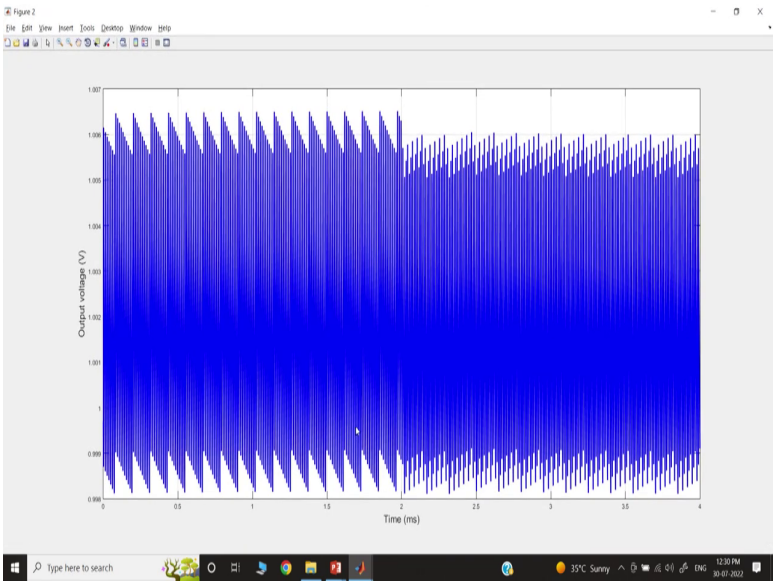

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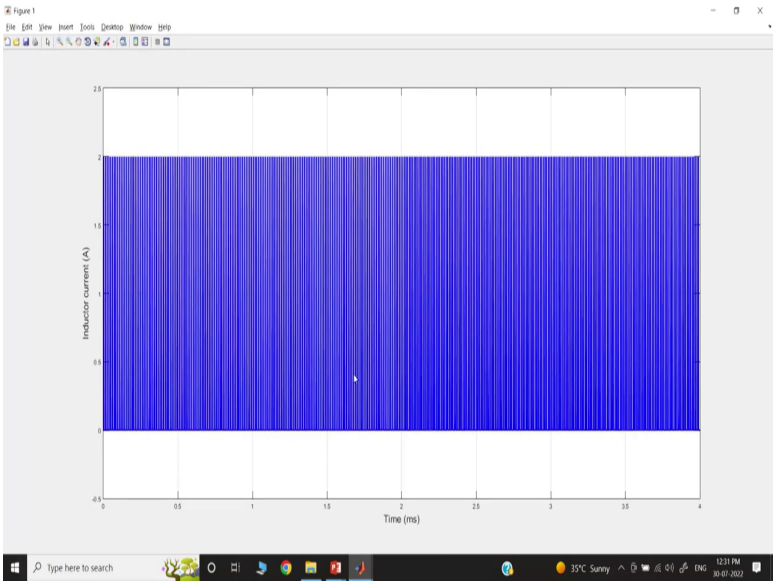

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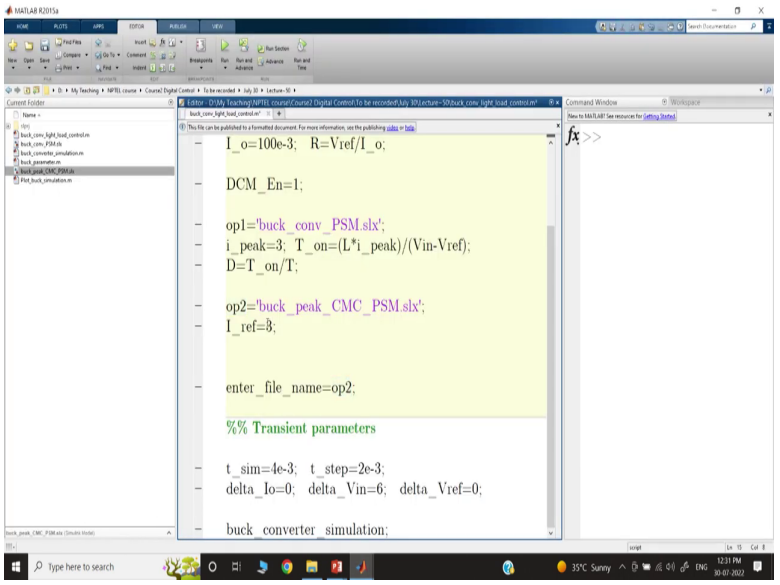

Now, if you want to simulate option 2, you can see, we are making a supply transient; that means, you can see the, but the inductor current remains the same because we are using a 2-ampere peak current in this case.

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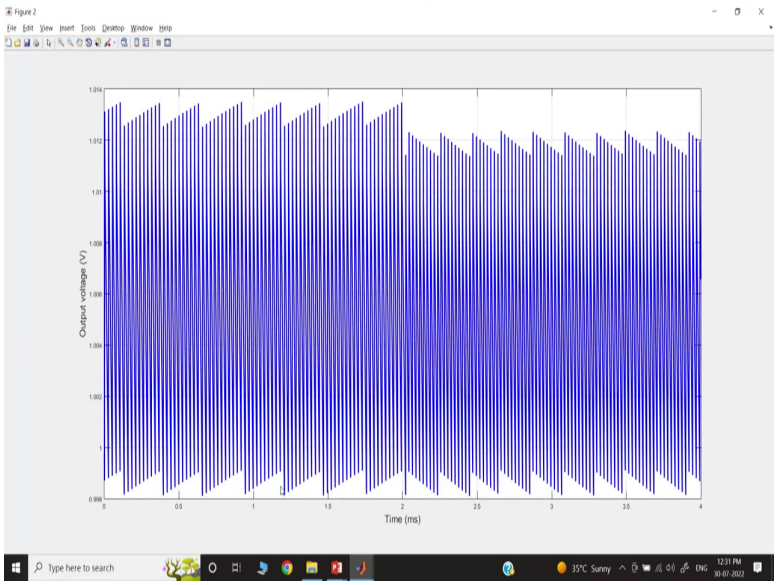

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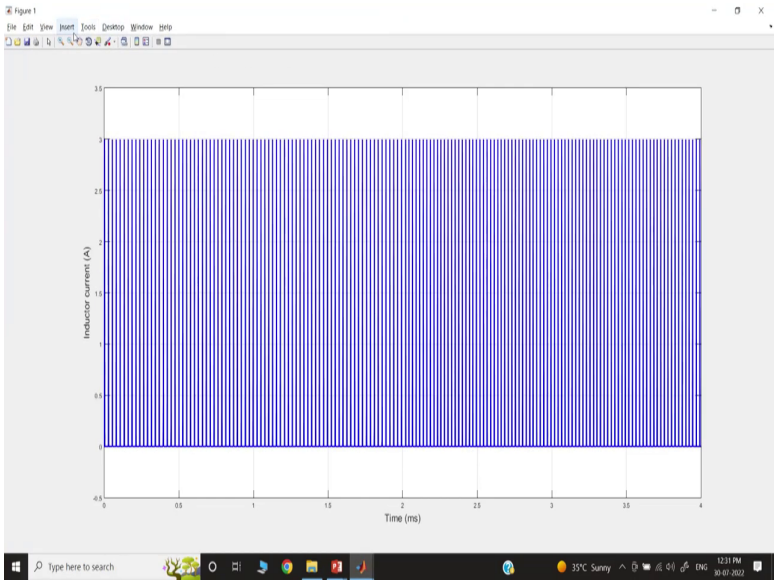

So, let us see, instead of 2 ampere, we can use 3 ampere to match the earlier case, no problem. So, if you do that, you will see, these 2 ampere peak current differences of 3 ampere are fixed, but here 3 milliseconds we are applying a transient, sorry at 2 millisecond, we applied transient.

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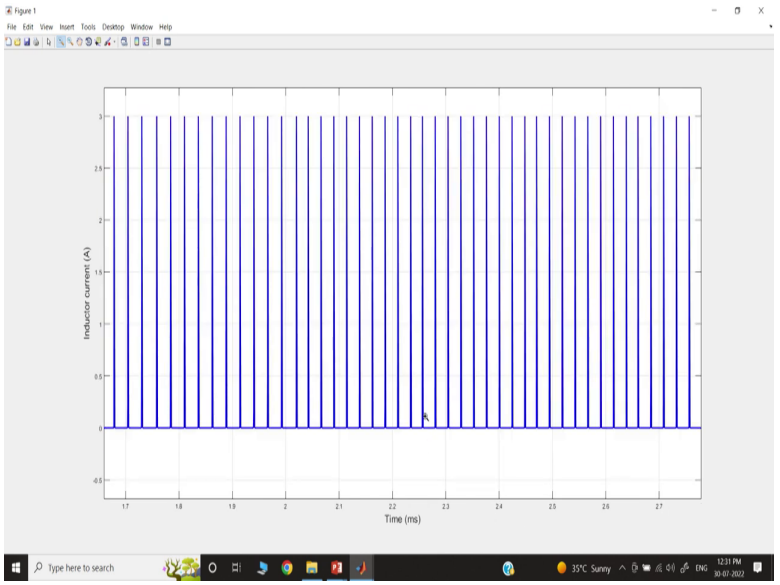

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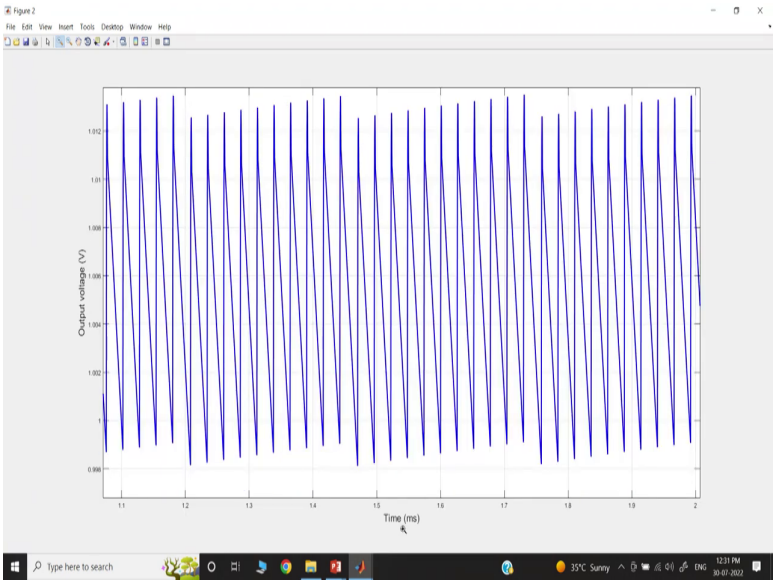

So, in 2 milliseconds, you will not find any effect. Because the pulse skipping skips the peak current the same. So, I mean you can maintain the ripple. So, you can see the output voltage ripples are more or less the same, but you may find some high periodic behaviour. Because, case of charge pulse skipping, we are let us say we are giving one charge pulse and that gives some duty ratio and during that time the energy is injected. The same energy has to be delivered to the capacitor, in the subsequent skip cycle.

So, ultimately over a period of one charge and a few skips, there should be a charge balance. But suppose, if there is a slight change in input voltage; that means, we are giving increased input voltage, we are giving some excess charge, and over 5 skip cycles they may not be perfectly balanced; there can be some residual charge. So, that over a multiple you know cycle of charge pulse followed by skip pulse, that period about multiple like an after 3, 4 combinations of this there can be an extra skip pulse.

And because of that this high periodic behaviour is coming and this has been well researched. We have first identified this technique for analog pulse skipping control and subsequently, there are multiple pieces of literature to address this, but this is not a big deal because we are not this is not affecting too much the ripple current. So, it is fine. So, we may go ahead with this design.

So; that means, we have discussed, that how to design this current-based mixed signal PSM, and these are the result for change in you know you can change input voltage load current whatever it is.

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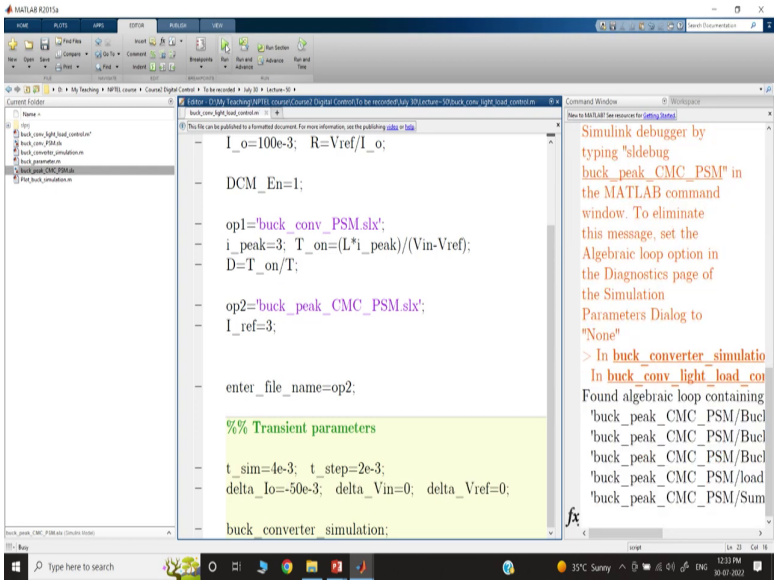

So; that means, we have introduced pulse-skipping modulation. Now we want to check for the same MATLAB case study, suppose we now, instead of input voltage change, want to make load transient; that means, will 0 and here we will make minus 50 milli ampere load current change.

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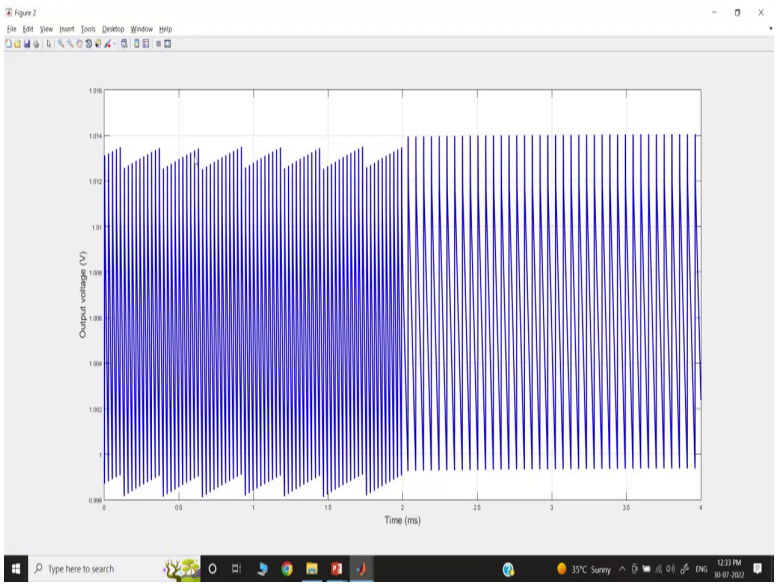

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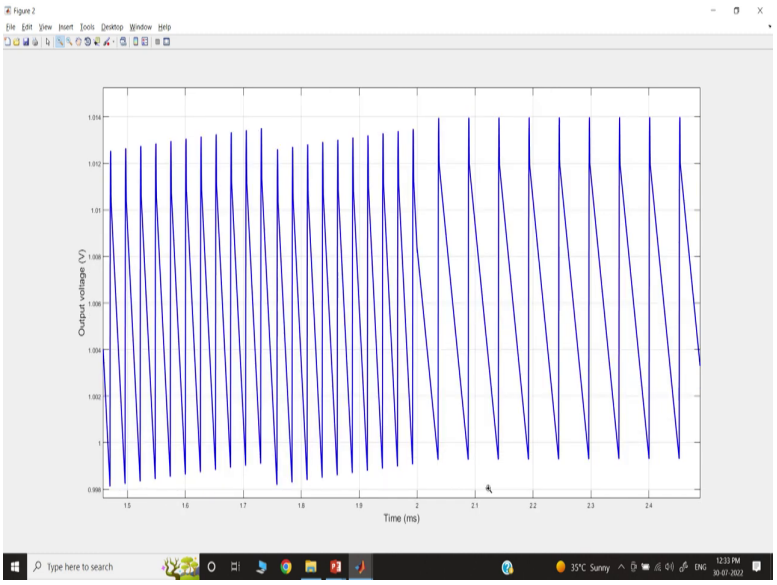

So; that means, from 100 milli ampere to 50 milli ampere there is a change, you see automatically several skip cycle increases. So, effective switching frequency seems to be reduced. So that means, it retains all the benefits of pulse skipping, and at the same time, it can manage the ripple adjustment, it is a kind of adaptive duty ratio control, under the charge cycle. So, it is a pulse skipping with adaptation in the duty ratio.

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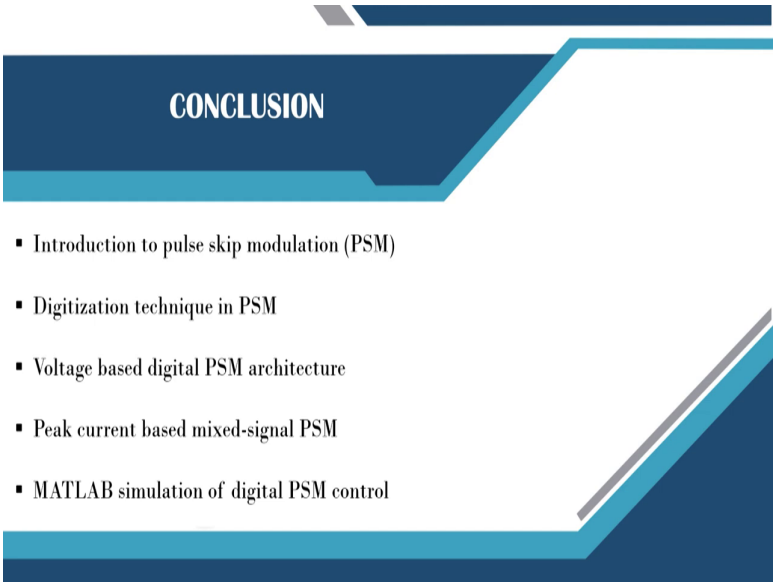

So, we have discussed this. So, in summary, we have discussed the pulse-skipping operation, and we have discussed the digitization method. We have discussed voltage-based digital pulse

skipping control, we have discussed peak current-based mixed signal pulse skipping and we have considered, multiple simulation case studies.

So, in the subsequent lecture, when you go to hardware implementation, we want to implement some of this logic in the digital control platform using FPGA and you want to show some practical demonstration case studies. That is it for today.

Thank you very much.