**Digital Control in Switched Mode Power Converters and FPGA-based Prototyping**

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**Module - 05**
**Frequency and Time Domain Digital Control Design Approaches**
**Lecture - 44**
**Design under Digital Current Mode Control – Frequency Domain Approaches**

Welcome. So, in this class, we are going to talk about the Design of Digital Current Mode Control using Frequency Domain Approach.

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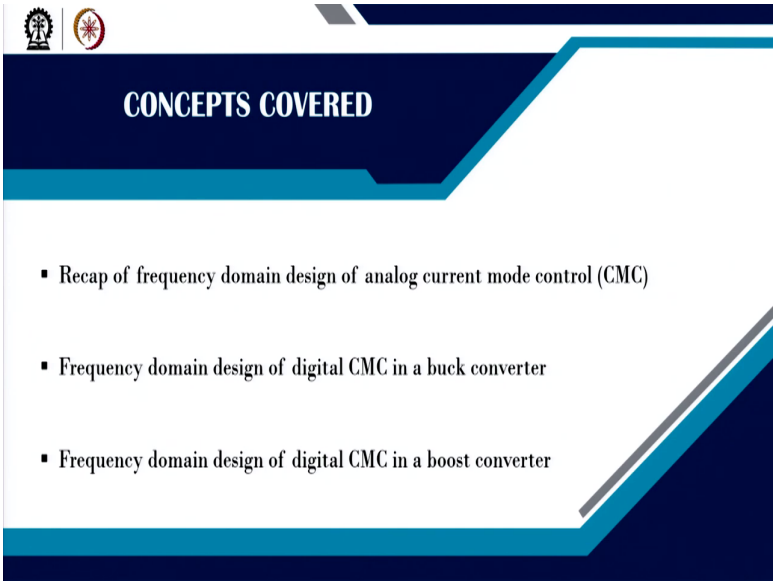


So, here we will discuss we will recapitulate the frequency domain design of analog current mode control, then we will discuss the frequency domain design of digital current mode control in a buck converter, and then the frequency domain design of digital current mode control in a boost converter.

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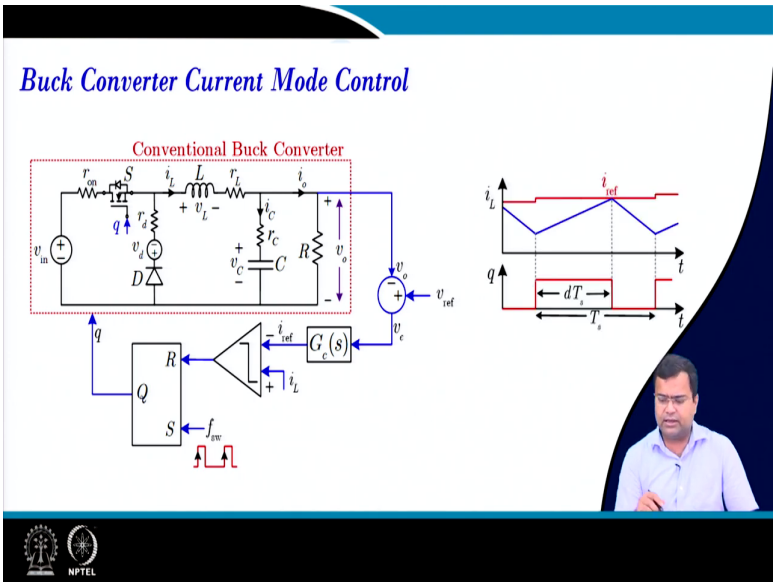


So, here we are talking about a buck converter current mode control, and this diagram we have explained multiple times, and this is analog control and then it is a peak current mode control.

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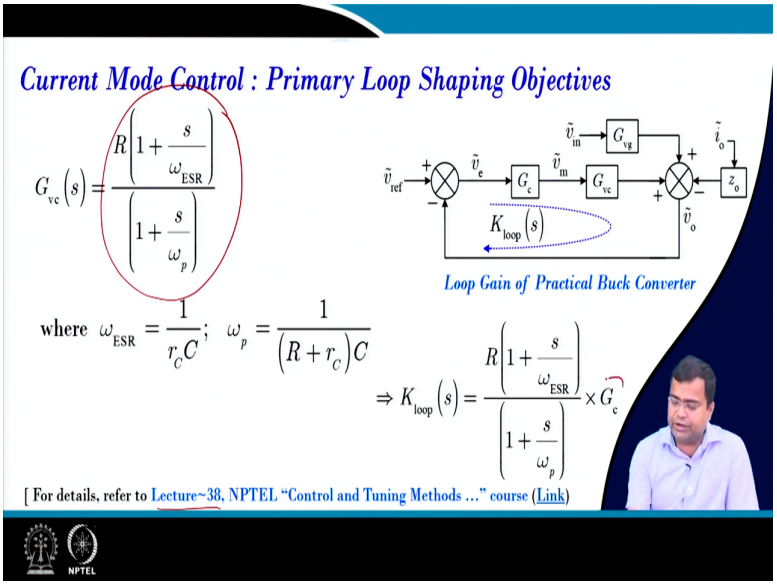


Now, when you are going for loop shaping of analog peak current mode control, we know that control to output transfer function if we use a very simple approximate model, it can be written in terms of a first-order model, and then we can find out the ESR 0 and poles and all.

And, this thing we have discussed in lecture 38 in NPTEL our previous NPTEL course, and the loop transfer function will look like this where we need to select the suitable controller.

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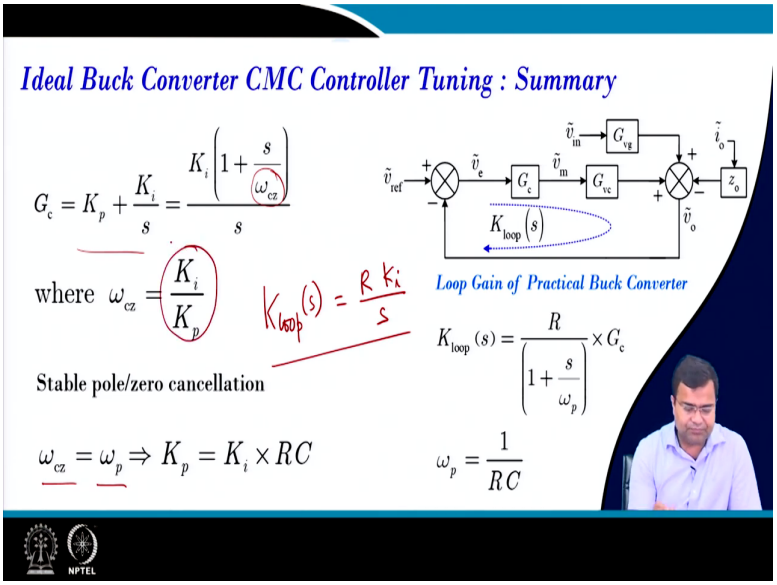


Now, we have discussed if you take an ideal buck converter or if the ESR is very very low then the ESR frequency due to the ESR; means, ESR 0 that frequency it will be much outside the control bandwidth as well as it can be even higher than the Nyquist frequency half of the switching frequency. So, it has almost no role in the closed-loop performance because it is at a much higher frequency.

So, in that case, we may not need to compensate for this 0, so, we will assume we will neglect this effect. In that case, it can be written in terms of an ideal buck converter; that means if this 0 is not there and then it will be simply R by 1 plus S divided by omega p. Now, we want to design a PI controller. So, if you take a PI controller it takes this form where omega cz that is the controller 0 will be K i by K p and we are now trying to shape the loop if we shape the loop what does it look like?

Using stable pole 0 cancellations, the loop will be something like a loop s using stable pole 0 cancellation R k i by s that will be a loop transfer function. Where omega CZ is placed in coincidence with our plant pole that is nothing but then we can find out; that means, this expression is this one and we know that omega p from here omega p from here. And, since we are ignoring the effect of ESR so, we can simply write this expression; that means, the

proportional gain can be obtained which is a function of integral gain and then load resistance and the capacitor.

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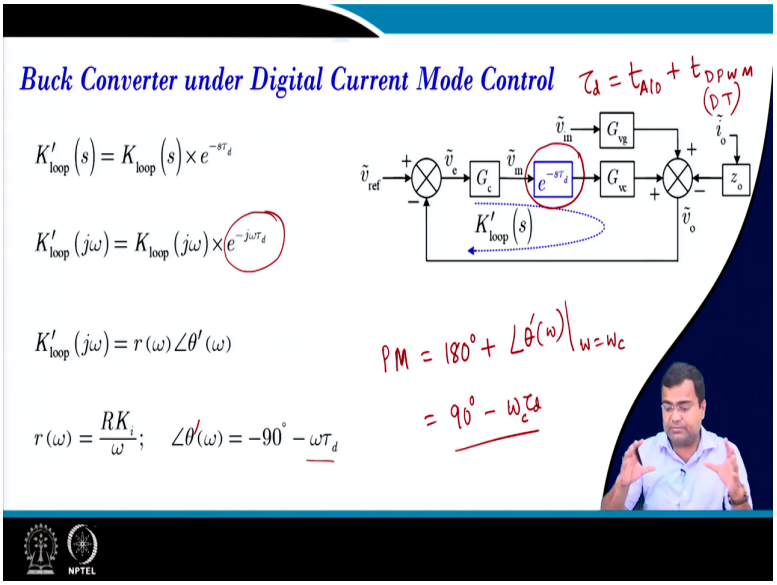


Now, when you go to digital current mode control, we know that again we have discussed in lecture 40 that we may have to introduce that simple delay; that means, you know the delay due to what is the delay? That is due to the ADC or A to D conversion delay plus delay DPWM and we know that DPWM delay is nothing but D into T.

Now, if we write the loop transfer function compared to the previous one only the delay term will come and we have discussed this delay will not affect the frequency response it will not affect the phase gain plot, but it will affect the phase plot because if you take the original analog loop transfer function it is simply some gain by s. So, the phase margin is 90 degrees and because of this term, we will get an additional minus omega tau d.

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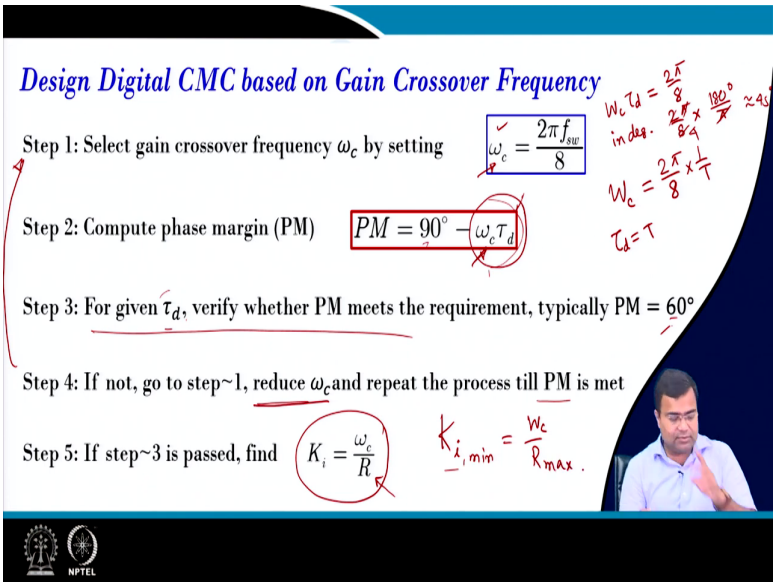


So, that means, the phase margin will be in this case what will be the phase margin it will be 180 degrees plus theta omega sorry, it will be theta dot omega which is nothing but 90 degrees minus omega tau d. So, by suitably selecting the gain crossover frequency so, this will be computed at omega equal to omega c. So, this will be omega c because we have to calculate the phase margin at the gain crossover frequency.

Now, what is the design step? So, we have to first select the gain crossover frequency. So, typically for current mode control for voltage mode in a buck converter we generally go one-tenth of the switching frequency, but in the case of current mode we can slightly increase, and that we have discussed in our earlier NPTEL course.

We can go effectively by one-eighth of the switching frequency and if you select one-eighth of the switching frequency and we know the phase margin computation because the exact cancellation for analog will be 90-a degree phase margin and it will be a delayed version. So, there will be a phase lag.

Now, depending upon the delay amount for the given delay because you may have up to one cycle delay if it is a switching cycle full cycle delay, then omega c what will be omega c? We have taken here 2 pi by 8 into f s which is nothing but 1 by T. And, we are talking about tau d which is also T; that means, what is my omega c tau d it will be simply 2 pi by 8 it is in radian and if you want to convert into a degree in degree how much? So, it will be 2 pi by 8 into 180 degree by pi.

So, if you cancel this, this will be 4. So, it will be around 45 degree. So, that means, you will lose around 45 degree phase margin due to this delay, but; that means, for a given tau d we may have to achieve it because in current mode control very easily we can get you to know we typically want to achieve 60 degree phase margin in the conservative case. So, that means, this will define what is the acceptable delay. So, if you have a delay higher than that then you need to sacrifice the phase margin.

So, now if we want to 6 achieve 60 degree phase margin for the given tau d it may so happen that your 60 degree phase margin may not be met, then you may have to reduce this. But, in this current mode controlling omega c has no effect it has an effect; that means, if you reduce the omega c, then we can reduce the phase contribution because of the delay we cannot. Delay is coming from the digital controller based on what ADC is using and what DPWM delay we cannot do anything.

But, we can reduce this product term by reducing omega c; that means, we have to reduce the crossover frequency; that means, that our initial target was to achieve one-eighth of the switching frequency to achieve 60 degree phase margin you may have to operate below one-tenth of the switching frequency. This is due to meeting the required phase margin.

Once this is not satisfied then you have to go to step 1 reduce the omega c and then again cross-check unless you reach 60 degree phase margin. Once it is met; that means, you know what is my crossover frequency, then you simply obtain the integral gain by this omega c by R.

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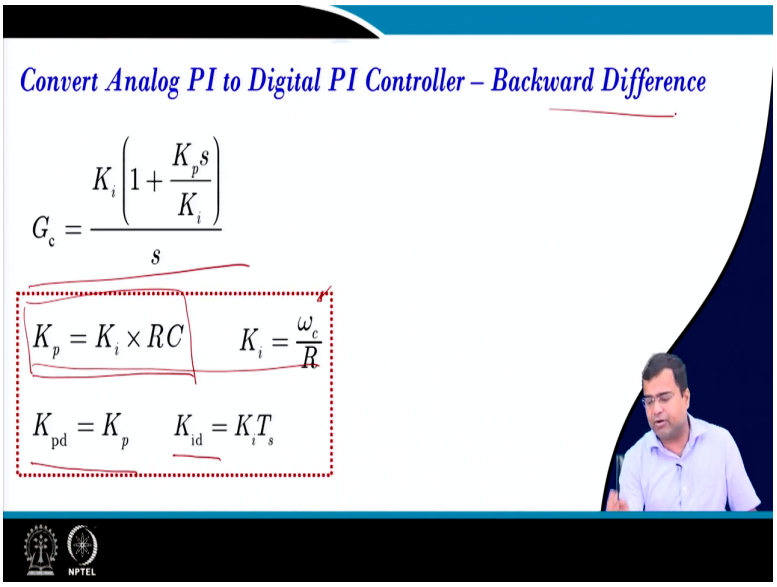


Now, once you have then we have to convert. Now you see the integral gain is a function of load. So, if you want to get the worst-case integral gain maybe you should select a conservative choice. So, you should take the highest load current condition ok. Now, that means, a higher load current which is a; that means if you want to get k i to be because the problem will be if you take a very large k i it may cause a problem during the light load when R will be very high.

So, we should choose a k i which is the minimum value and that is dependent on omega c into R max. Then what is the maximum load resistance? So, this will give the K i minimum then we want to convert analog PI into digital and this is straightforward this is the analog PI controller. We already know K p is a function of K i into RC and we already have found K i to be omega c by R and we have already selected omega c based on the required phase margin criteria.

Now, we want to convert the proportional analog controller gain into discrete time and the proportional gain will remain the same integral gain will be simply the analog integral gain minus the sampling time where the sampling time is the same as the switching period. So, in that way, we can design the controller by using the backward difference formula.

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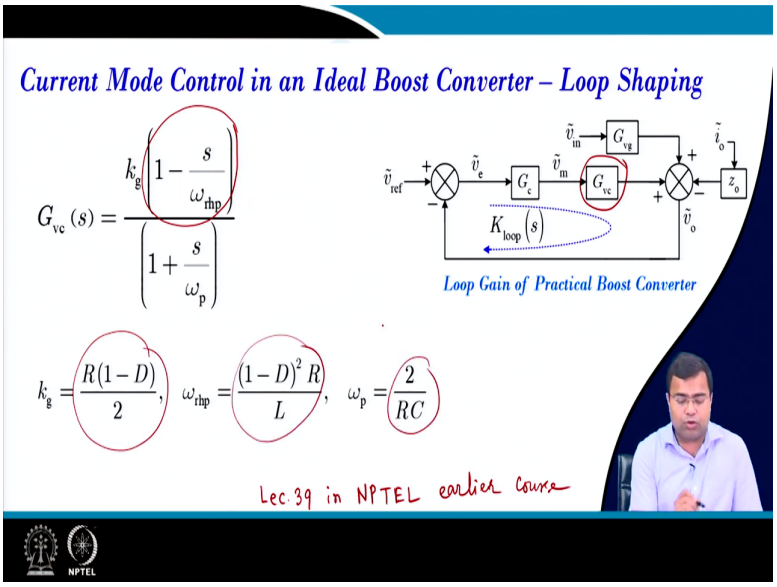


Now, when we go for a boost converter then in a boost converter if you write the loop transfer function, G vc which is a control to output transfer function will have a right half plane 0 and that is also discussed in our you know lecture number I think it was discussed in lecture 39 in our you know NPTEL earlier course NP earlier course.

So, then if we have this rhp 0 and this expression is already given so, this is the expression omega rhp 0 that is the right half plane 0, then this is the pole.

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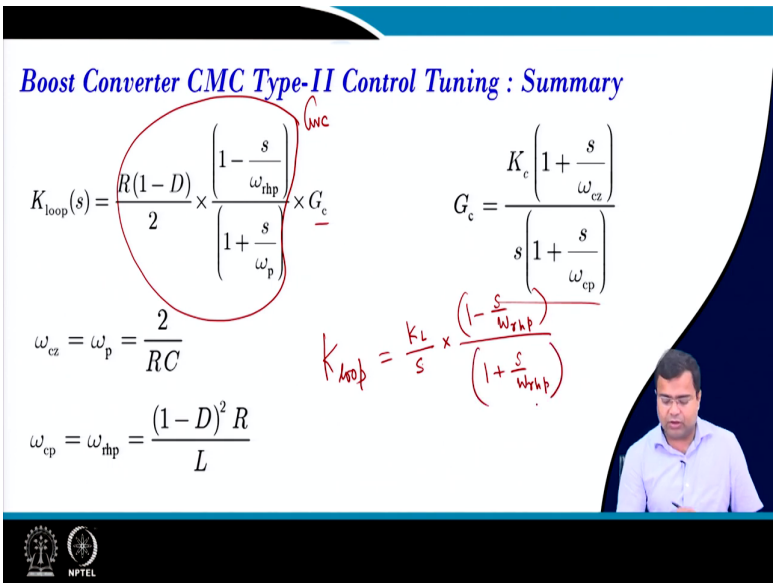

Now, we want to design a type-II compensator why because in the case of type-II, there should be another s type-II compensator, the controller error I mean in the case of a PI controller we will have a just 0 and 1 pole at the origin, but in type-II, we have an additional pole and that is needed to anticipate the effect due to the rhp 0 because the controller pole where this is the controller pole. Sorry, this is the plant I am sorry for the loop transfer function. So, I think this is all right because this part is our G vc is our G vc. So, you have to design the controller.

So, if the controller is this form, then what is the loop transfer function? So, the loop transfer function now after this compensation, will be some gain divided by s into 1 minus s omega rhp divided by 1 plus s omega rhp, ok. So, loop transfer function.

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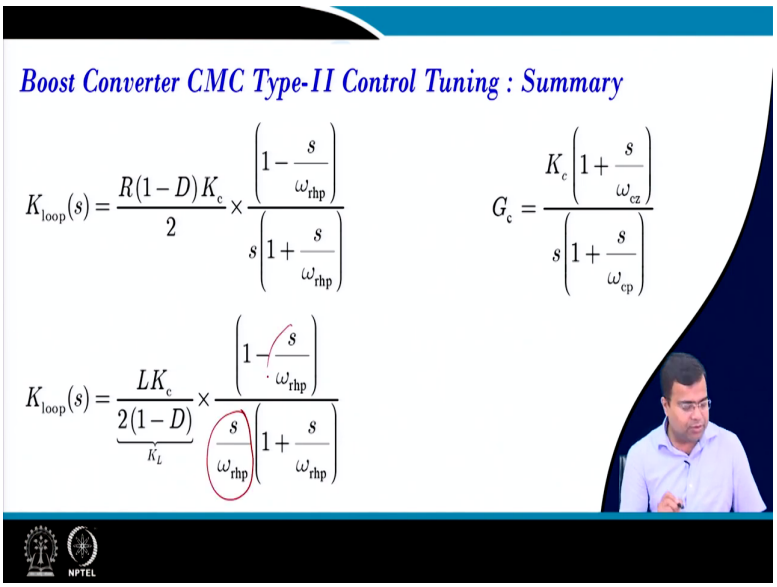


And, now we have to design. So, the summary is that this is the loop transfer function that we have discussed, this is a controller and this is the loop transfer function we are writing in terms of K L and here we are using this term because it is common.

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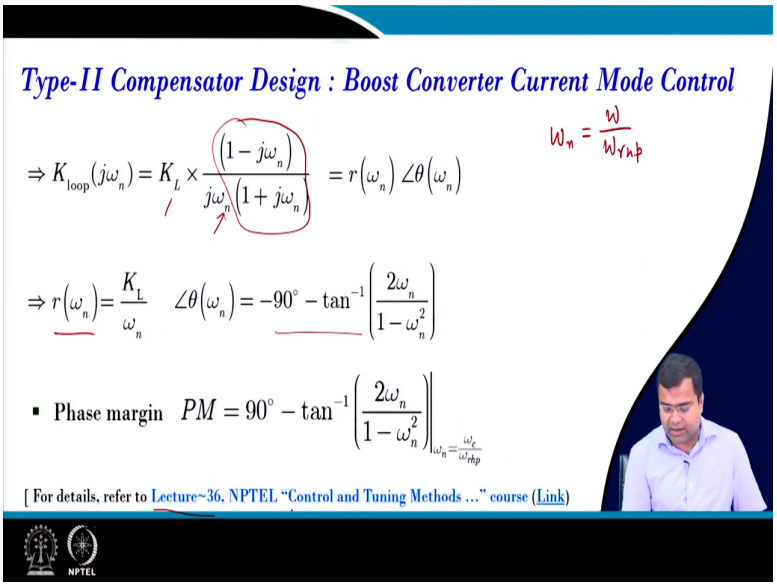


Now, we can do a normalization by selecting omega n to be omega by omega rhp. Then we already know that the gain plot can be written as K L by omega n because this term and this term their gains are identical. So, there will be 1 and the gain will be primarily because of this term and this scale, but the phase will be this term, and then what we will get? The phase margin will be 90 degree minus tan inverse of this and this will be computed at the crossover frequency. And, this is discussed in lecture 36 in our earlier NPTEL course.

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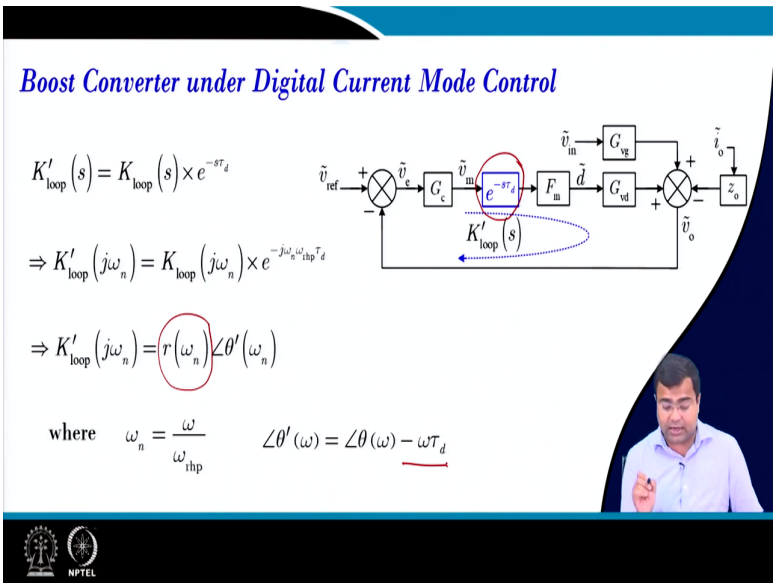

Now, we want to design a digital current mode control. In the case of digital current mode control, we have this additional delay and it will affect the loop transfer function in terms of phase. It will not affect the gain, the gain will remain the same, but the phase will be affected there will be an additional phase lag of minus omega tau d.

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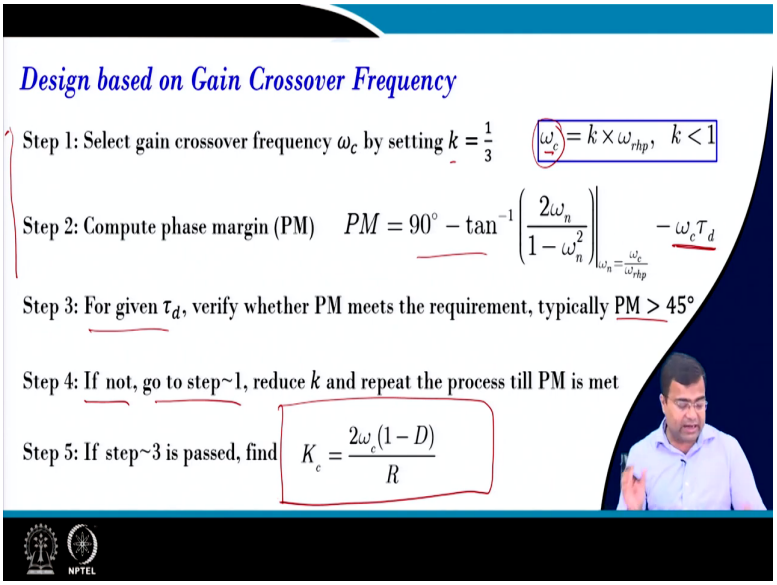


That means if you want to design based on the crossover frequency we can first set it in the current mode control analog we typically can achieve the crossover frequency one-third of the rhp 0. So, we will start with that point then we will compute the phase margin because we have an additional phase lag due to the delay. So, given delay, if the delay is given, then we need to check if can we meet a phase margin of 45 degree or not. If it is not then you need to reduce the crossover frequency if not go to step 1 reduce k.

So, that means, the factor is reduced. So, the crossover frequency is reduced and you iterate this process till the phase criteria are met. Once it is met; that means, for setting the suitable value of omega c, then you can compute the Kc from this expression, and after computing this; that means, you got the controller gain and now all the controller parameters are known.

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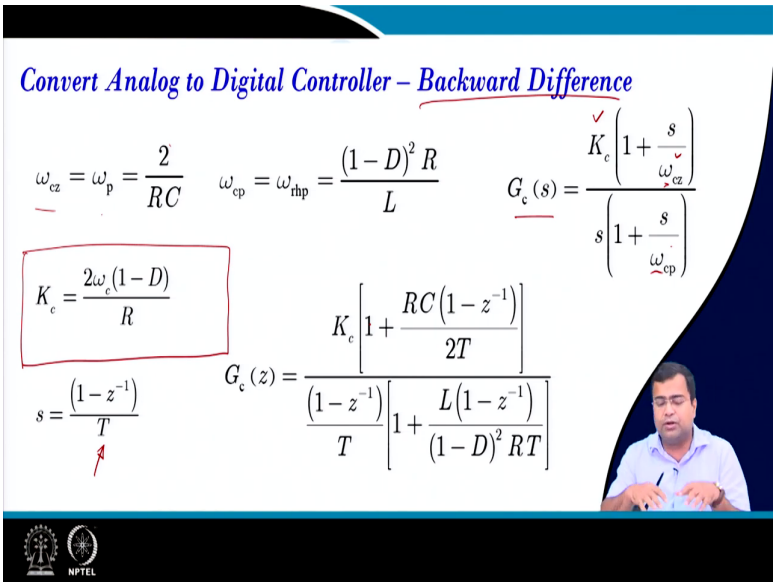


So, now, we are summarizing the equation. This is my controller and the first controller 0 is to plant pole which is 1 by 2 RC. Then the controller pole is nothing but the rhp 0 in coincidence we are placing, this is also known. Then we have just computed right now, this is computed in such a way we can achieve the desired phase margin which is typically 45 degree.

Then once we get it; that means, in this controller all the values we know. So, the controller parameters are known, but it is in the analog domain. So, we have to convert this analog into digital using backward difference formula where we need to place s equal to 1 minus z inverse by T, where T is the sampling time which is the same as the switching period because we are taking uniform sampling at the rate of the switching frequency.

And, then we can convert this G c z in this, and then if you obtain the inverse Laplace we can write the expression of the differential equation of the controller, and that we can also discuss. So, we are going to take the case study of digital current mode control for both buck and boost converters in the subsequent lecture when MATLAB case study when we want to design by this frequency domain approach in using continuous type model with delay.

And, we also want to discuss direct digital design; that means, in the time domain. And, we also want to show some case studies with the direct design and this frequency domain design and there we want to show the MATLAB simulation case study.

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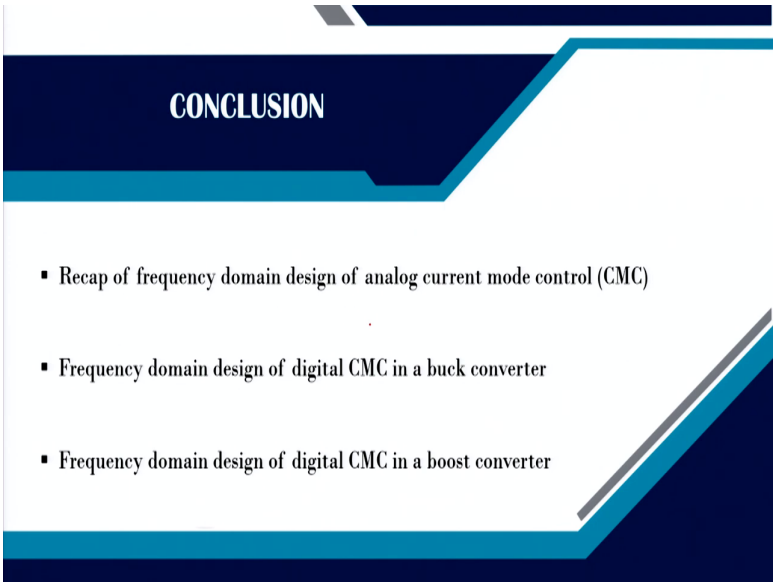


So, in summary, we have discussed we have recapitulated the frequency domain design approach of analog current mode control. We have discussed the frequency domain design of digital current mode control in a buck converter and we have also discussed the frequency domain design of digital current mode control in a boost converter. And, we will be taking a MATLAB simulation case study in the subsequent lecture, when we also consider the direct digital design as well as we also want to consider the large signal-based current mode control design. That is it for today.

Thank you very much.