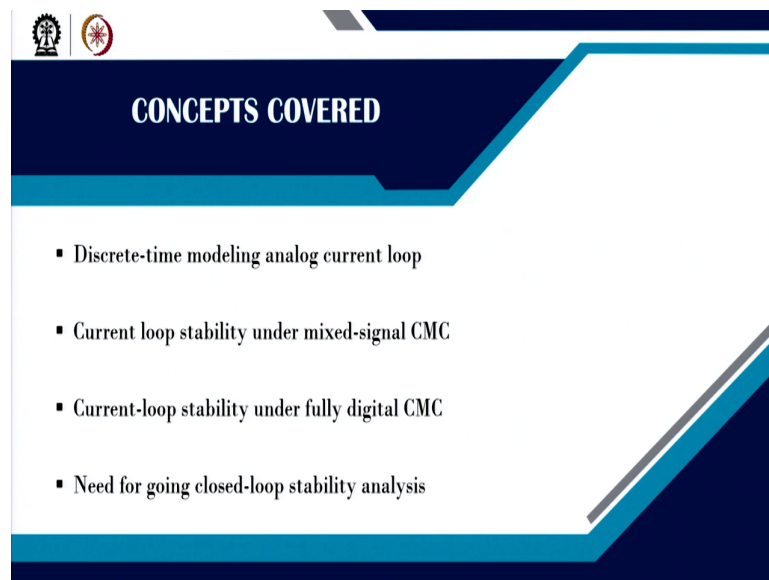


**Digital Control in Switched Mode Power Converters and FPGA-based Prototyping**  
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**Module - 04**  
**Modeling Techniques and Mode Validation using MATLAB**  
**Lecture - 32**  
**Discrete-Time Modeling with Closed Current Loop**

Welcome back. In this lecture, we are going to talk about Discrete Time Modeling with a Closed Current Loop.

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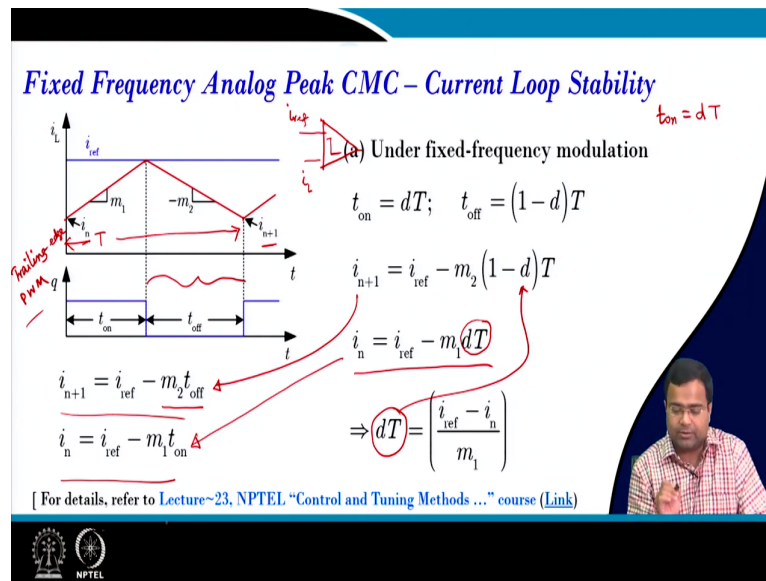


The slide features a dark blue background with a light blue diagonal stripe. At the top left, there are two small circular logos. The main title 'CONCEPTS COVERED' is centered in white. Below the title, a bulleted list contains four items.

- Discrete-time modeling analog current loop
- Current loop stability under mixed-signal CMC
- Current-loop stability under fully digital CMC
- Need for going closed-loop stability analysis

So, we will first consider analog current mode control and the current loop stability with only the inner current loop closed. Then, we will talk about what is the stability criteria of the current loop stability criteria under mixed signal current mode control. And, then we will see what is the stability criteria under fully digital current mode control. And then why do we need to go for closed-loop stability analysis, that also we will see in this lecture; the motivation behind you know analysis of closed-loop stability.

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So, first, we will start with the current loop stability under analog current mode control. So, here you can see this is our peak current reference and we are considering the current reference to be constant; that means, here is my  $i_{ref}$  and it is compared with the sense current there is a comparator. And, in current mode control, there will be a latch circuit. And this is we are talking about the trailing edge modulation that is under peak current mode control. So, it is under trailing edge PWM and peak current mode control.

So, here we want to first write what is the equation ok. So, we want to write. So, this is under trailing edge modulation, this is under trailing edge PWM. And, we want to write this  $i_{n+1}$  in terms of  $i_n$  and want to check what is the stability of the current loop. So, first, we will start with how can we write  $i_{n+1}$  in terms of  $i_{ref}$ . So, it will be  $i_{ref} - m_2 t_{off}$ . The cut-off is this duration; then we need to find how  $t_{off}$  can be represented in terms of  $i_n$ .

So; that means, again we can write that  $i_{ref}$  another equation; that means,  $i_n$  which is this current is equal to  $i_{ref} - m_1 t_{on}$  right. So, these two are the two equations. And how do you relate these two equations? So, under fixed frequency modulation; that means, if you are talking about the trailing edge PWM, then we generally write the on time; that means, we keep on time to be duty ratio into the time period.

So, under trailing edge fixed frequency, we take the time period constant. And then, we will replace  $t_{on}$  equal to  $dT$ ; then what is  $t_{off}$ ? It is  $1 - d$  into  $T$ . And, then let us substitute. So, first, we will substitute in this equation and we will get this equation, then the next

equation again we substitute here where  $t$  on equal to  $dT$ . Then, we want to replace this intermediate variable  $dT$  in both equations, and then we can get. So, do will be from this equation; what is it? It is  $i_{ref}$  minus  $i_n$  by  $m_1$ .

Now, we want to replace this  $DT$  term in this equation and then want to find it. And the detail of these derivations is discussed in our previous NPTEL course in lecture number 23. So, if you substitute; that means,  $dT$ ; that means, what you got? it is equal to  $i_{ref}$  minus  $i_n$  by  $m_1$ , and we have substituted here, and then we will get the full expression.

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**Current Loop Stability Analysis (contd...)**

Thus,  $i_{n+1} = i_{ref} + m_2 \left( \frac{i_{ref} - i_n}{m_1} \right) - m_2 T = - \left( \frac{m_2}{m_1} \right) i_n + \left( 1 + \frac{m_2}{m_1} \right) i_{ref} - m_2 T$

Perturbed current dynamics becomes

$$\tilde{i}_{n+1} = - \left( \frac{m_2}{m_1} \right) \tilde{i}_n + \left( 1 + \frac{m_2}{m_1} \right) \tilde{i}_{ref}$$

Assumptions:

1. Perturbations in slopes are neglected
2. Nonlinear perturbed (product) terms are neglected

[ For details, refer to [Lecture-23, NPTEL "Control and Tuning Methods ..."](#) course ([Link](#)) ]

So, if you separate the term associated with  $i_n$  and if we separate the term associated with  $i_{ref}$  and the rest of the offset term, then what can you write? Now, this is the large signal current loop equation where since we are keeping the  $i_{ref}$  constant and we are not; that means, we can assume that for small perturbation, the slope perturbation is neglected; that means, we are assuming that the perturbations of the slopes are neglected. So, that means, under perturb conditions, this quantity will be 0.

And we are taking  $m_2$ ,  $m_1$  is constant. And another condition, we initially considered a fixed current difference; that means, the change in current the perturbation in  $i_{ref}$  will be 0. So, if you set perturbation in the; that means, another product perturbation we can ignore. So, there are two I mean for this equation there are two terms that will come out; that means, one is what is called zero input stability zero input stability; what does it mean?

So, under zero input stability, the perturbation for the input is 0. So, here the control input is my reference current because if the current loop is closed and the  $i_{ref}$  is my control variable. So, I want to keep  $i_{ref}$  to be constant then we will consider  $i_{ref}$  perturbation this tilde to be 0. But,  $i_n$  perturbation initial condition is non-zero; that means, we are only perturbing the initial condition.

So, that is why it is called zero input stability. It is the stability only due to the perturbation in the initial condition ok. And that is you know sometimes it is also known as a homogeneous solution; that means, unforced response. Another is that zero state stability - under this condition we are not disturbing the initial current as if we are disturbing the reference; that means, we are perturbing the reference current.

So, what does it look like? Let us take a current waveform to let us take; so just to give a visual understanding. So, this is my time domain and this is my inductor current. So, if I draw the nominal current; that means, this is let us say this is my  $i_{ref}$ , and this is my nominal  $i_{ref}$ , and this is my nominal inductor current like this. Now, in the first case, we are perturbing the initial condition; which means, zero input stability this is case 1 and this is case 2.

So, in case 1, if we consider the perturbation in the initial condition; that means, let us say we are perturbing this. So, the current will reach here and then this perturb current will go, it will go up since it is fixed frequency it will continue. So, since we have applied a perturbation in  $\Delta i_n$  as and we want to see the effect the perturbation is  $\Delta i_n + 1$  ok. So, it is going out of the screen. So, let us say this will be  $\Delta i_n + 1$ ; that means, the perturbation effect of perturbation the end of the cycle.

So, this effect can be analyzed when we  $i_{ref}$  perturbation is set to 0. So, this blue line corresponds to condition 1. The second condition is if we consider the second condition. So, let us say green line green. So, here we are perturbing this current; that means, we are perturbing this  $i_{ref}$  now, so; that means, this will be my nominal  $i_{ref}$  plus some  $i_{ref}$  perturbation then how does this trajectory look like?

So, under that condition, we will consider letting us say this same because we are not disturbing the initial current, but we are perturbing this current. So, it is coming, coming, coming like this. So; that means, the effect due to this perturbation; that means, this perturbation which is my  $\Delta i_n + 1$  due to the change in  $\Delta i_{ref}$  or  $\tilde{i}_{ref}$  tilde is the perturbation due to the second condition. This is our condition 2.

So; that means, we want to see the first condition if we keep the  $i_{ref}$  constant and if you perturb the  $i_n$ , then we want to see the natural response whether the current loop is stable or not for a given constant reference. And the second case will be helpful for the closed-loop stability analysis. And if you combine them then the entire closed-loop stability analysis can be carried out. So, and these things can be the details of this derivation can be obtained in lecture number 23.

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**Current Loop Stability Analysis (contd...)**


For constant reference,  $\tilde{i}_{ref} = 0$ ; *inner current-loop stability due to the perturbation in  $i_n$*

Thus,  $\tilde{i}_{n+1} = -\begin{pmatrix} m_2 \\ m_1 \end{pmatrix} \tilde{i}_n$   *$\tilde{i}(z) = (z + \frac{m_2}{m_1}) \tilde{i}_n$   
 $z = -\frac{m_2}{m_1}$*

For inner loop stability,  $\left| \frac{m_2}{m_1} \right| < 1$

Slope	Buck Converter	Boost Converter
$m_1$ ✓	$\frac{V_{in} - V_o}{L}$	$\frac{V_{in}}{L}$
$m_2$	$\frac{V_o}{L}$	$\frac{V_o - V_{in}}{L}$

[ For details, refer to [Lecture~23, NPTEL "Control and Tuning Methods ..." course \(Link\)](#) ]



So, here if you want to say zero input stability; that means, we are taking only the inner loop current and inner current loop stability due to the perturbation in  $i_n$  that is the initial current. And that is why you are not perturbing the  $i_{ref}$ , then inner loop stability. So, this will be the perturbation. And it is a discrete-time equation. So, we want this quantity the whole quantity associated with that mod of this should be smaller than unity.

And if you can ensure this mod because it is a discrete-time; that means, that should be inside the magnitude should be inside the unit circle; that means, the location of this coefficient such that if you obtain the z transform then you know what if I apply the z transform what will get. You will get  $\tilde{i}_1(z)$ , and this will be  $z$  for this  $n+1$  plus  $\frac{m_2}{m_1}$ ; this whole thing 0.

So, we have to ensure that  $z$ ; that means,  $z$  is equal to minus  $\frac{m_2}{m_1}$ . So, you have to ensure that this minus  $\frac{m_2}{m_1}$ , there should be always a unit within the unit circle. So, it can be proved if we take the mod of this. And if we write  $m_1$   $m_2$  expression for the buck and boost converter. So, we know that the rising slope of the buck is  $V_{in} - V_o$  by  $L$  for

the boost it is  $V_{in}$  by 1, and for the buck falling slope is  $V_0$  by 1 I mean we are talking minus of  $m_2$  falling slope.



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**Current Loop Stability Analysis (contd...)**

- **Buck Converter:**

$$\left| \frac{m_2}{m_1} \right| = \left| \frac{V_o}{V_{in} - V_o} \right| = \frac{V_o}{V_{in} - V_o} \quad (\text{Since } 0 < V_o < V_{in} )$$
$$\therefore \frac{V_o}{V_{in} - V_o} < 1$$
$$\Rightarrow \frac{V_o}{V_{in}} < \frac{1}{2}$$
$$\Rightarrow D < 0.5$$

[ For details, refer to [Lecture~23, NPTEL "Control and Tuning Methods ..."](#) course ([Link](#))



So,  $m_2$  equal to  $V_0$  by 1 and for the boost it is  $V_0$  minus  $V_{in}$  by 1. Then if you substitute it turns out that if you simplify that  $V_0$  by  $V_{in}$  should be less than half which means the duty ratio should be smaller than 0.5. So, only for the closed inner loop, but we are not talking about the closed loop it is just the inner loop closed. So, the requirement that the duty ratio should be smaller than 0.5, but we will see in the subsequent lecture, even much lower than a 50 percent duty ratio you will end up with subharmonic oscillation when you close the outer loop ok.



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*Current Loop Stability Analysis (contd...)*

- **Boost Converter:**

$$\frac{m_2}{m_1} = \frac{V_o - V_{in}}{V_{in}}$$
$$\therefore \frac{V_o - V_{in}}{V_{in}} < 1$$
$$\Rightarrow V_o < 2V_{in}$$
$$\Rightarrow D < 0.5$$

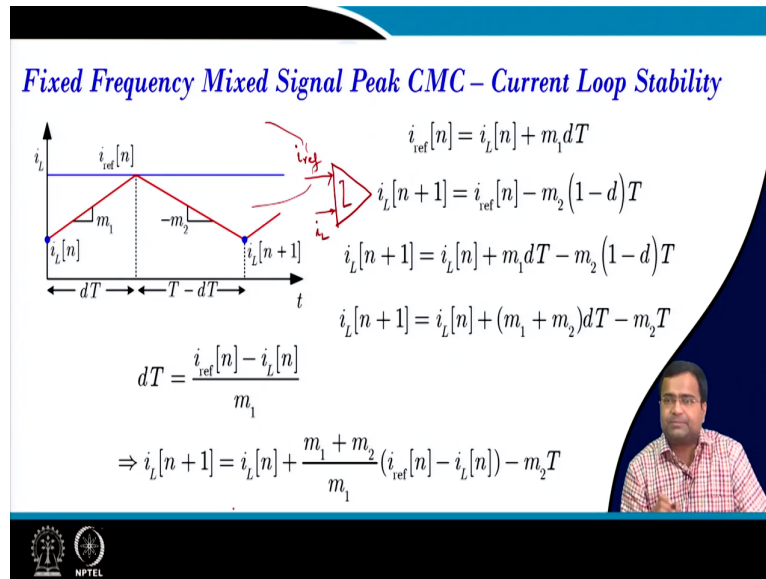
[ For details, refer to [Lecture~23, NPTEL "Control and Tuning Methods ..."](#) course ([Link](#))



Similarly, for the boost converter if you take again  $m_2$  by  $m_1$ , and if you get  $V_o$  by  $V_{in}$  that term because if you take mod of  $m_2$   $m_1$  since both are positive. So, it will be  $m_2$  by  $m_1$  should be smaller than 1, because it is always greater than 0. Then, again it can be shown the duty ratio should be less than 0.5. So, it is a universal requirement the duty ratio should be smaller than 0.5 with a closed inner loop.

Now, we want to see these things are already discussed here, but now we want to move forward. Because I was giving some conceptual understanding of the current loop, what will happen for mixed-signal current mode control?

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Remember, in mixed-signal current mode control your reference current and the inductor current are in analog. So, one can expect for the same reference current the mixed signal inner loop stability; that means, the zero input stability must be identical because they are identical in terms of the analog current loop. So, only the digital part will come here when the mixed signal will have a digital compensator followed by a D to A converter that we have seen.

After that, the  $i_{ref}$  is in analog and all the current loop comparator latch circuits are in analog which is identical to analog current mode control. So, with only a closed inner loop for a fixed  $i_{ref}$  the stability must be identical. And if we again carry out the same process  $i_L[n+1]$  and if you substitute the  $dT$  from this expression then this is the overall expression.



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**Fixed Frequency Mixed Signal Peak CMC – Current Loop Stability**

$$i_L[n+1] = i_L[n] + \frac{m_1 + m_2}{m_1} (i_{ref}[n] - i_L[n]) - m_2 T$$

Perturbed dynamics

$$\tilde{i}_L[n+1] = \tilde{i}_L[n] + \frac{m_1 + m_2}{m_1} (\tilde{i}_{ref}[n] - \tilde{i}_L[n])$$

Z transform

$$\frac{\tilde{i}_L(z)}{\tilde{i}_{ref}(z)} = \frac{1 + \frac{m_2}{m_1}}{z + \frac{m_2}{m_1}} \Rightarrow \left| \frac{m_2}{m_1} \right| < 1 \Rightarrow D < 0.5$$

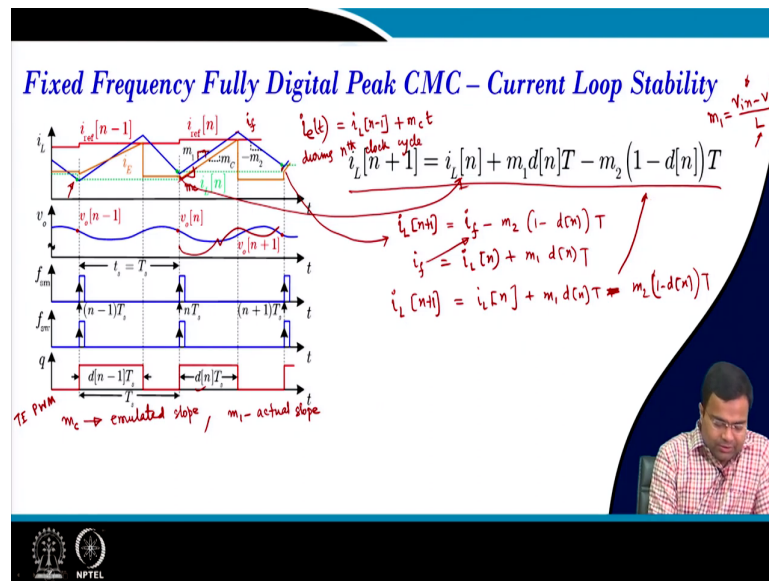
*Handwritten notes:*  
 $0 < \frac{m_2}{m_1} < 1$   
 zero-input stability  $(\tilde{i}_{ref} = 0)$   
 Same as analog CMC!!  
 Fixed reference current ineq

And, you can show you know subsequent perturbation that if you take the z transform it turns out again mod  $\frac{m_2}{m_1}$  should be smaller than 1. And since  $\frac{m_2}{m_1} < 1$  and  $m_1, m_2$  both are positive. So, you require that  $\frac{m_2}{m_1}$  must be greater than 0 which is true and it must be less than unity; and again it will come to less than 0.5. So, I do not know going through all the steps because we have already discussed the analog current loop.

So, the bottom line is this. So, the same as this; that means, the zero input stability are same where  $i_{ref}$  perturbation we are considering to be 0 that because it is analog current loop. So, we are only considering the initial perturbation initial current perturbation. But I will show you that if we consider  $i_{ref}$  perturbation with a closed loop then the stability criteria will be different even compared to your analog control and digital control they will be significantly different because of the sampling effect.

But in this case, we are not showing that. Here, in this case, we are showing that the current loop is only if we keep the fixed reference current; for fixed reference current  $i_{ref}$  the inner loop stability for both mixed-signal and analog current mode control are the same.

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Now, what will happen for fully digital current mode control? So, in fully digital current mode control I think we have discussed this in the previous lecture. In that lecture, we have shown we want to take the sample of the current just before the switch turns on because we are talking about trailing edge modulation trailing edge PWM right? So, we are just taking the sample before the switch turns on.

But, keeping in mind the conversion time as well as the computational time, we are using that sample current for the next cycle and we are adding this ram which is this color. So, its slope is  $m_c$ . So, that is the emulated RAM; that means, we are getting the emulated current for the  $n$ th cycle that is equal to the inductor current of the  $n-1$  cycle plus  $m_c$ .

That means we want to emulate the current right. So, I will say emulate current in the time domain in the time domain will be  $m_c t$  into  $t$ . And this is during the  $n$ th clock cycle. So, we are taking the initial value for the previous cycle and the current cycle will use this RAM and update it. Now, the question is one might think that if you are under steady state if you take the  $m_c$  to be identical to  $m_1$ ; that means if you take  $m_c$  the emulated slope which is my emulated slope, and  $m_1$  is my actual slope right.

So, emulated slope and the actual slope are actual; that means, both are the actual rising slope of the inductor current. So, this is you can see this is the actual blue color is the actual rising slope of the inductor current. So, one might think if you want to get the exact current

waveform inside the digital platform by emulation. So, it is very like common very common that we want to take emulated current exactly equal to the rising slope.

First of all, that method is not robust because what is  $m_1$ ?  $m_1$  is  $V_{in} - V_0$  by  $l$ . So, to extract that information you need to get input voltage information that you can sense and you can put a pass through D to A to convert ADC voltage you are already taking no problem, but how do you get the inductance value? So, exact information on the inductance is not available because inductance can vary.

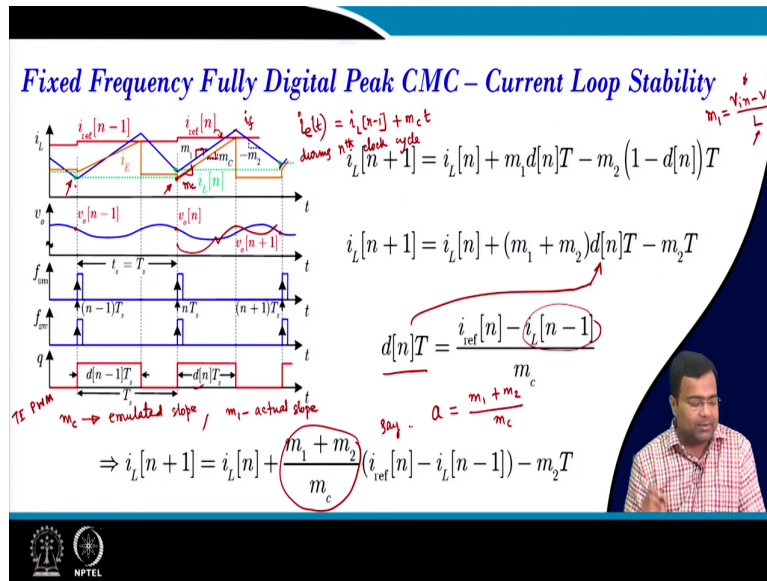
Even if you take the BH curve of the magnetic material of the inductor it will show that as current increases the inductor can decrease because if you are pushing more toward the saturation region then the inductance value decreases. So, as a result, this value may not remain constant or there can be a deviation plus or minus 10, 20 percent deviation. So, you may not know the exact value of  $l$ .

Even if you try to extract the exact value and if you want to set it as emulated we want to see what is the effect. So, again this is the basic equation of the current loop that we have derived because if you take for the  $n$ th cycle let us say this is my  $n$ th cycle. So, starting value is  $I_{l,n}$  which is the initial value of the cycle. That means I will say this is  $i_{l,n}$  this value is our  $i_{l,n}$ .

Then, it will be and this expression we have seen in the previous like a few slides back that it is nothing, but  $i_{l,n+1}$  is  $i_{l,n} + m_1 d_n T - m_2 (1 - d_n) T$  where  $d_n T$  is the duty ratio for this cycle ok. So, how do you get it? Let us say  $i_{l,n}$  that is the value here. So, if this is the value this will be equal to let us say, what is the final value? So, let us say it is the final value of this.

So,  $i_{l,n+1} - m_2 (1 - d_n) T$ , correct? Now, what is  $i_{l,n+1}$ ?  $i_{l,n+1}$  equal to  $m_1$  sorry. So,  $i_{l,n+1}$  equal to  $i_{l,n}$  that is this value plus  $m_1 d_n T$ . Now, you replace here then you will get  $i_{l,n} + m_1 d_n T - m_2 (1 - d_n) T$  plus  $m_2 (1 - d_n) T$  is equal to  $i_{l,n} + m_1 d_n T$  and this is exactly is this equation ok.

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So, next ok so, since it is overlapping. So, I think I have already given the intermediate step to show how it is coming. So, now, you can derive. So, next, is that you can rearrange this equation then what will do? Next, this  $d[n]T$  I have shown you the  $d[n]T$  is if it is, now if it is a fully digital because we know  $d[n]T$  it is now not straightforward because  $d[n]T$  is a duty ratio expression.

How we are getting the duty ratio expression? So, the starting value of this cycle is coming from the emulated slope and you can see this starting value for the emulated current the starting value is the inductor sample value at the previous cycle here. So, that is why it is  $i_L[n-1] - i_{ref}[n]$  which is this cycle. This is the  $i_{ref}[n] - i_L[n-1]$  divided by  $m_c$ ;  $m_c$  is the slope of this emulated current.

So, since the emulated current start with  $i_L[n-1]$  and  $i_{ref}[n]$ . So,  $i_{ref}[n] - i_L[n-1]$  by  $m_c$  is the  $d[n]T$ . Now, you substitute this  $d[n]T$  here ok. Then what will get? This is that complete equation. Now, this term let us say I take  $a$ , an equal to  $m_1 + m_2$  by  $m_c$  let us say. So, say this is what we have taken.

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**Fixed Frequency Fully Digital Peak CMC – Current Loop Stability**

$$i_L[n+1] = i_L[n] + \frac{m_1 + m_2}{m_c} (i_{ref}[n] - i_L[n-1]) - m_2 T$$

**Perturbed dynamics**

$$\tilde{i}_L[n+1] = \tilde{i}_L[n] + \frac{m_1 + m_2}{m_c} (\tilde{i}_{ref}[n] - \tilde{i}_L[n-1])$$

**Apply Z transform**

$$z\tilde{i}_L(z) = \tilde{i}_L(z) + a\tilde{i}_{ref}(z) - az^{-1}\tilde{i}_L(z)$$

So, this is the one, now I want to again do the perturbation because I want to do perturbation and I want to see the effect. So, here if we perturb the initial condition we can find out what is the requirement of the stability of the  $i_{ref}[n]$  is constant. So, now if we apply the Z transform here then, since it is a perturb term there is an initial condition is for this term; if you straightway apply the perturbation it will be  $z$  into  $i_L(z)$  then  $i_L(z)$  then this I have taken  $a$ .

So, this whole term I have taken equal to  $a$ ; and then an into  $i_{ref}(z)$  minus this will be a  $z$  inverse of  $i_L(z)$ .

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**Fixed Frequency Fully Digital Peak CMC – Current Loop Stability**

**Z transform**

$$z\tilde{i}_L(z) = \tilde{i}_L(z) + a\tilde{i}_{ref}(z) - az^{-1}\tilde{i}_L(z)$$

$$\tilde{i}_L(z)[z - 1 + az^{-1}] = \tilde{i}_{ref}(z)a$$

*Roots of  $z^2 - z + a = 0$  if  $\tilde{i}_{ref}(z) = 0$  must lie inside the unit circle. Zero-input stability.*

$$\frac{\tilde{i}_L(z)}{\tilde{i}_{ref}(z)} = \frac{az}{z^2 - z + a} \quad \text{where } a = \frac{m_1 + m_2}{m_c}$$

And then if you substitute rearrange this equation you will get  $i_l(z)$  by  $i_{ref}(z)$  equal to this; that means, if you talk about only perturbation in the initial current no perturbation here then you will get  $i_l(z)$  this into  $z^2 - z + a$ . And that will be equal to 0, if  $i_{ref}(z)$  this  $z$  equal to 0 or there is no perturbation. So, this is my zero-input stability.

So, zero input stability and this is the equation if you perturb  $i_{ref}$  then how  $i_l(z)$  is also getting affected. So, for zero input stability, we have to ensure that the poles of this; that means, the roots of this equation if I say poles or eigenvalue whatever. So, you can say the root of  $z$  must lie inside the unit circle and that can be proved if you write this equation.

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**Fixed Frequency Fully Digital Peak CMC - Current Loop Stability**

$$\frac{\tilde{i}_l(z)}{\tilde{i}_{ref}(z)} = \frac{az}{z^2 - z + a}$$
 where  $a = \frac{m_1 + m_2}{m_c}$

For current-loop stability

$$a < 1 \Rightarrow \frac{m_1 + m_2}{m_c} < 1$$

$$z^2 - z + a = 0$$

$$\left(z - \frac{1}{2}\right)^2 = \left(\frac{1}{2}\right)^2 - a$$

$$z = \frac{1}{2} \pm \frac{1}{2} \sqrt{1 - 4a}$$

$a > \frac{1}{4}$   
 complex conjugate  
 $|z| < 1 \Rightarrow a < 1$

$a = \frac{1}{4}$   
 $a < 1$

So, you are interested here. And that can be proved that it will be true if we take  $a$  less than 1. It can be easily proved because if I write  $z^2 - z + a$  that equal to 0, I can write  $z^2 - z + a = 0$ . I can write  $z^2 - z + \frac{1}{4} = \frac{1}{4}$  minus  $a$ . So, I can write  $z$  equal to  $\frac{1}{2} \pm \sqrt{\frac{1}{4} - a}$ . So, if I take half common what we will get? We will get so  $1 - 4a$ , correct? So, now, you can see  $a$  is always greater than  $\frac{1}{4}$ .

So, from here you can say  $a$  is always greater than 0 sorry 0 because all are positive, all are positive so it is common. Now, if  $a$  equal to 0, then you can show that suppose if  $a$  equal to 0 then  $z$  will have two values; one will be 0 another will be 1. So; that means, one will be on the unit circle another will be at 0, the origin, but since  $a$  is greater than 0. So, if you keep on increasing  $a$ , and when  $a$  become like a one-fourth then this term will be 0.

So, it will be half; that means, if you draw the root locus you will find the roots are slowly coming inside the unit circle and they will be identical when equal to 1 by 4. Then, again if you keep on increasing the value of an again they will be different and you will get. So, for a greater than 1.4 so we will get complex conjugate, complex conjugate.

And if a becomes 1, if a becomes 1 then what will happen? Then you will get; that means, equal to 1 1 minus 4. So, you can prove that the magnitude of z will be inside the unit circle will imply that a must be greater the a must be less than 1.

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**Fixed Frequency Fully Digital Peak CMC – Current Loop Stability**

$$\frac{\tilde{i}_L(z)}{\tilde{i}_{ref}(z)} = \frac{az}{z^2 - z + a} \quad \text{where } a = \frac{m_1 + m_2}{m_c} \quad a > 0$$

For current-loop stability

$$a < 1 \Rightarrow \frac{m_1 + m_2}{m_c} < 1$$

$$\Downarrow$$

$$m_c > m_1 + m_2$$

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$$z^2 - 2za + a^2 = 0$$

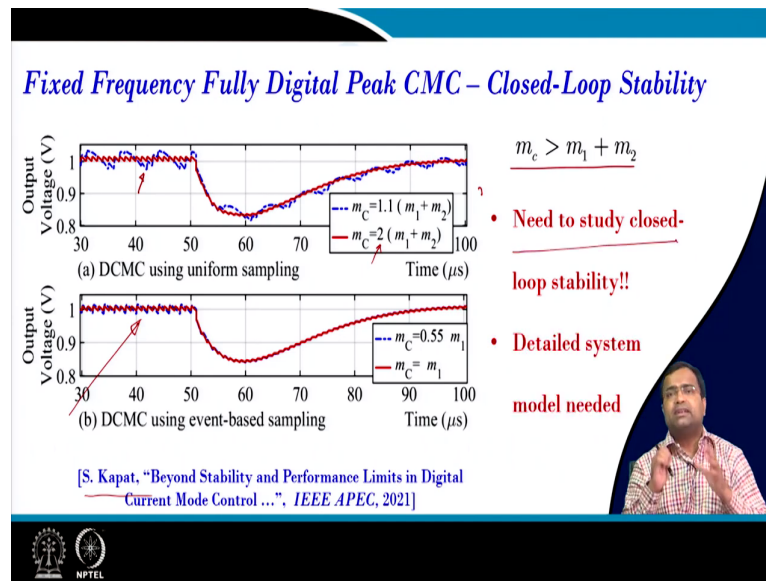
$$(z - \frac{1}{2})^2 = (\frac{1}{2})^2 - a$$

$$z = \frac{1}{2} \pm \frac{1}{2} \sqrt{1 - 4a}$$

[S. Kapat, "Beyond Stability and Performance Limits in Digital Current Mode Control ...", IEEE APEC, 2021]

So, that can be proved. I am not deriving so that means if you take this. So, this can be proved that a; that means, a must be this and this will be m c must be; that means, what is it is m 1 plus m 2 by m c. So, m c must be greater than 0. And for buck converter this is; means, your m c must be at least m 1 plus m 2 which means it is greater than the rising slope. So, you cannot set the emulated slope to be a rising flow; it has to be greater. And, this is the minimum requirement only with the closed inner loop.

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But once you close the outer loop I am just showing an example because I will go to this closed loop analysis later. So, here I am showing if I just close the outer loop and if I set  $m_c$  equal to 1.1 times because this is greater than; that means, I have taken  $m_c$  to be greater than  $m_1 + m_2$ . But, with the closed loop you see the blue lines indicate there is subharmonic oscillation.

This is for a closed loop. So, that means, the condition we got is just for inner loop stability, but if you close the outer loop because of the sampling effect and another effect and we will discuss closed-loop eigenvalues that will go outside the unit circle, and your current loop closed loop become unstable. And that is you know shown from the blue stage, but if you increase further then you can make it stable.

So, it is interesting to show how this  $m_c$  should be selected and that will depend on the controller gain. But I am showing another approach of even sampling you can get the detail in this paper, but it is not necessary I am just showing that using this approach of digital current mode control there is an alternative architecture where it is emulated only, but the different sampling technique.

And this is not covered in our lecture this may be for an advanced topic, but what I am saying? In the regular current mode control analysis for full digital, it will be unstable even just slightly increase you know a higher value of  $m_1 + m_2$  is not sufficient. So, you need to take an even much higher closed loop. So; that means, we need to go for closed-loop



stability analysis. So, only inner loop stability is not enough and we need a detailed system model.

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**CONCLUSION**

- Discrete-time modeling analog current loop
- Current loop stability under mixed-signal CMC
- Current-loop stability under fully digital CMC
- Need for going closed-loop stability analysis

So, in summary, we have discussed discrete-time modeling with analog current loop, we have discussed the current loop stability under mixed signal current mode control, and we have discussed current loop stability under fully digital current mode control. And all these we have only considered the closed inner loop, not the outer loop that is still open.

And, we saw that with this only inner loop stability we can ensure when there is no closed loop controller, but once we have the closed loop controller then the stability requirement will further become complicated and we need the full model of the system.

So, we will discuss this full modeling complete modeling of the switching converter in the next lecture. We will start with how to do the complete model or discrete-time model of the closed-loop converter. So, with this, I want to finish it here.

Thank you very much.